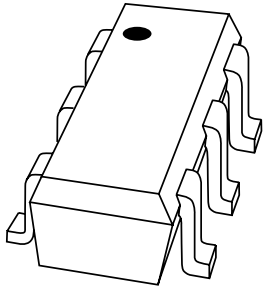


DATA SHEET



BF1205 Dual N-channel dual gate MOS-FET

Product specification

2003 Sep 30

Dual N-channel dual gate MOS-FET

BF1205

FEATURES

- Two low noise gain controlled amplifiers in a single package. One with a fully integrated bias and one with a partly integrated bias
- Internal switch reduces the number of external components
- Superior cross-modulation performance during AGC
- High forward transfer admittance
- High forward transfer admittance to input capacitance ratio.

APPLICATIONS

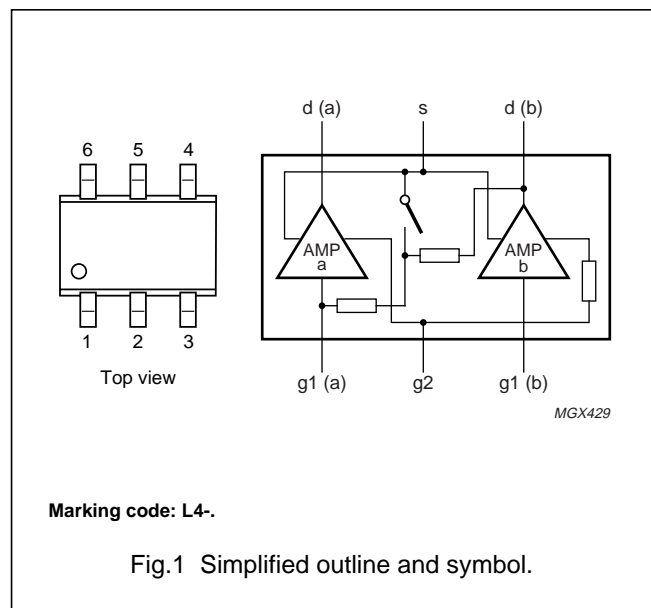
- Gain controlled low noise amplifiers for VHF and UHF applications with 5 V supply voltage, such as digital and analog television tuners and professional communications equipment.

DESCRIPTION

The BF1205 is a combination of two equal dual gate MOS-FET amplifiers with shared source and gate 2 leads and an integrated switch. The integrated switch is operated by the gate 1 bias of amplifier b. The source and substrate are interconnected. Internal bias circuits enable DC stabilization and a very good cross-modulation performance during AGC. Integrated diodes between the gates and source protect against excessive input voltage surges. The transistor is encapsulated in SOT363 micro-miniature plastic package.

PINNING - SOT363

PIN	DESCRIPTION
1	gate 1 (a)
2	gate 2
3	gate 1 (b)
4	drain (b)
5	source
6	drain (a)



ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
BF1205	–	Plastic surface mounted package; 6 leads	SOT363

Dual N-channel dual gate MOS-FET

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per MOS-FET; unless otherwise specified						
V_{DS}	drain-source voltage		–	–	10	V
I_D	drain current (DC)		–	–	30	mA
P_{tot}	total power dissipation	$T_s \leq 102\text{ }^\circ\text{C}$; temperature at the soldering point of the source lead	–	–	200	mW
$ y_{fs} $	forward transfer admittance	$I_D = 12\text{ mA}$	26	31	40	mS
C_{ig1-ss}	input capacitance at gate 1	amp. a: $f = 1\text{ MHz}$	–	1.8	2.3	pF
		amp. b: $f = 1\text{ MHz}$	–	2.0	2.5	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	20	–	fF
NF	noise figure	amp. a: $f = 800\text{ MHz}$	–	1.2	1.9	dB
		amp. b: $f = 800\text{ MHz}$	–	1.4	2.1	dB
X_{mod}	cross-modulation	amp. a: input level for $k = 1\%$ at 40 dB AGC	98	102	–	dB μ V
		amp. b: input level for $k = 1\%$ at 40 dB AGC	100	105	–	dB μ V
T_j	junction temperature		–	–	150	$^\circ\text{C}$

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per MOS-FET; unless otherwise specified					
V_{DS}	drain-source voltage		–	10	V
I_D	drain current (DC)		–	30	mA
I_{G1}	gate 1 current		–	± 10	mA
I_{G2}	gate 2 current		–	± 10	mA
P_{tot}	total power dissipation	$T_s \leq 102\text{ }^\circ\text{C}$; note	–	200	mW
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	junction temperature		–	150	$^\circ\text{C}$

Note

- T_s is the temperature at the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	240	K/W

Dual N-channel dual gate MOS-FET

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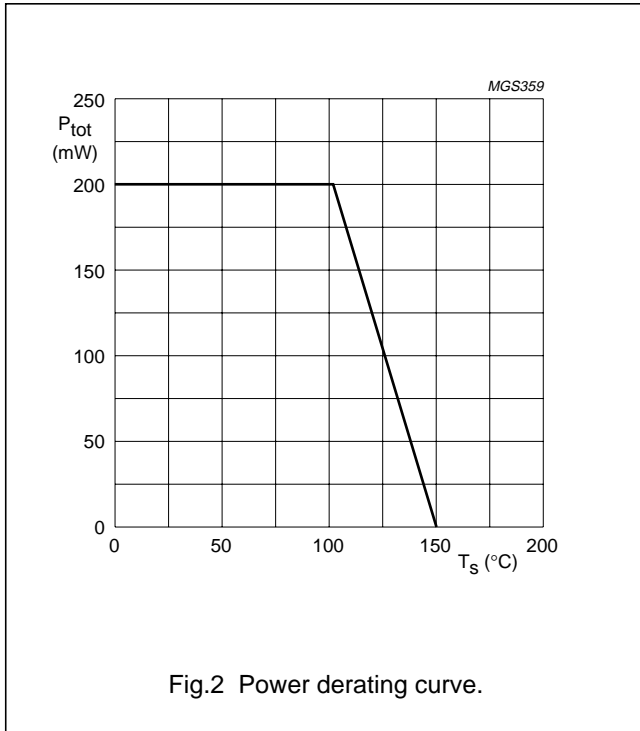


Fig.2 Power derating curve.

STATIC CHARACTERISTICS

$T_j = 25\text{ }^\circ\text{C}$; per MOS-FET; unless otherwise specified.

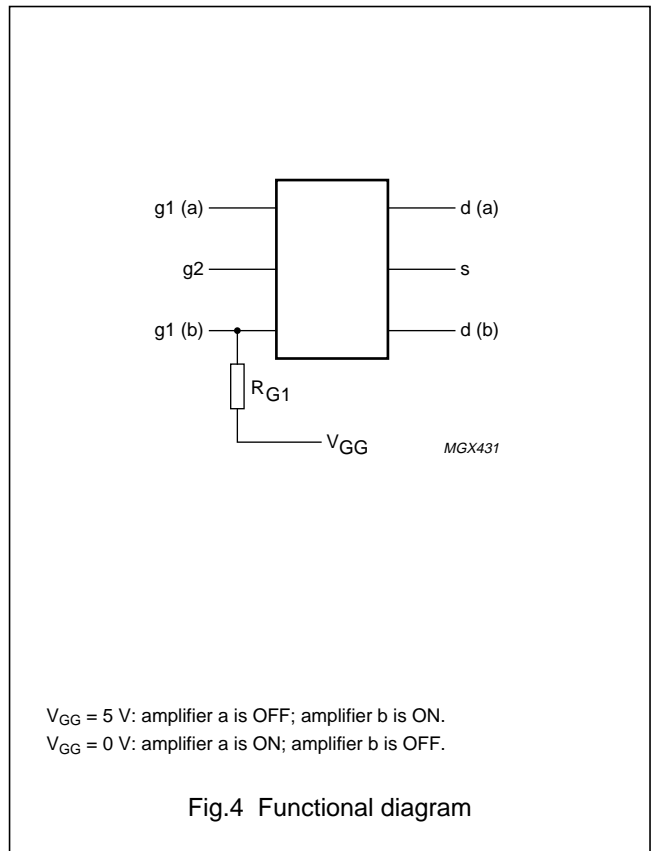
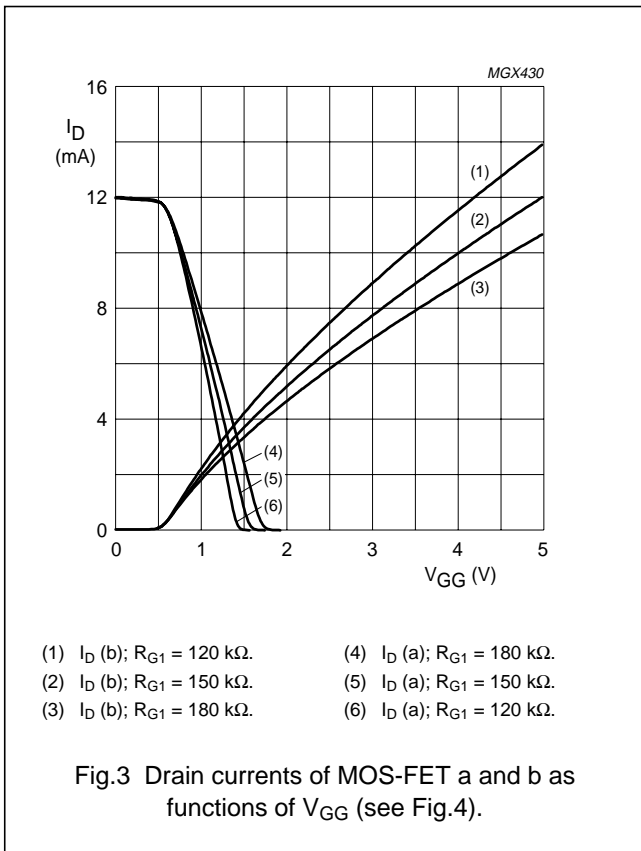
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	amp. a: $V_{G1-S} = V_{G2-S} = 0\text{ V}$; $I_D = 10\text{ }\mu\text{A}$	10	–	V
		amp. b: $V_{G1-S} = V_{G2-S} = 0\text{ V}$; $I_D = 10\text{ }\mu\text{A}$	7	–	V
$V_{(BR)G1-SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0\text{ V}$; $I_{G1-S} = 10\text{ mA}$	6	10	V
$V_{(BR)G2-SS}$	gate-source breakdown voltage	$V_{GS} = V_{DS} = 0\text{ V}$; $I_{G2-S} = 10\text{ mA}$	6	10	V
$V_{(F)S-G1}$	forward source-gate voltage	$V_{G2-S} = V_{DS} = 0\text{ V}$; $I_{S-G1} = 10\text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate voltage	$V_{G1-S} = V_{DS} = 0\text{ V}$; $I_{S-G2} = 10\text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate-source threshold voltage	$V_{DS} = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate-source threshold voltage	$V_{DS} = 5\text{ V}$; $V_{G1-S} = 5\text{ V}$; $I_D = 100\text{ }\mu\text{A}$	0.4	1.0	V
I_{DSX}	drain-source current	amp. a: $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 150\text{ k}\Omega$; note 1	8	16	mA
		amp. b: $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $R_{G1} = 150\text{ k}\Omega$; note 2	8	16	mA
I_{G1-S}	gate cut-off current	amp. a: $V_{G1-S} = 5\text{ V}$; $V_{G2-S} = V_{DS} = 0\text{ V}$	–	50	nA
		amp. b: $V_{G1-S} = 5\text{ V}$; $V_{G2-S} = V_{DS} = 0\text{ V}$	–	50	nA
I_{G2-S}	gate cut-off current	$V_{G2-S} = 4\text{ V}$; $V_{G1-S} = V_{DS} = 0\text{ V}$	–	20	nA

Note

- R_{G1} connects gate 1 (b) to $V_{GG} = 0\text{ V}$ (see Fig.4).
- R_{G1} connects gate 1 (b) to $V_{GG} = 5\text{ V}$ (see Fig.4).

Dual N-channel dual gate MOS-FET

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Dual N-channel dual gate MOS-FET

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DYNAMIC CHARACTERISTICS AMPLIFIER aCommon source; $T_{amb} = 25\text{ °C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 5\text{ V}$; $I_D = 12\text{ mA}$; note 1

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	$T_j = 25\text{ °C}$	26	31	40	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	1.8	2.3	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	3.3	–	pF
C_{oss}	output capacitance	$f = 1\text{ MHz}$	–	0.75	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	20	–	fF
G_{tr}	power gain	$f = 200\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 0.5\text{ mS}$; $B_L = B_{L(opt)}$	31	35	39	dB
		$f = 400\text{ MHz}$; $G_S = 2\text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 1\text{ mS}$; $B_L = B_{L(opt)}$	27	31	35	dB
		$f = 800\text{ MHz}$; $G_S = 3.3\text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 1\text{ mS}$; $B_L = B_{L(opt)}$	22	26	30	dB
NF	noise figure	$f = 10.7\text{ MHz}$; $G_S = 20\text{ mS}$; $B_S = 0$	–	4	–	dB
		$f = 400\text{ MHz}$; $Y_S = Y_{S(opt)}$	–	1.1	1.7	dB
		$f = 800\text{ MHz}$; $Y_S = Y_{S(opt)}$	–	1.2	1.9	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 0 dB AGC; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 2	90	–	–	dB μ V
		input level for $k = 1\%$ at 10 dB AGC; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 2	–	90	–	dB μ V
		input level for $k = 1\%$ at 40 dB AGC; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; note 2	98	102	–	dB μ V

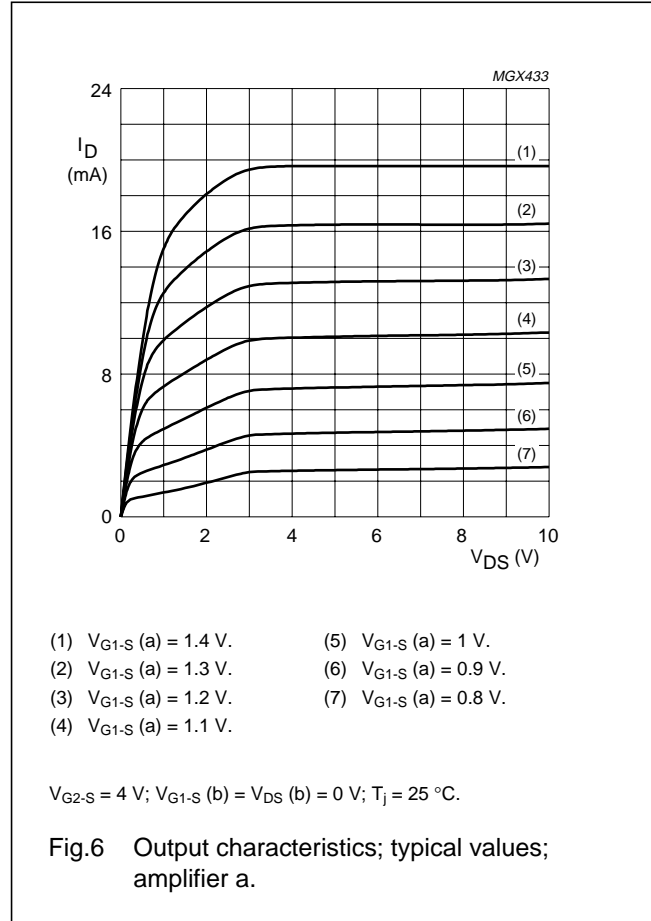
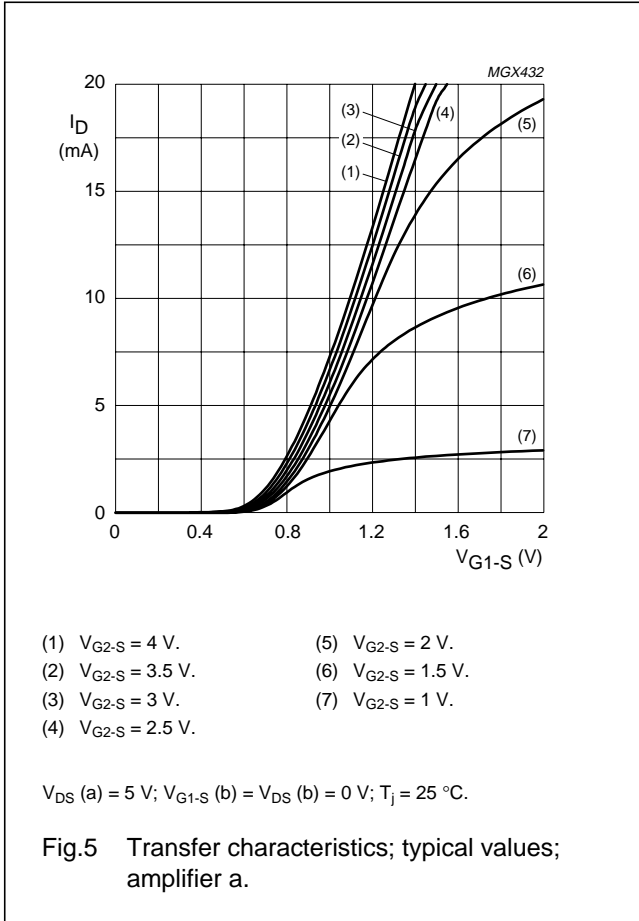
Notes

1. For the MOS-FET not in use: $V_{G1-S} (b) = 0\text{ V}$; $V_{DS} (b) = 0\text{ V}$.
2. Measured in Fig.13 test circuit.

Dual N-channel dual gate MOS-FET

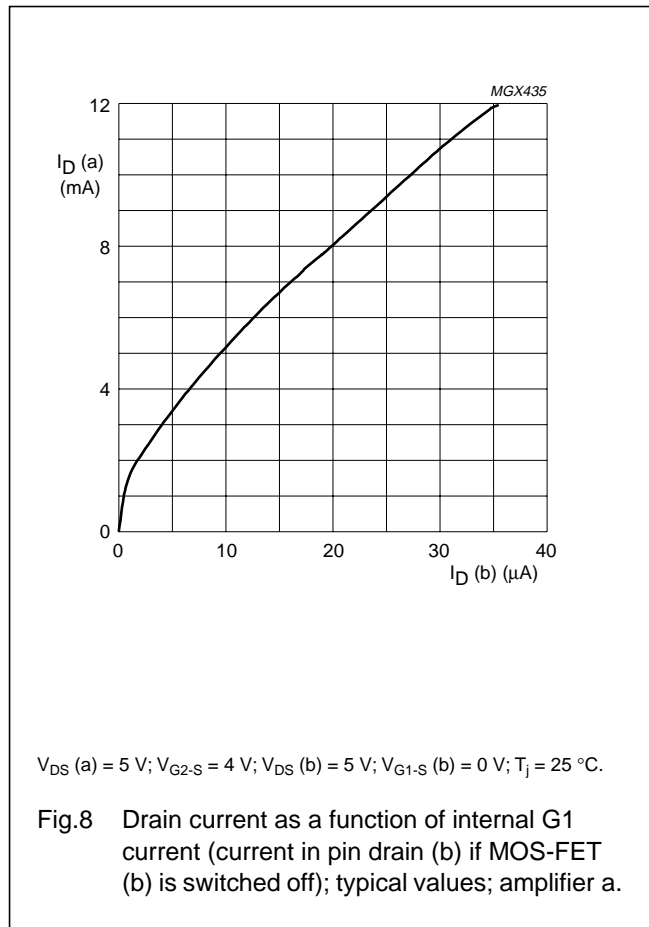
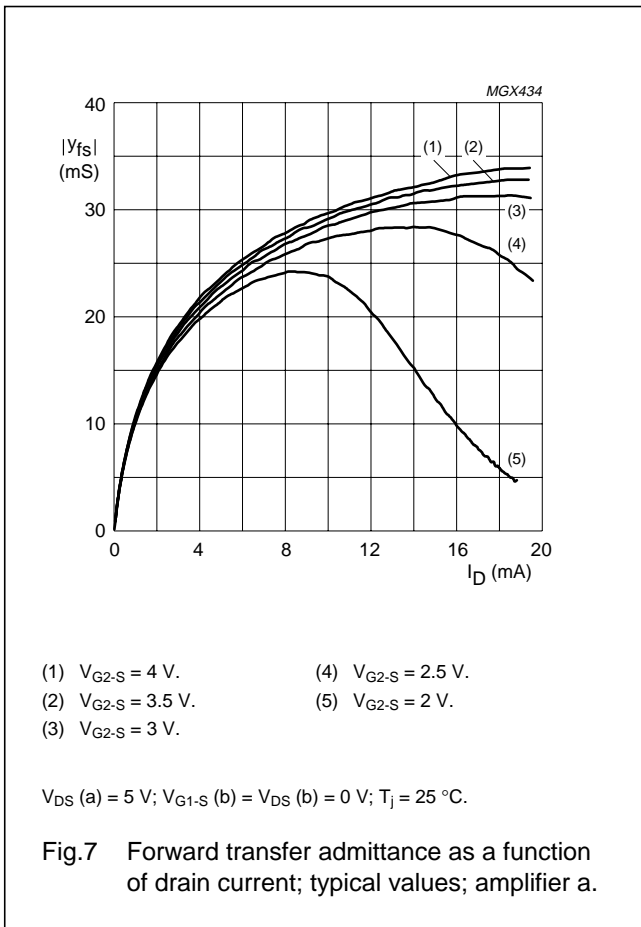
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GRAPHS FOR AMPLIFIER a



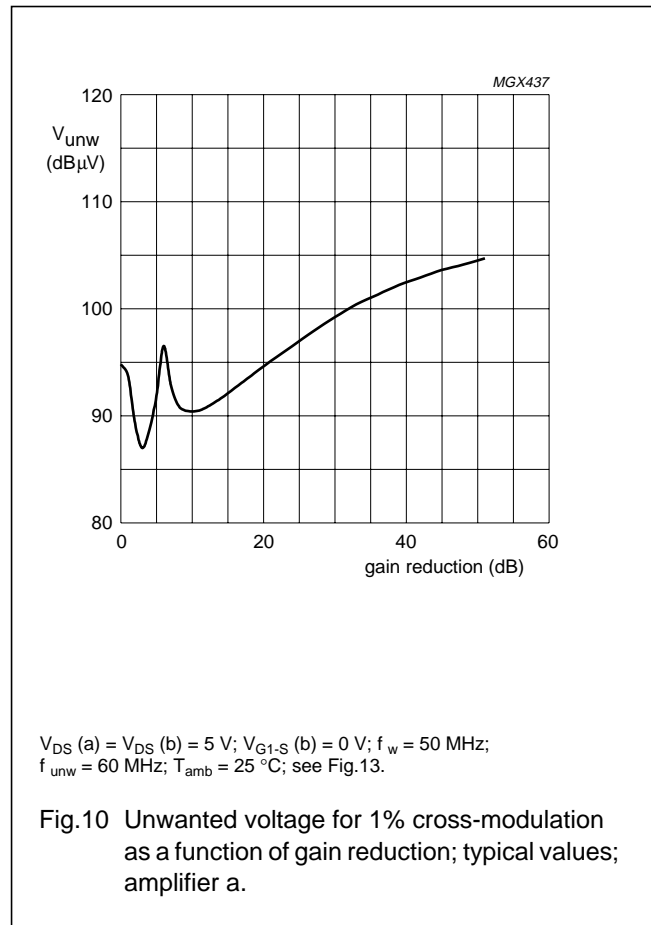
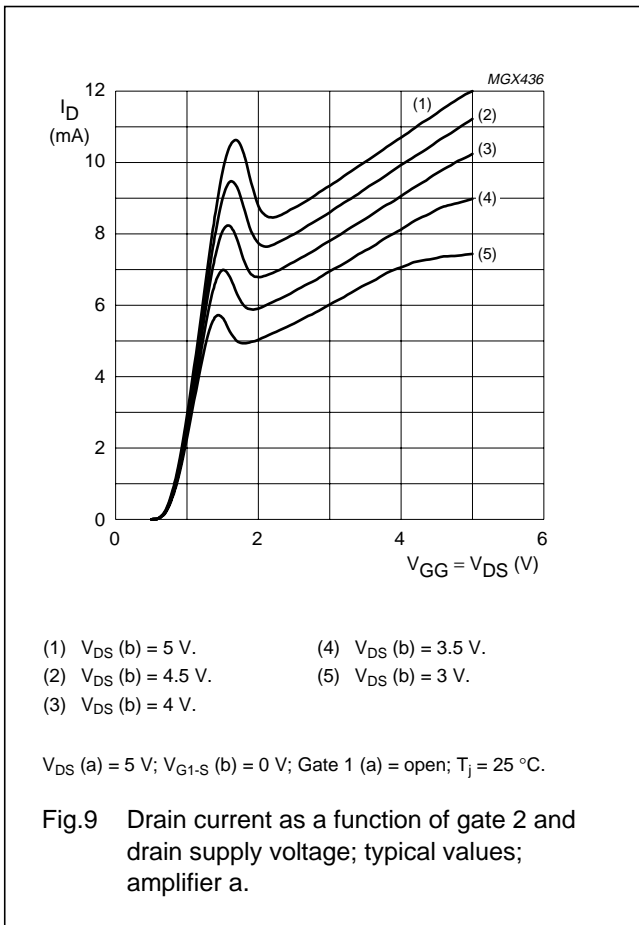
Dual N-channel dual gate MOS-FET

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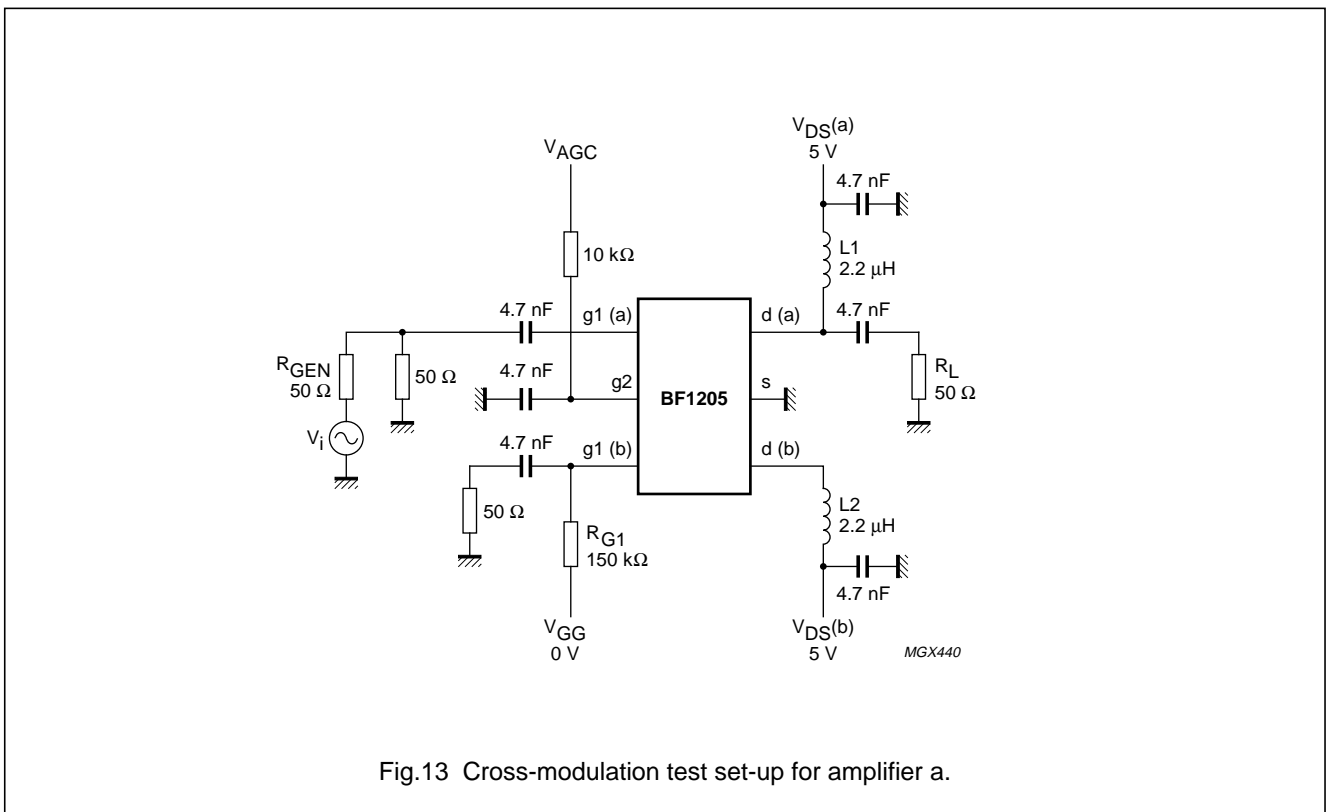
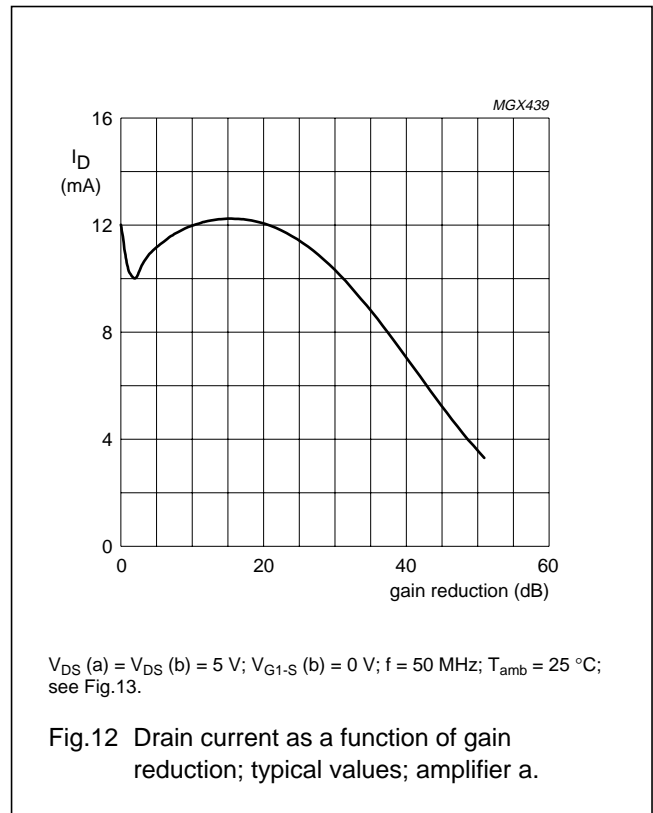
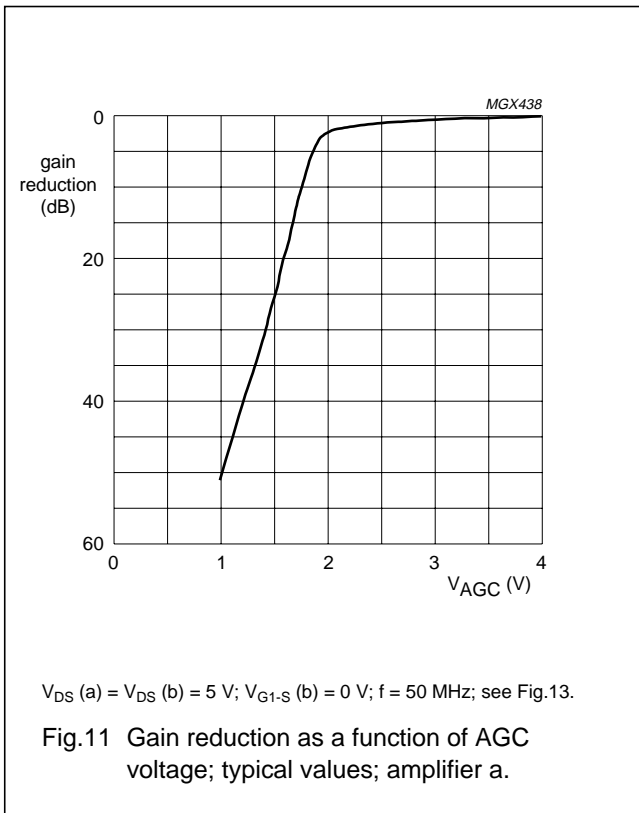
Dual N-channel dual gate MOS-FET

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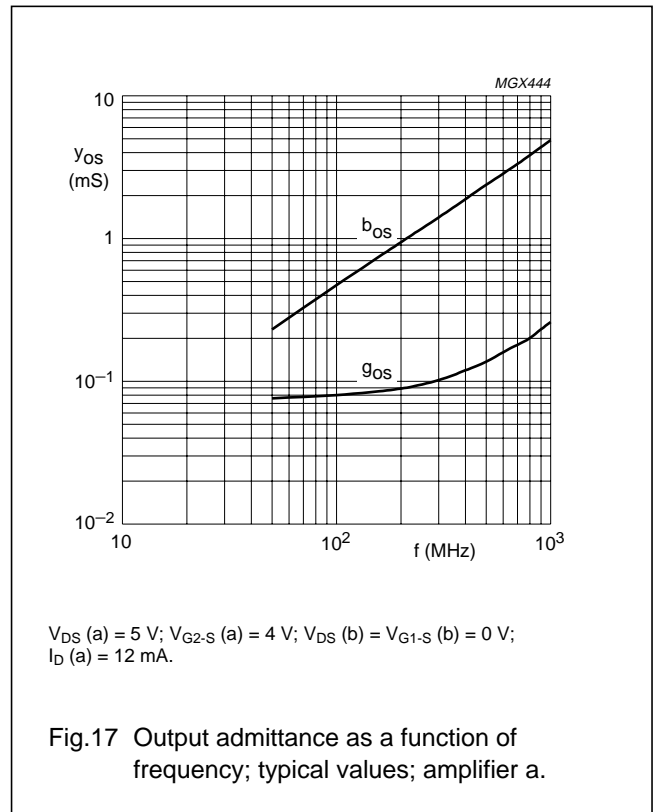
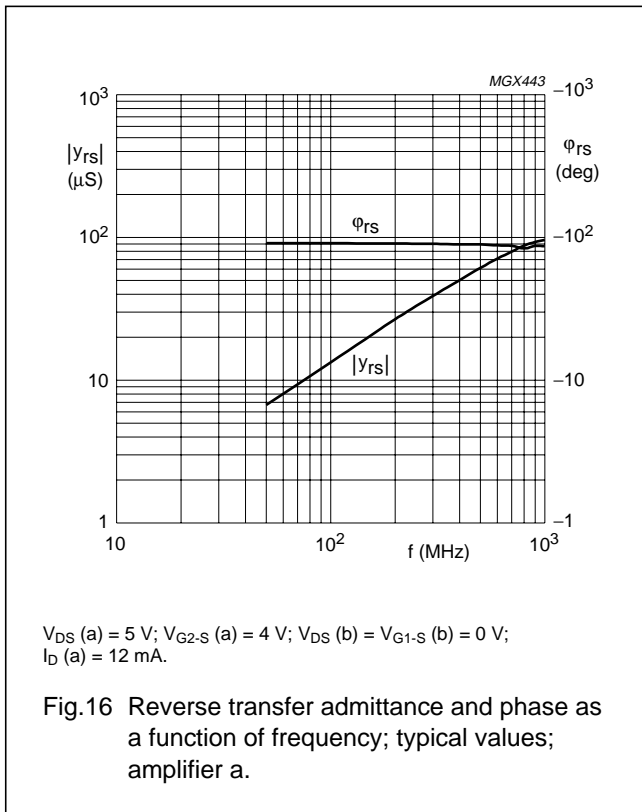
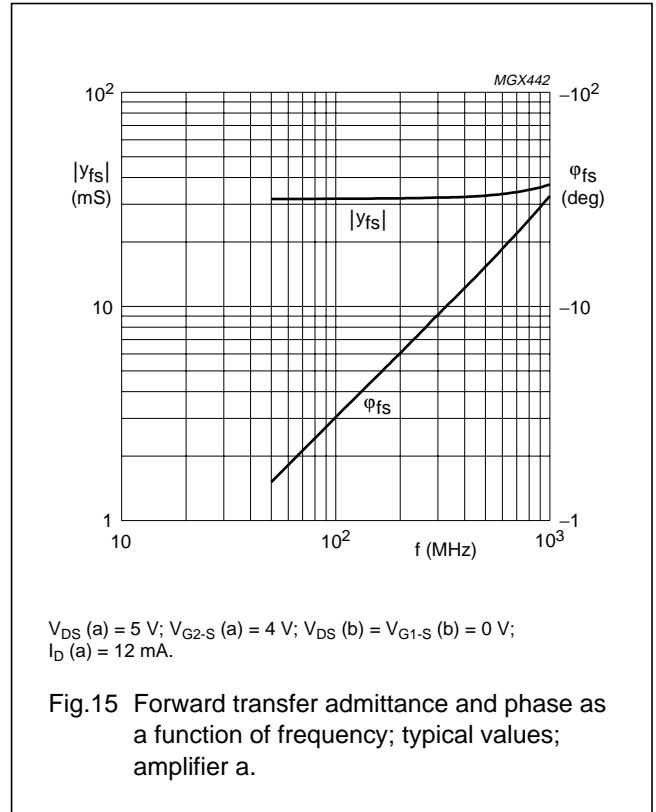
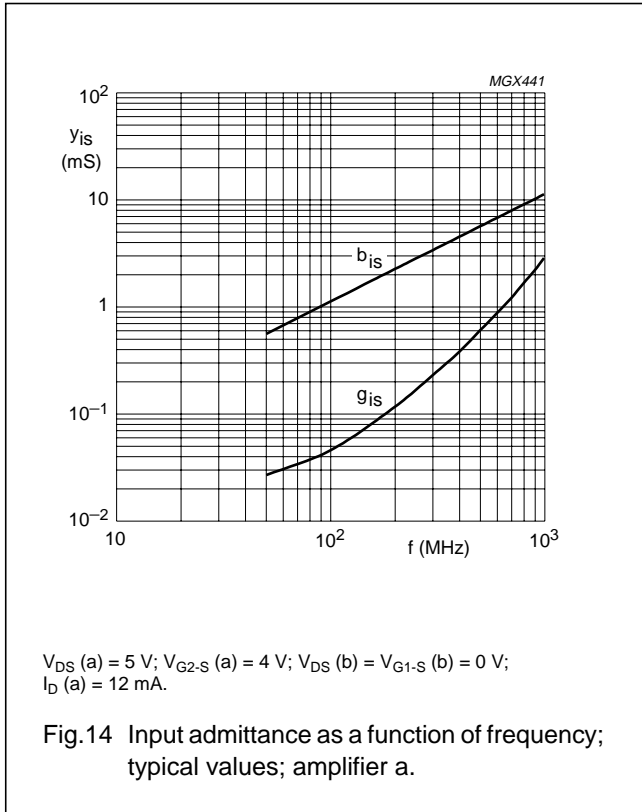
Dual N-channel dual gate MOS-FET

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Dual N-channel dual gate MOS-FET

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Dual N-channel dual gate MOS-FET

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Scattering parameters: amplifier a

 $V_{DS} (a) = 5 \text{ V}$; $V_{G2-S} = 4 \text{ V}$; $I_D (a) = 12 \text{ mA}$; $V_{DS} (b) = 0 \text{ V}$; $V_{G-1S} (b) = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.997	-3.70	3.15	175.99	0.00067	86.39	0.992	-1.38
100	0.995	-7.37	3.15	171.92	0.00132	84.34	0.991	-2.83
200	0.988	-14.64	3.12	163.99	0.00262	79.71	0.990	-5.62
300	0.976	-21.85	3.09	156.06	0.00373	75.29	0.988	-8.40
400	0.963	-28.95	3.04	148.32	0.00471	71.43	0.985	-11.15
500	0.944	-35.98	2.99	140.52	0.00557	66.89	0.982	-13.88
600	0.924	-42.90	2.94	132.88	0.00624	63.52	0.978	-16.65
700	0.900	-49.77	2.87	125.30	0.00669	60.09	0.975	-19.35
800	0.874	-56.61	2.81	117.79	0.00701	59.58	0.972	-22.08
900	0.846	-63.18	2.73	110.29	0.00705	52.42	0.968	-24.87
1000	0.817	-69.84	2.65	102.91	0.00688	49.17	0.965	-27.63

Noise data

 $V_{DS} (a) = 5 \text{ V}$; $V_{G2-S} = 4 \text{ V}$; $I_D (a) = 12 \text{ mA}$; $V_{DS} (b) = 0 \text{ V}$; $V_{G-1S} (b) = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$

f (MHz)	F MIN (dB)	GAMMA OPT		Rn (Ω)
		(ratio)	(deg)	
400	1.1	0.719	16.16	31.18
800	1.2	0.628	32.7	29.74

DYNAMIC CHARACTERISTICS AMPLIFIER b

Common source; $T_{amb} = 25 \text{ }^\circ\text{C}$; $V_{G2-S} = 4 \text{ V}$; $V_{DS} = 5 \text{ V}$; $I_D = 12 \text{ mA}$

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	$T_j = 25 \text{ }^\circ\text{C}$	26	31	40	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1 \text{ MHz}$	–	2.0	2.5	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1 \text{ MHz}$	–	3.3	–	pF
C_{oss}	output capacitance	$f = 1 \text{ MHz}$	–	0.85	–	pF
C_{rss}	reverse transfer capacitance	$f = 1 \text{ MHz}$	–	20	–	fF
G_{tr}	power gain	$f = 200 \text{ MHz}$; $G_S = 2 \text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 0.5 \text{ mS}$; $B_L = B_{L(opt)}$; note 1	30	34	38	dB
		$f = 400 \text{ MHz}$; $G_S = 2 \text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 1 \text{ mS}$; $B_L = B_{L(opt)}$; note 1	27	31	35	dB
		$f = 800 \text{ MHz}$; $G_S = 3.3 \text{ mS}$; $B_S = B_{S(opt)}$; $G_L = 1 \text{ mS}$; $B_L = B_{L(opt)}$; note 1	22	26	30	dB
NF	noise figure	$f = 10.7 \text{ MHz}$; $G_S = 20 \text{ mS}$; $B_S = 0$	–	4	–	dB
		$f = 400 \text{ MHz}$; $Y_S = Y_{S(opt)}$	–	1.3	1.9	dB
		$f = 800 \text{ MHz}$; $Y_S = Y_{S(opt)}$	–	1.4	2.1	dB

Dual N-channel dual gate MOS-FET

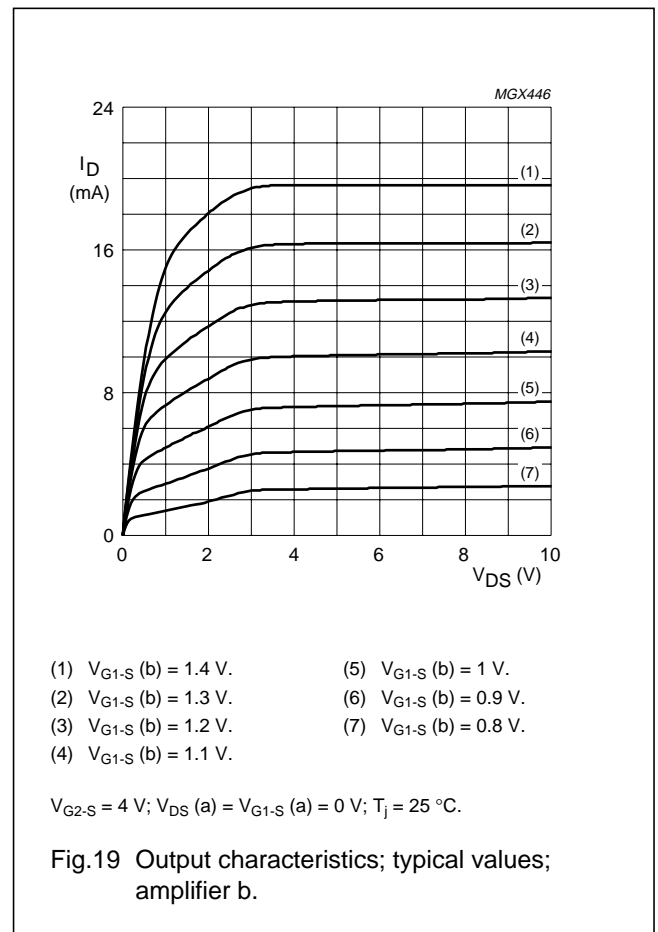
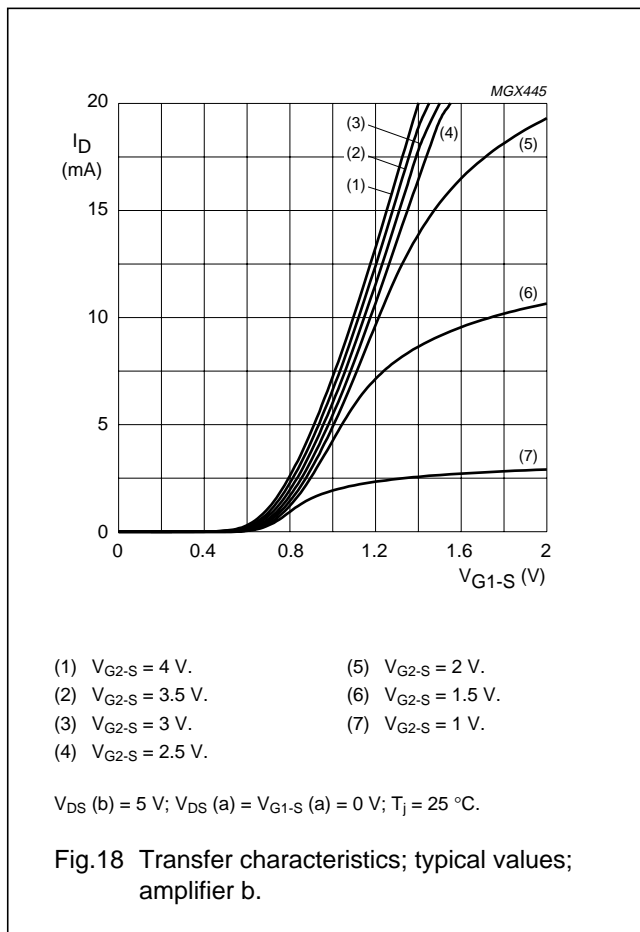
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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
X_{mod}	cross-modulation	input level for $k = 1\%$ at 0 dB AGC; $f_w = 50$ MHz; $f_{unw} = 60$ MHz; note 2	90	–	–	$\text{dB}\mu\text{V}$
		input level for $k = 1\%$ at 10 dB AGC; $f_w = 50$ MHz; $f_{unw} = 60$ MHz; note 2	–	92	–	$\text{dB}\mu\text{V}$
		input level for $k = 1\%$ at 40 dB AGC; $f_w = 50$ MHz; $f_{unw} = 60$ MHz; note 2	100	105	–	$\text{dB}\mu\text{V}$

Notes

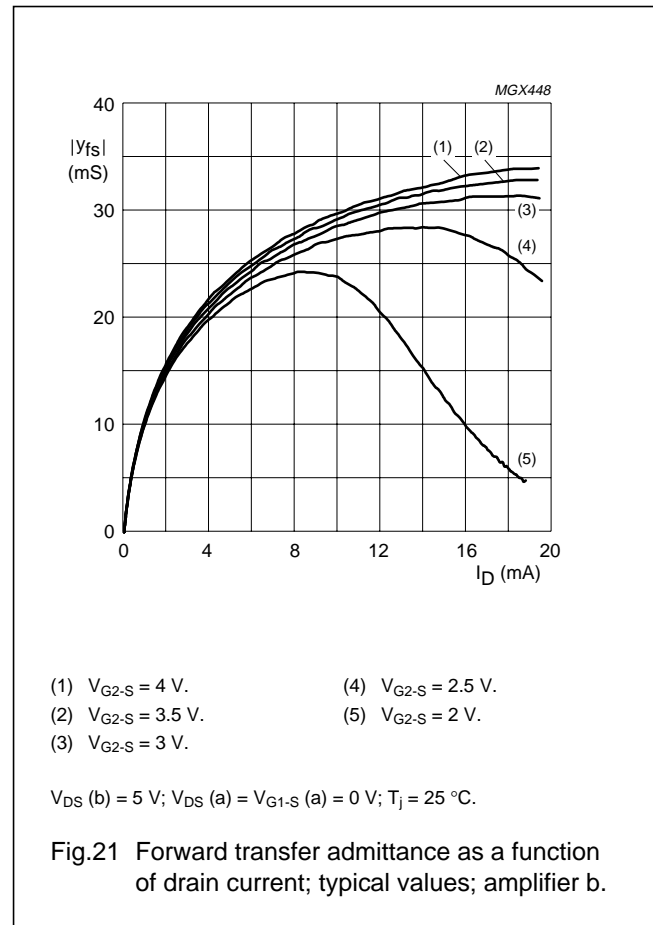
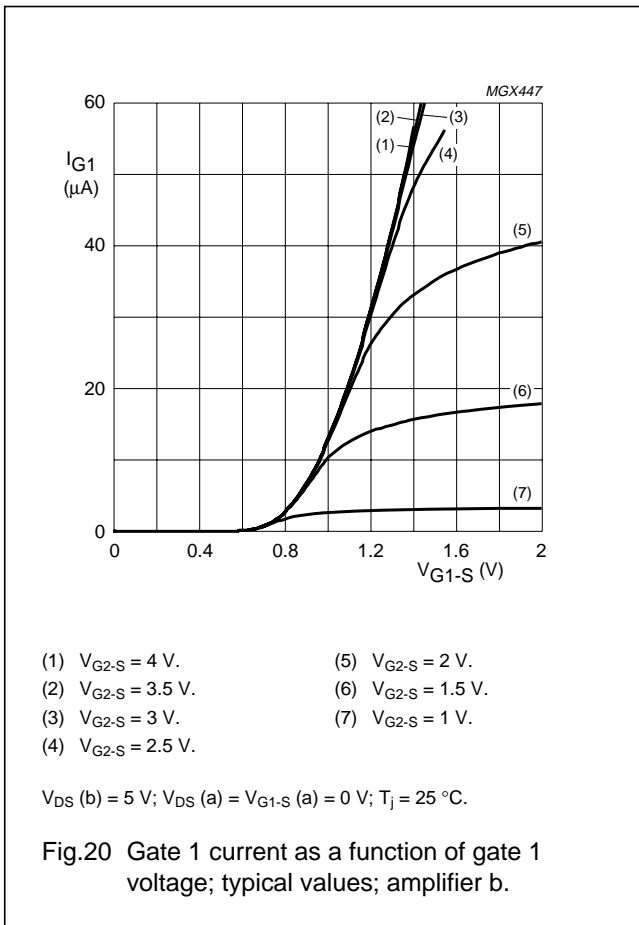
- For the MOS-FET not in use: $V_{G1-S} (a) = 0$; $V_{DS} (a) = 0$.
- Measured in test circuit Fig.30.

GRAPHS FOR AMPLIFIER b



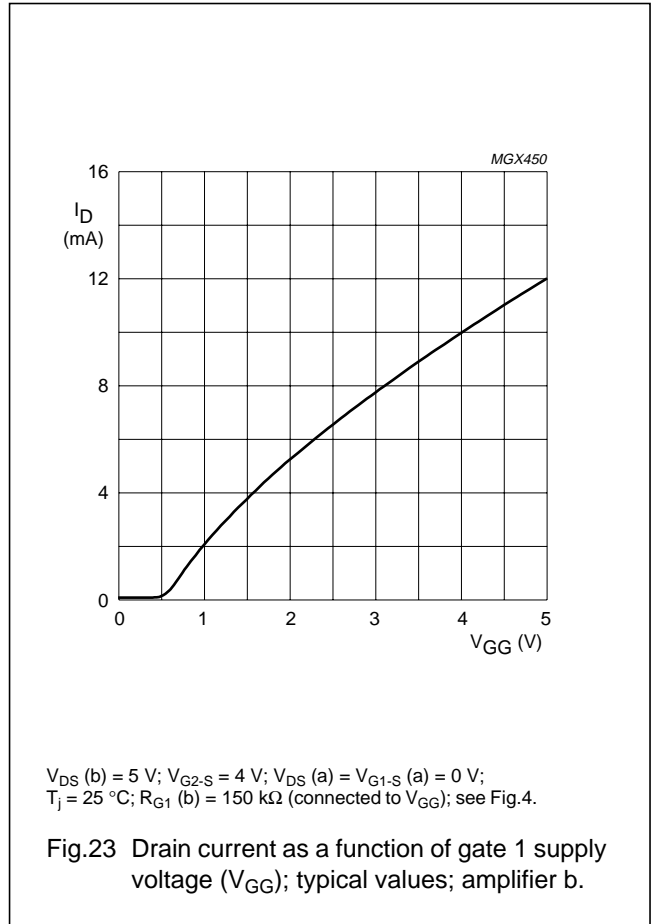
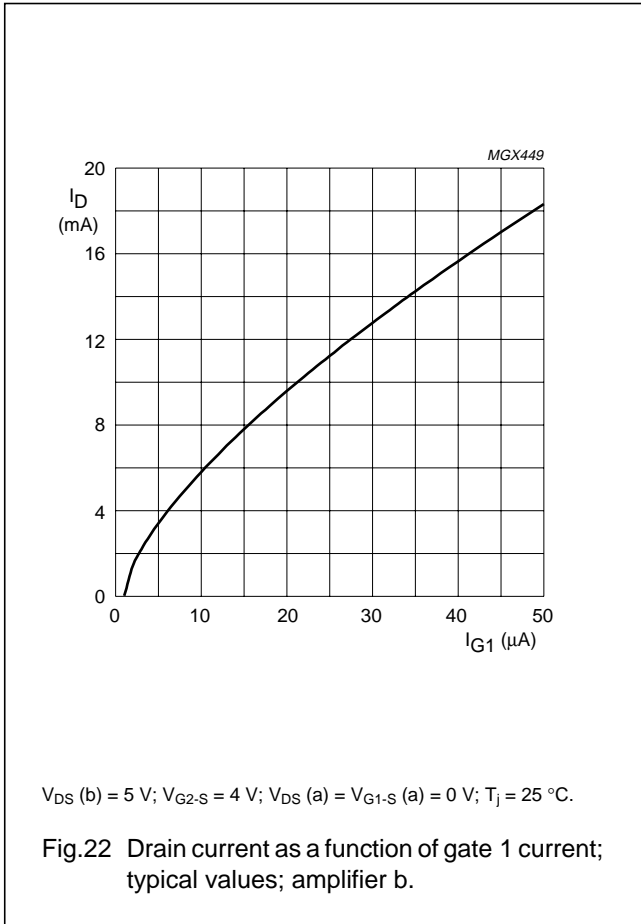
Dual N-channel dual gate MOS-FET

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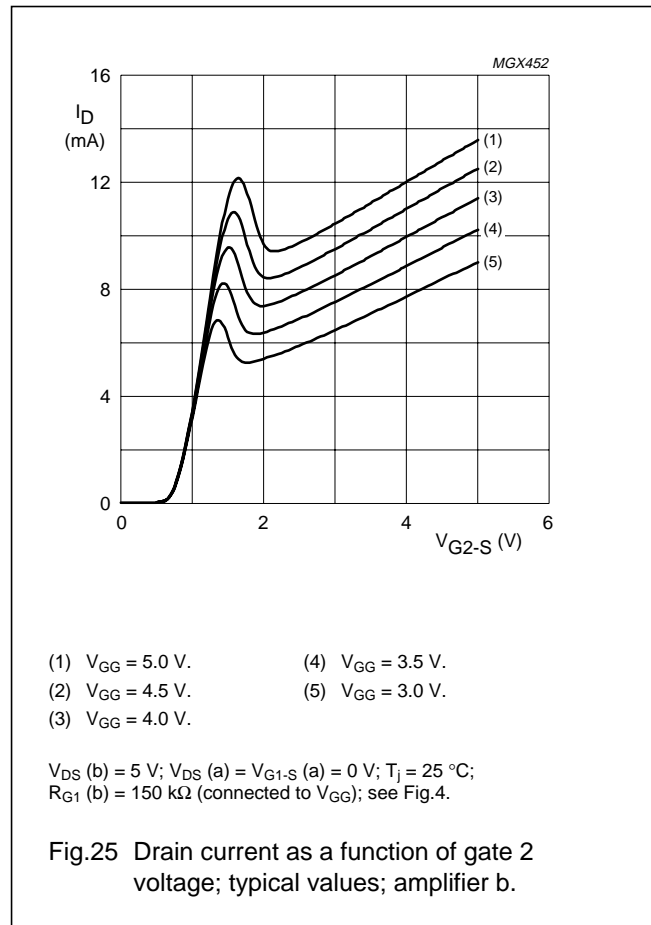
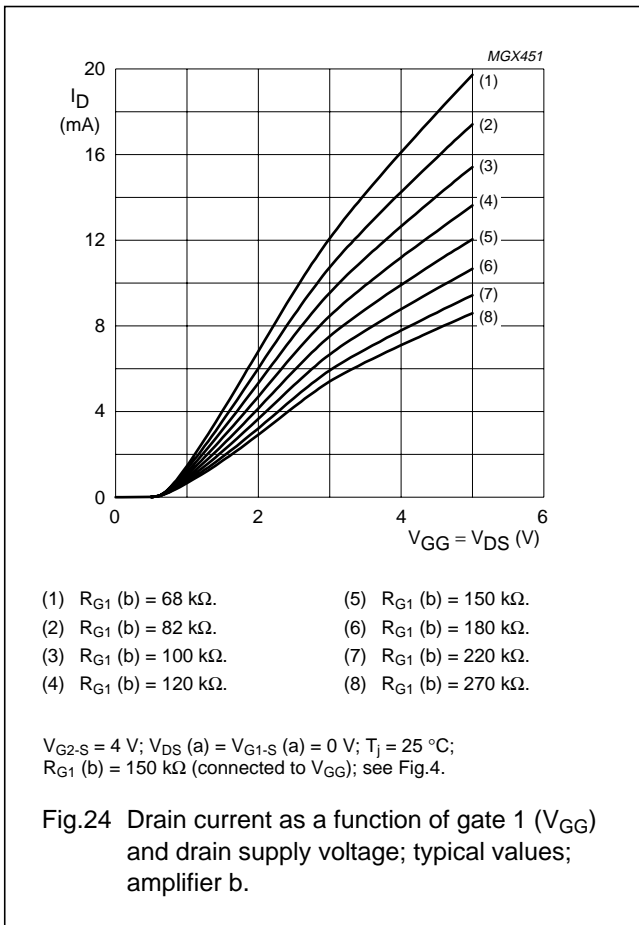
Dual N-channel dual gate MOS-FET

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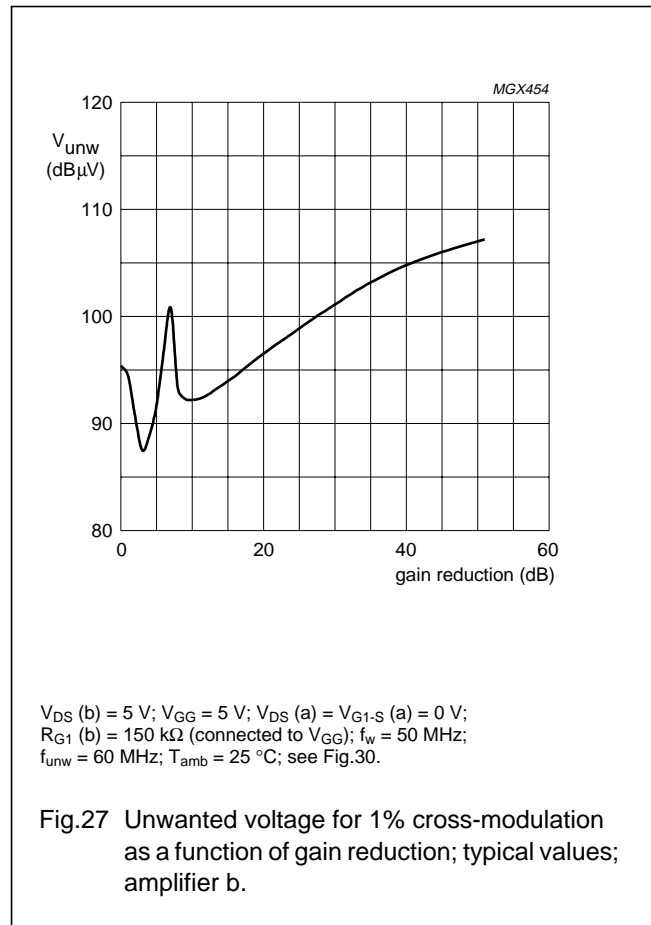
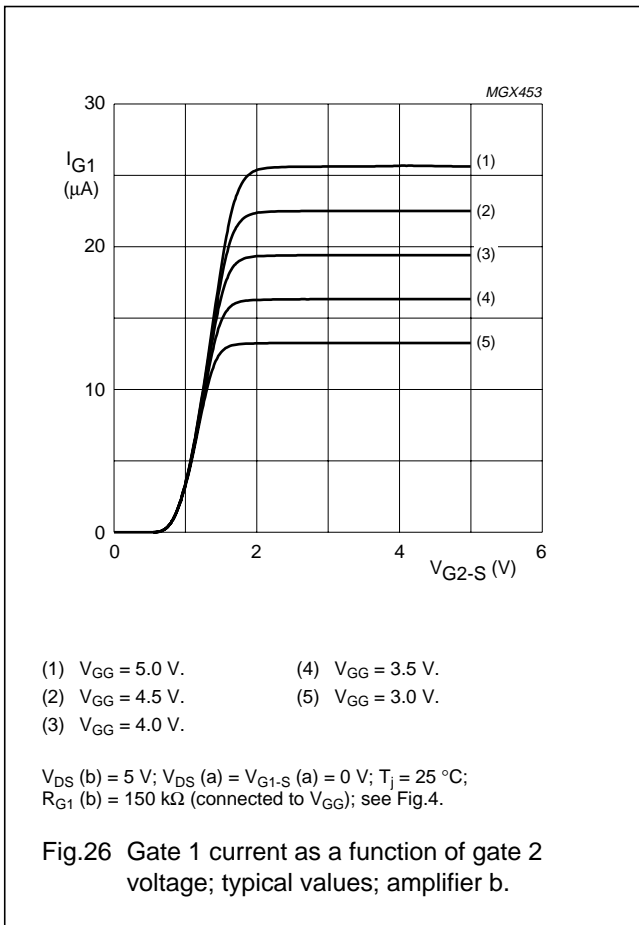
Dual N-channel dual gate MOS-FET

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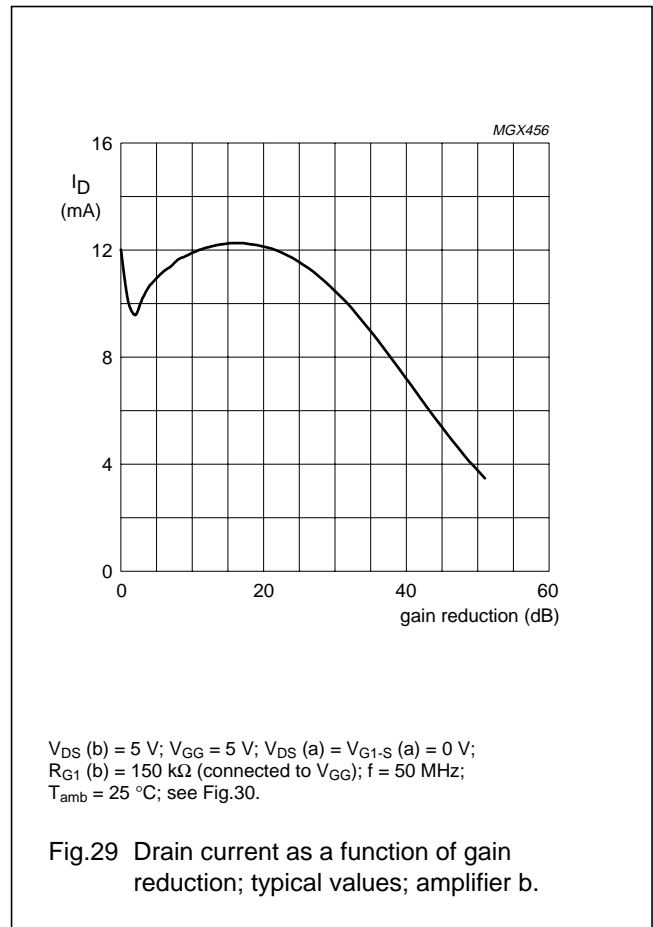
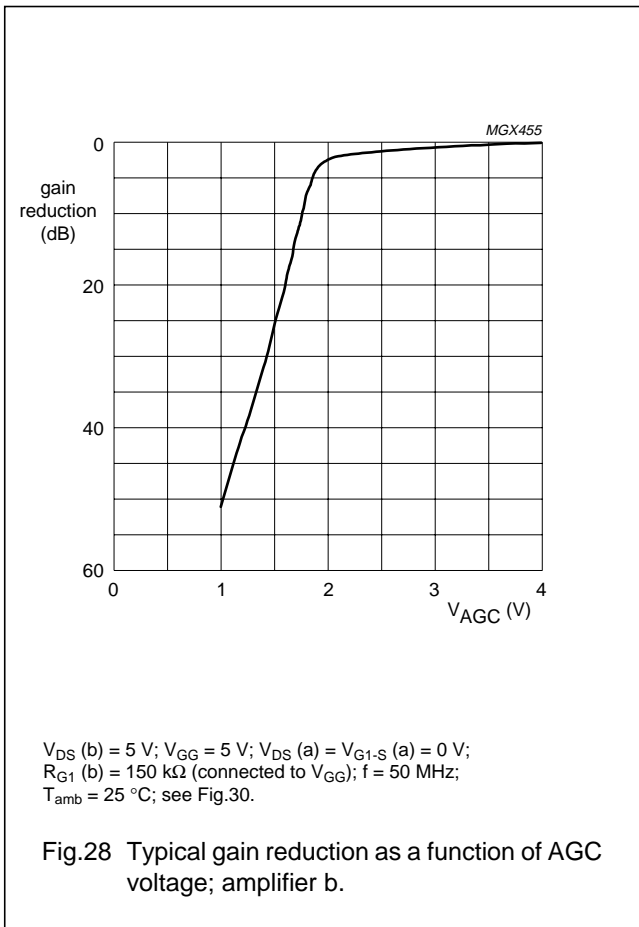
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Dual N-channel dual gate MOS-FET

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Dual N-channel dual gate MOS-FET

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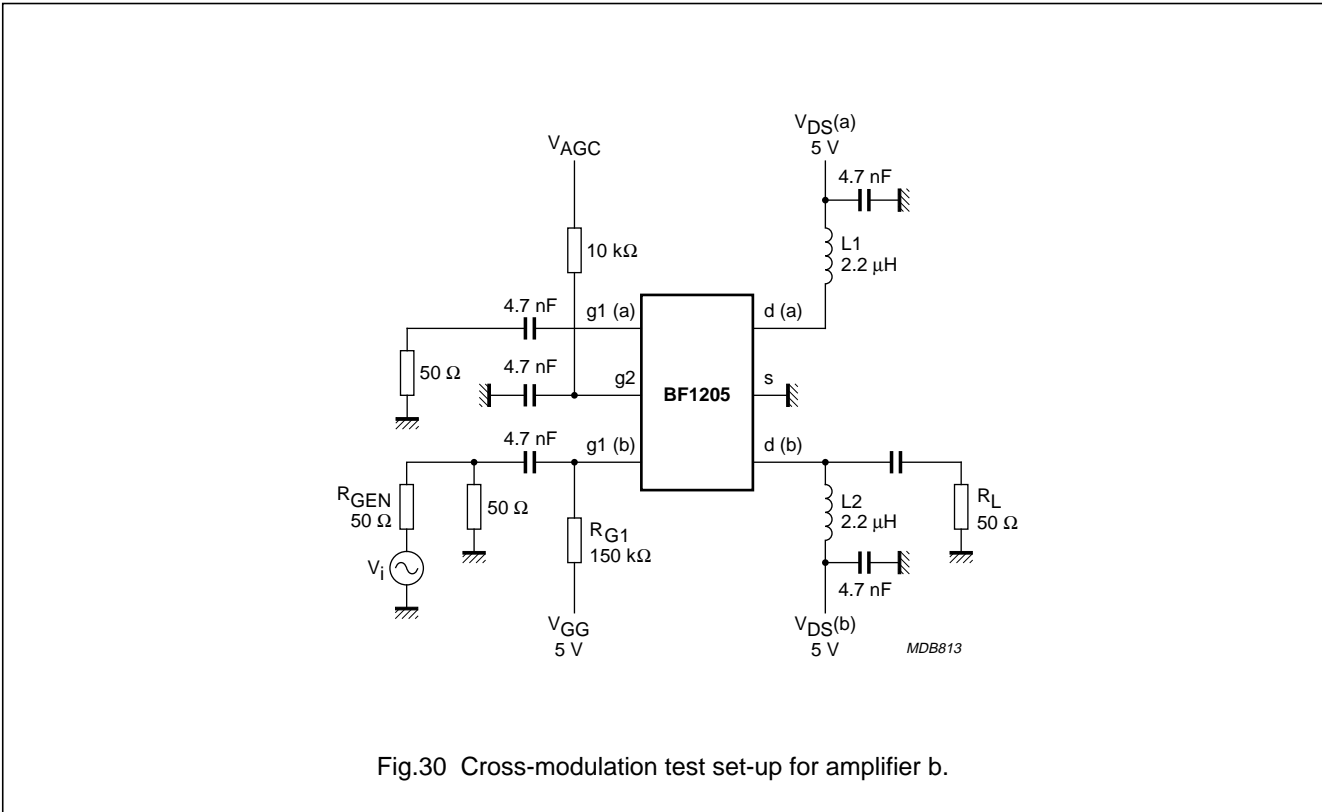
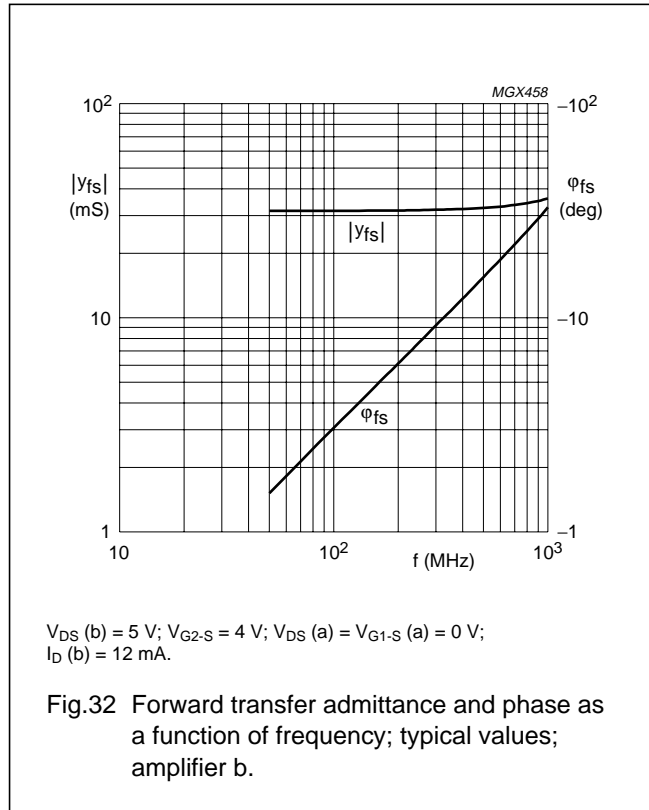
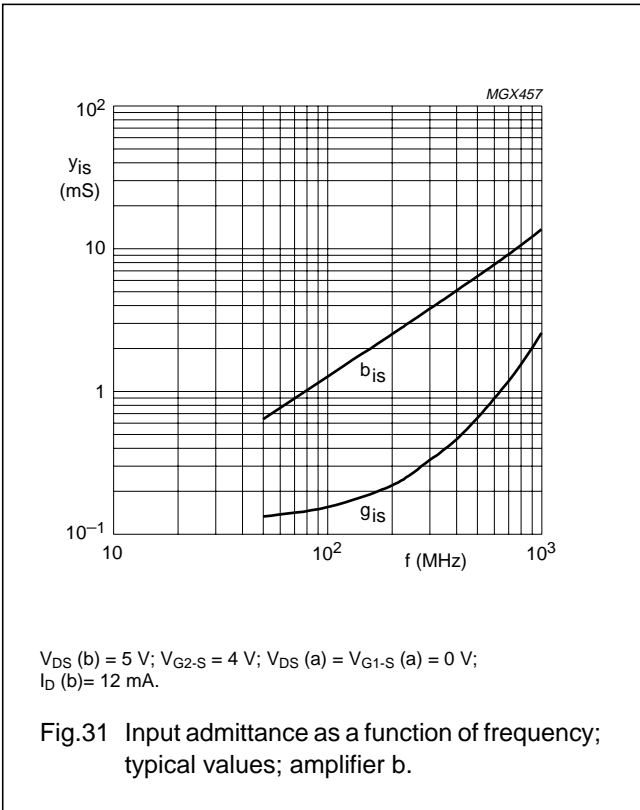
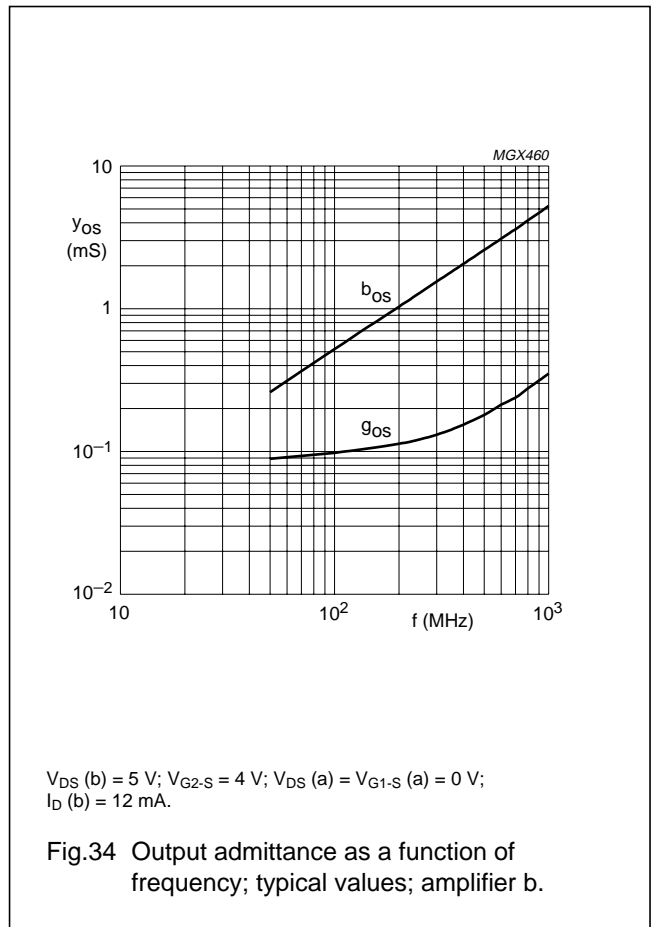
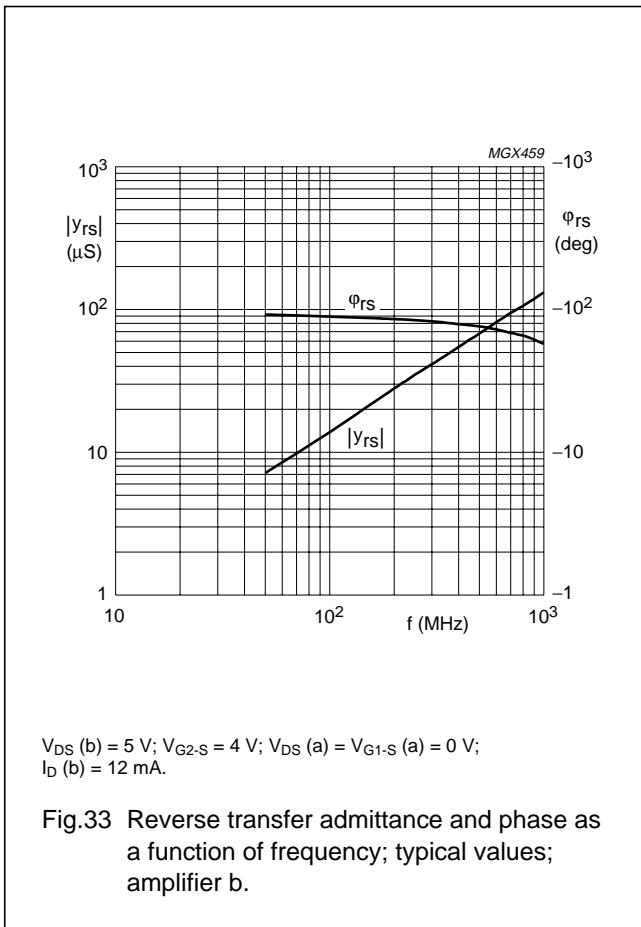


Fig.30 Cross-modulation test set-up for amplifier b.



Dual N-channel dual gate MOS-FET

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Dual N-channel dual gate MOS-FET

BF1205

Scattering parameters: amplifier b $V_{DS}(b) = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D(b) = 12\text{ mA}$; $V_{DS}(a) = 0\text{ V}$; $V_{G1-S}(a) = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.987	-3.76	3.12	175.87	0.00071	85.43	0.991	-1.56
100	0.985	-7.38	3.11	171.77	0.00136	86.06	0.989	-3.11
200	0.978	-14.63	3.09	163.72	0.00272	84.25	0.988	-6.16
300	0.968	-21.82	3.06	155.67	0.00396	82.63	0.986	-9.17
400	0.956	-28.92	3.01	147.79	0.00509	81.35	0.983	-12.17
500	0.941	-35.99	2.95	139.86	0.00616	79.46	0.973	-15.16
600	0.924	-42.93	2.89	132.06	0.00710	78.57	0.975	-18.15
700	0.905	-49.89	2.83	124.31	0.00791	77.88	0.972	-21.07
800	0.884	-56.57	2.75	116.69	0.00848	76.72	0.968	-24.08
900	0.861	-63.36	2.67	108.97	0.00900	76.55	0.964	-27.03
1000	0.837	-70.05	2.59	101.39	0.00941	76.67	0.959	-30.02

Noise data $V_{DS}(b) = 5\text{ V}$; $V_{G2-S} = 4\text{ V}$; $I_D(b) = 12\text{ mA}$; $V_{DS}(a) = 0\text{ V}$; $V_{G1-S}(a) = 0\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$

f (MHz)	F MIN (dB)	F MIN (dB)		R _n (Ω)
		(ratio)	(deg)	
400	1.3	0.662	16.76	31.55
800	1.4	0.578	33.97	30.53

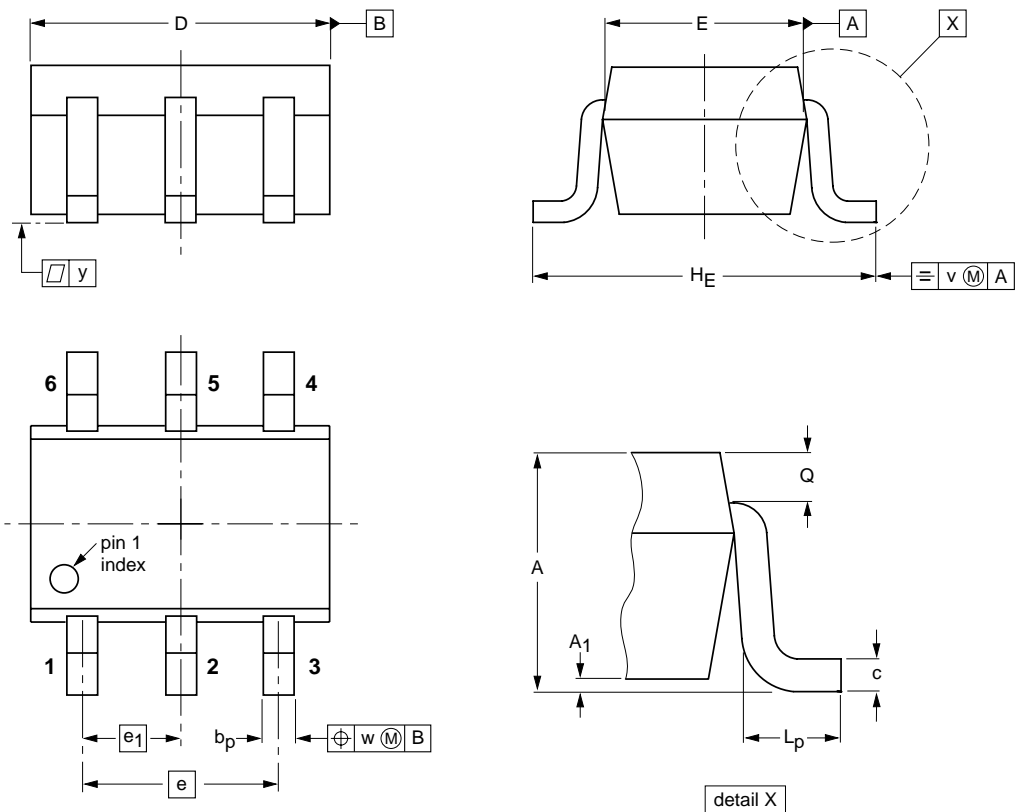
Dual N-channel dual gate MOS-FET

BF1205

PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

Dual N-channel dual gate MOS-FET

BF1205

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾⁽³⁾	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.
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Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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