

# CLC5955

## 11-bit, 55MSPS Broadband Monolithic A/D Converter

### General Description

The CLC5955 is a monolithic 11-bit, 55MSPS analog-to-digital converter. The device has been optimized for use in IF-sampled digital receivers and other applications where high resolution, high sampling rate, wide dynamic range, low power dissipation, and compact size are required. The CLC5955 features differential analog inputs, low jitter differential universal clock inputs, a low distortion track-and-hold with 0-300MHz input bandwidth, a bandgap voltage reference, data valid clock output, TTL compatible CMOS (3.3V or 2.5V) programmable output logic, and a proprietary multi-stage quantizer. The CLC5955 is fabricated on the ABIC-V 0.8 micron BiCMOS process.

The CLC5955 features a 74dBc spurious free dynamic range (SFDR) and a 64dB signal to noise ratio (SNR). The wideband track-and-hold allows sampling of IF signals to greater than 250MHz. The part produces two-tone, dithered, SFDR of 83dBFS at 75MHz input frequency. The differential analog input provides excellent common mode rejection, while the differential universal clock inputs minimize jitter. The 48-pin TSSOP package provides an extremely small footprint for applications where space is a critical consideration. The CLC5955 operates from a single +5V power supply. Operation over the industrial temperature range of -40°C to +85°C is guaranteed. National Semiconductor tests each part to verify compliance with the guaranteed specifications.

### Features

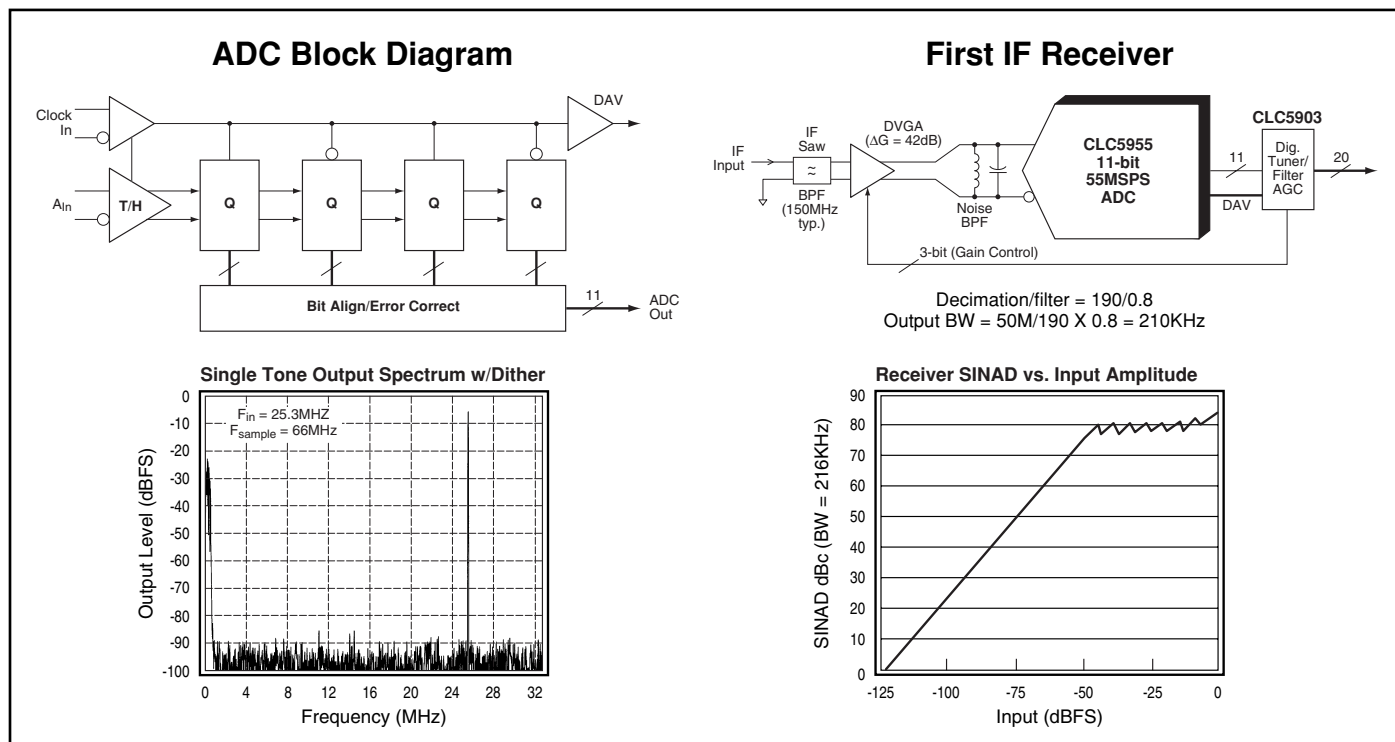
- 55MSPS
- Wide dynamic range
  - SFDR: 74dBc
  - SFDR w/dither: 85dBFS
  - SNR: 64dB
- IF sampling capability
- Input bandwidth = 0-300MHz
- Low power dissipation: 640mW
- Very small package: 48-pin TSSOP
- Single +5V supply
- Data valid clock output
- Programmable output levels:
  - 3.3V or 2.5V

### Applications

- Cellular base-stations
- Digital communications
- Infrared/CCD imaging
- IF sampling
- Electro-optics
- Instrumentation
- Medical imaging
- High definition video



Actual Size



# CLC5955 Electrical Characteristics (V<sub>cc</sub> = +5V, 55MSPS; unless specified) (T<sub>min</sub> = -40°C, T<sub>max</sub> = +85°C)

PARAMETERS	CONDITIONS	TEMP	RATINGS			UNITS	NOTES
			MIN	TYP	MAX		
							2
<b>RESOLUTION</b>		Full		11		Bits	1
<b>DIFF. INPUT VOLTAGE RANGE</b>		Full		2,048		V	
<b>MAXIMUM CONVERSION RATE</b>		Full	55	75		MSPS	1
<b>SNR</b>	f <sub>in</sub> = 25MHz, A <sub>in</sub> = -1dBFS	+25°C	60	64		dBFS	1
<b>SFDR</b>	f <sub>in</sub> = 25MHz, A <sub>in</sub> = -1dBFS	+25°C	65	74		dBc	1
<b>DYNAMIC PERFORMANCE</b>							
large-signal bandwidth	A <sub>in</sub> = -3dBFS	+25°C		300		MHz	
overvoltage recovery time	A <sub>in</sub> = 1.5FS (0.01%)	+25°C		12		ns	
effective aperture delay (Ta)		+25°C		-0.41		ns	
aperture jitter		+25°C		0.3		ps(rms)	
<b>NOISE AND DISTORTION</b>							
signal-to-noise ratio (w/o 50 harmonics)							
f <sub>in</sub> = 5.0MHz	A <sub>in</sub> = -1dBFS	Full		65		dBFS	
f <sub>in</sub> = 25MHz	A <sub>in</sub> = -1dBFS	Full	57	64		dBFS	1
f <sub>in</sub> = 75MHz	A <sub>in</sub> = -3dBFS	Full		63		dBFS	
f <sub>in</sub> = 150MHz	A <sub>in</sub> = -15dBFS	Full		64		dBFS	
f <sub>in</sub> = 250MHz	A <sub>in</sub> = -15dBFS	Full		64		dBFS	
spurious-free dynamic range							
f <sub>in</sub> = 5.0MHz	A <sub>in</sub> = -1dBFS	Full		74		dBc	
f <sub>in</sub> = 25MHz	A <sub>in</sub> = -1dBFS	Full	59	74		dBc	1
f <sub>in</sub> = 75MHz	A <sub>in</sub> = -3dBFS	Full		72		dBc	
f <sub>in</sub> = 150MHz	A <sub>in</sub> = -15dBFS	Full		69		dBc	
f <sub>in</sub> = 250MHz	A <sub>in</sub> = -15dBFS	Full		65		dBc	
intermodulation distortion							
f <sub>in1</sub> = 149.84MHz, f <sub>in2</sub> = 149.7MHz	A <sub>in</sub> = -10dBFS	+25°C		68		dBFS	
f <sub>in1</sub> = 249.86MHz, f <sub>in2</sub> = 249.69MHz	A <sub>in</sub> = -10dBFS	+25°C		58		dBFS	
dithered performance							
spurious-free dynamic range							
f <sub>in</sub> = 19MHz	A <sub>in</sub> = -6dBFS	+25°C		85		dBFS	
intermodulation distortion							
f <sub>in1</sub> = 74MHz, f <sub>in2</sub> = 75MHz	A <sub>in</sub> = -12dBFS	+25°C		83		dBFS	
<b>DC ACCURACY AND PERFORMANCE</b>							
differential non-linearity	f <sub>in</sub> = 5MHz, A <sub>in</sub> = -1dBFS	Full		±0.8		LSB	
integral non-linearity	f <sub>in</sub> = 5MHz, A <sub>in</sub> = -1dBFS	Full		±2.0		LSB	
offset error		Full	-30	0	30	mV	1
gain error		Full		1.2		%FS	
V <sub>ref</sub>		+25°C	2.2	2.37	2.6	V	1
<b>ANALOG INPUTS</b>							
analog differential input voltage range		Full		2,048		V <sub>pp</sub>	
analog input resistance (single ended)		Full		500		Ω	
analog input resistance (differential)		Full		1000		Ω	
analog input capacitance (single-ended)		Full		2		pF	
<b>ENCODE INPUTS (Universal)</b>							
V <sub>IH</sub>		+25°C			5	V	3, 4
V <sub>IL</sub>		+25°C	0			V	3, 4
differential input swing		+25°C	0.2			V	3, 4
<b>DIGITAL OUTPUTS</b>							
output voltage	logic LOW	+25°C		0.01	0.4	V	1
	logic HIGH	+25°C	3.2	3.5	3.8	V	1
	logic HIGH	+25°C	2.4	2.7	3.0	V	1
<b>POWER REQUIREMENTS</b>							
+5V supply current		Full		128	150	mA	1
Power dissipation		Full		640	750	mW	1
V <sub>CC</sub> power supply rejection ratio		+25°C		64		dB	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

# CLC5955 Electrical Characteristics ( $V_{CC} = +5V$ , 55MSPS; unless specified) ( $T_{min} = -40^{\circ}C$ , $T_{max} = +85^{\circ}C$ )

PARAMETERS	CONDITIONS	SYMB	TEMP	RATINGS			UNITS	NOTES
				MIN	TYP	MAX		
								2
<b>TIMING</b> ( $C_L = 7pF$ DATA; $10pF$ DAV)								
max conversion rate (ENCODE)			Full	55	75		MSPS	1
min conversion rate (ENCODE)			+25°C		10		MSPS	
pulse width high (ENCODE)	50% threshold	$t_p$	Full	9.1			ns	3
pulse width low (ENCODE)	50% threshold	$t_M$	Full	9.1			ns	3
ENCODE falling edge to DATA not valid		$t_{DNV}$	Full	8.3			ns	3
ENCODE falling edge to DATA guaranteed valid		$t_{DGV}$	Full			17.8	ns	3
rising ENCODE to rising DAV delay	50% threshold	$t_{DAV}$	Full	8.3		12.6	ns	3
DATA setup time before rising DAV		$t_S$	Full	$t_M - 2.4$			ns	3
DATA hold time after rising DAV		$t_H$	Full	$t_p - 1.6$			ns	3
pipeline latency			Full			3.0	clk cycle	

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

## Notes

- 1) These parameters guaranteed by test.
- 2) Typical specifications are based on the mean test values of deliverable converters from the first three diffusion lots.
- 3) Values guaranteed based on characterization and simulation.
- 4) See page 8, Figure 3 for ENCODE Inputs circuit.

## Absolute Maximum Ratings

positive supply voltage ( $V_{CC}$ )	-0.5V to +6V
differential voltage between any two grounds	<100mV
analog input voltage range	GND to $V_{CC}$
digital input voltage range	-0.5V to + $V_{CC}$
output short circuit duration (one-pin to ground)	infinite
junction temperature	175°C
storage temperature range	-65°C to 150°C
lead solder duration (+300°C)	10sec
ESD tolerance	
human body model	2000V
machine model	200V

Note: Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure to maximum ratings for extended periods may affect device reliability.

## Recommended Operating Conditions

positive supply voltage ( $V_{CC}$ )	+5V ±5%
analog input voltage range	2.048V <sub>pp</sub> diff.
operating temperature range	-40°C to +85°C

## Package Thermal Resistance

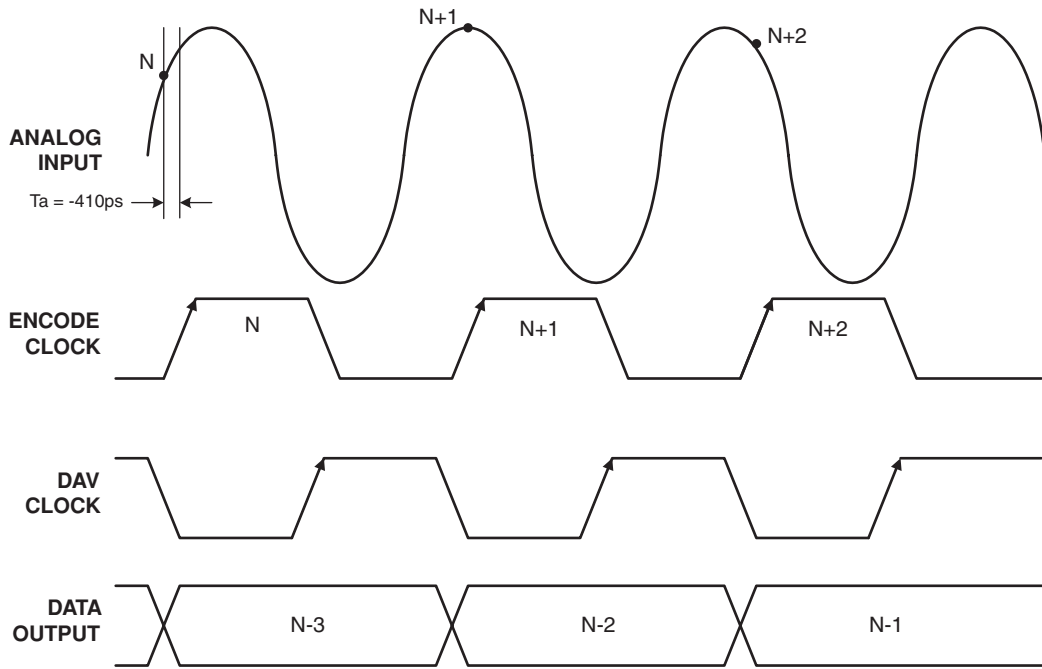
Package	$\theta_{JA}$	$\theta_{JC}$
48-pin TSSOP	56°C/W	16°C/W

## Reliability Information

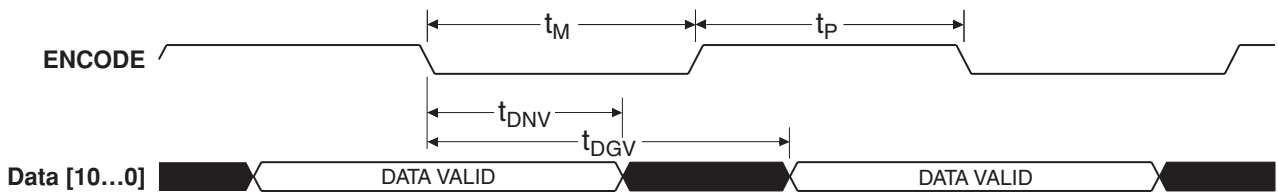
Transistor count	5000
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## Ordering Information

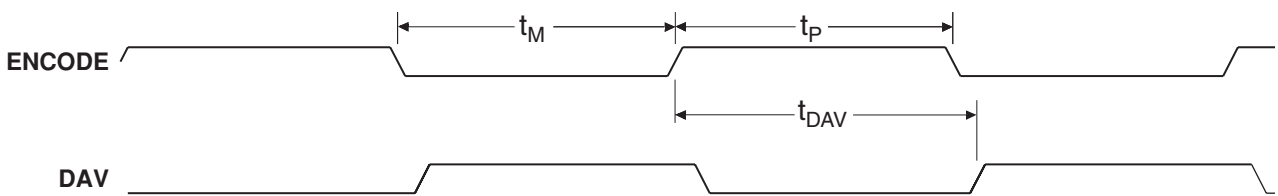
Model	Temperature Range	Description
CLC5955MTDX	-40°C to +85°C	48-pin TSSOP (TNR 1000 pc reel)



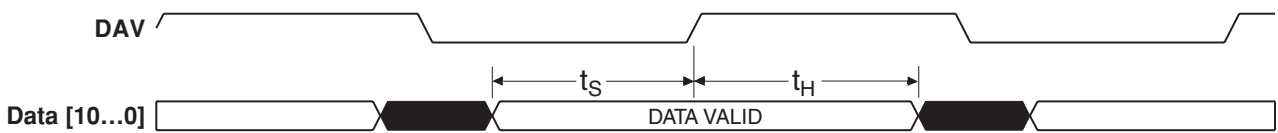
**CLC5955 Aperture Delay Diagram**



**CLC5955 ENCODE to Data Timing Diagram**

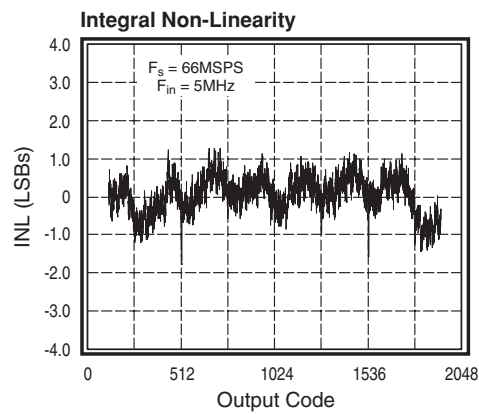
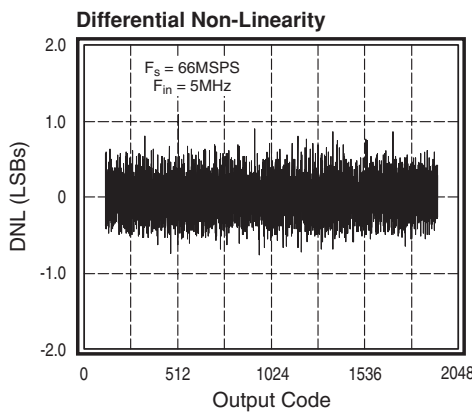
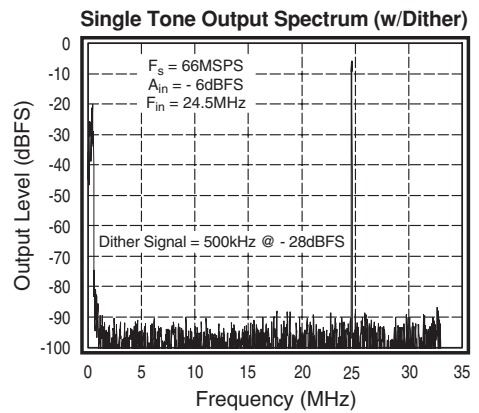
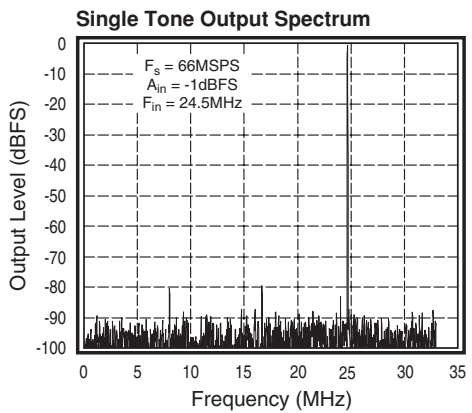
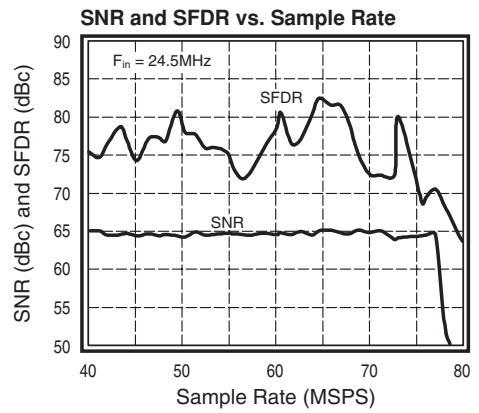
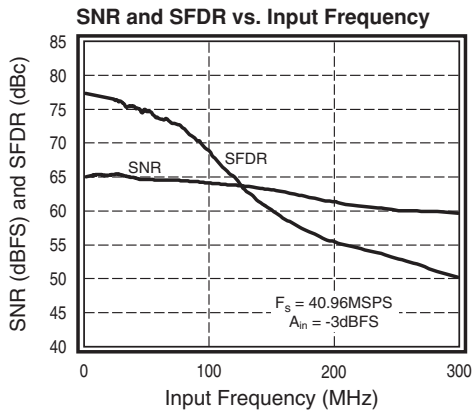
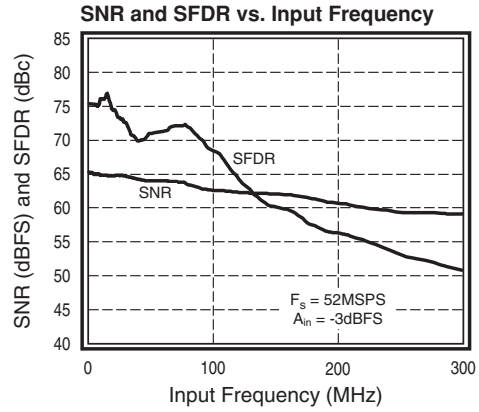
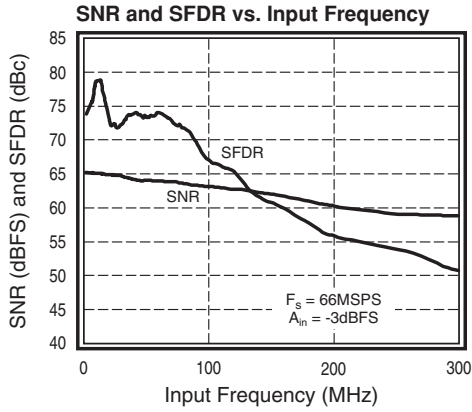


**CLC5955 ENCODE to DAV Timing Diagram**

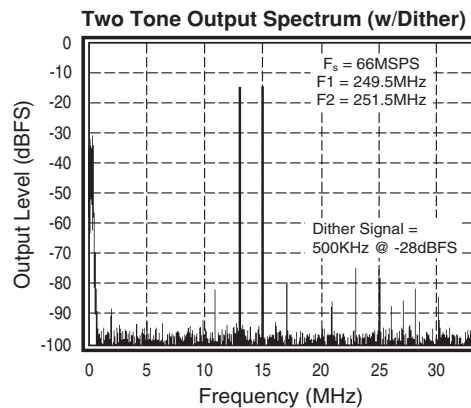
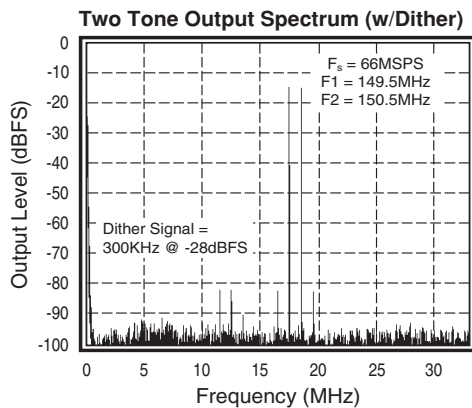
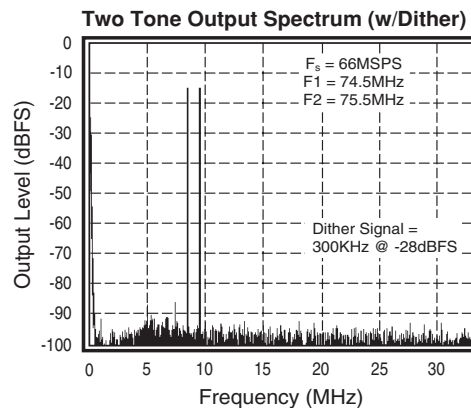
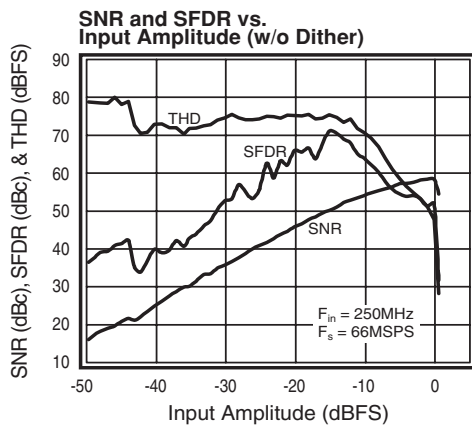
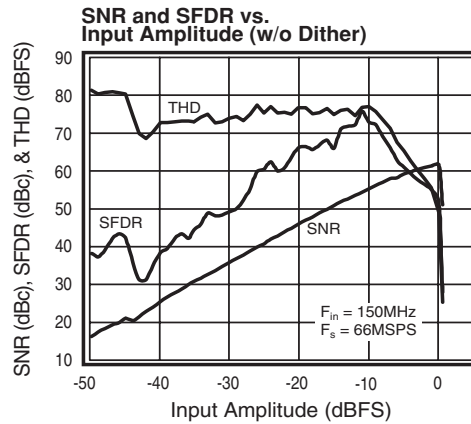
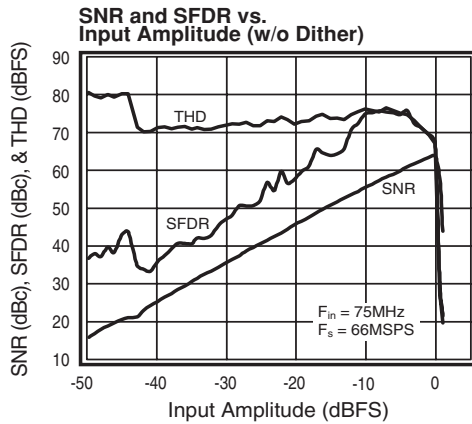
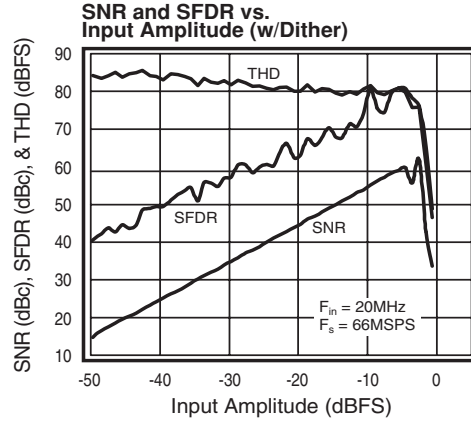
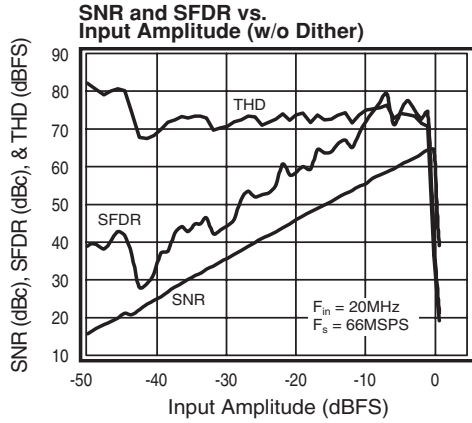


**CLC5955 DAV to Data Timing Diagram**

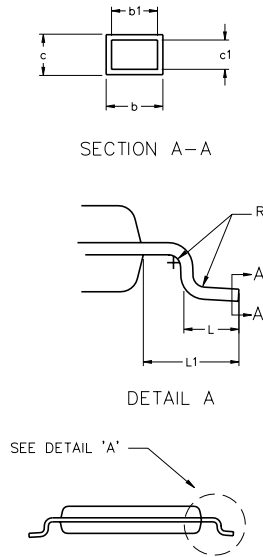
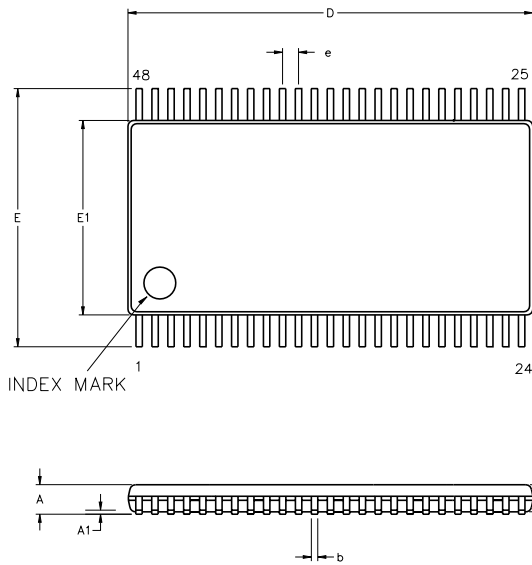
# CLC5955 Typical Performance Characteristics ( $V_{CC} = +5V$ )



# CLC5955 Typical Performance Characteristics ( $V_{CC} = +5V$ )



# Physical Dimensions

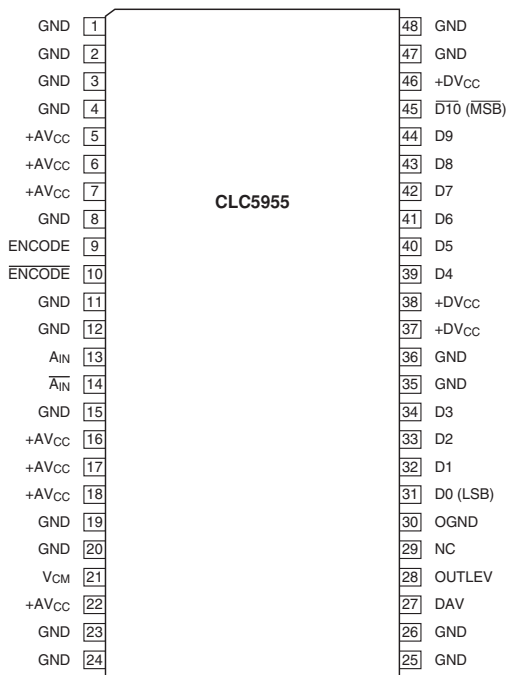


Symbol	Min	Max	Notes
A	—	1.10	
A1	0.05	0.15	
A2	0.80	1.05	
b	0.17	0.27	
b1	0.17	0.23	
c	0.09	0.20	
c1	0.09	0.16	
D	12.40	12.60	2
E	8.1 BSC		
E1	6.00	6.20	2
e	0.50 BSC		
L	0.50	0.75	
L1	1.00 REF		
R1	0.127		

**Notes:**

- All dimensions are in millimeters.
- Dimensions D and E1 do not include mold protrusion. Allowable protrusion is 0.20mm per side.

# CLC5955 Pin Definitions



**$A_{IN}, \overline{A_{IN}}$**

(Pins 13, 14) Differential input with a common mode voltage of +2.4V. The ADC full scale input is  $1.024V_{pp}$  on each of the complimentary input signals.

**ENCODE, ENCODE**

(Pins 9, 10) Differential clock where ENCODE initiates a new data conversion cycle on each rising edge. Logic for these inputs are 50% duty cycle universal differential signal (>200mV). The clock input is internally biased to  $V_{CC}/2$  with a termination impedance of 2.5k $\Omega$ .

**D0-D10**

(Pins 31-34, 39-45) Digital data outputs are CMOS and TTL compatible. D0 is the LSB and D10 is the MSB. MSB is inverted. Output coding is two's complement. Current limited to source/sink 2.5mA typical.

**DAV**

(Pin 27) Data Valid Clock. Data is valid on rising edge. Current limited to source/sink 5mA typical.

**OUTLEV**

(Pin 28) Output Logic 3.3V or 2.5V option. Open = 3.3V, GND = 2.5V.

**$V_{CM}$**

(Pin 21) Internal common mode voltage reference. Nominally +2.4V. Can be used for the input common mode voltage. This voltage is derived from an internal bandgap reference.  $V_{CM}$  should be buffered when driving any external load. Failure to buffer this signal can cause errors in the internal bias currents.

**GND**

(Pins 1-4, 8, 11, 12, 15, 19, 20, 23-26, 35, 36, 47, 48) circuit ground.

**+AV<sub>CC</sub>**

(Pins 5-7, 16-18, 22,) +5V power supply for the analog section. Bypass to ground with a 0.1 $\mu$ F capacitor.

**+DV<sub>CC</sub>**

(Pins 37, 38, 46) +5V power supply for the digital section. Bypass to ground with a 0.1 $\mu$ F capacitor.

**NC**

(Pin 29) No connect. May be left open or grounded.

**OGND**

(Pin 30) Option ground. May be tied to GND or left floating.

# CLC5955 Applications

## Analog Inputs and Bias

Figure 1 depicts the analog input and bias scheme. Each of the differential analog inputs are internally biased to a nominal voltage of 2.40 volts DC through a 500Ω resistor to a low impedance buffer. This enables a simple interface to a broadband RF transformer with a center-tapped output winding that is decoupled to the analog ground. If the application requires the inputs to be DC coupled, the  $V_{cm}$  output can be used to establish the proper common-mode input voltage for the ADC. The  $V_{cm}$  voltage reference is generated from an internal bandgap source that is very accurate and stable.

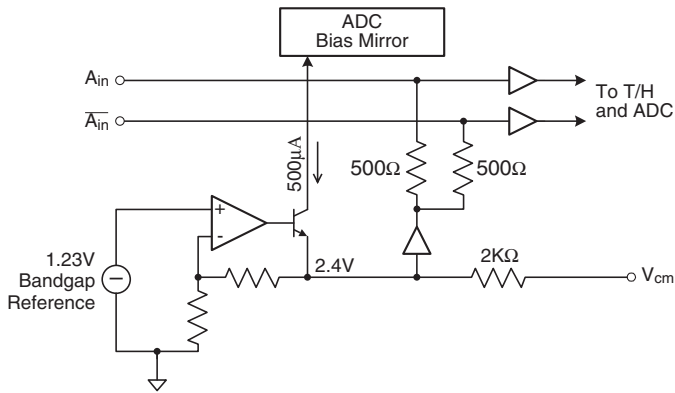


Figure 1: CLC5955 Bias Scheme

The  $V_{cm}$  output may also be used to power down the ADC. When the  $V_{cm}$  pin is pulled above 3.5V, the internal bias mirror is disabled and the total current is reduced to less than 10mA. Figure 2 depicts how this function can be used. The diode is necessary to prevent the logic gate from altering the ADC bias value.

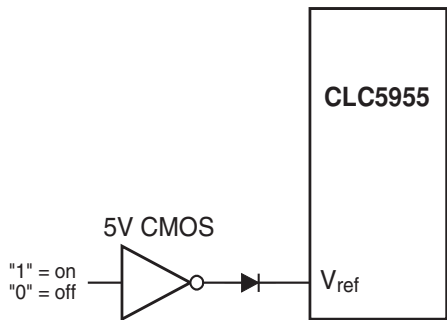


Figure 2: Power Shutdown Scheme

## ENCODE Clock Inputs

The CLC5955's differential input clock scheme is compatible with all commonly used clock sources. Although small differential and single-ended signals are adequate, for best aperture jitter performance a low noise differential clock with a high slew rate is preferred. As depicted in Figure 3, both ENCODE clock inputs are internally biased to  $V_{CC}/2$  through a pair of 5KΩ resistors. The clock input buffer operates with any common-mode voltage between the supply and ground.

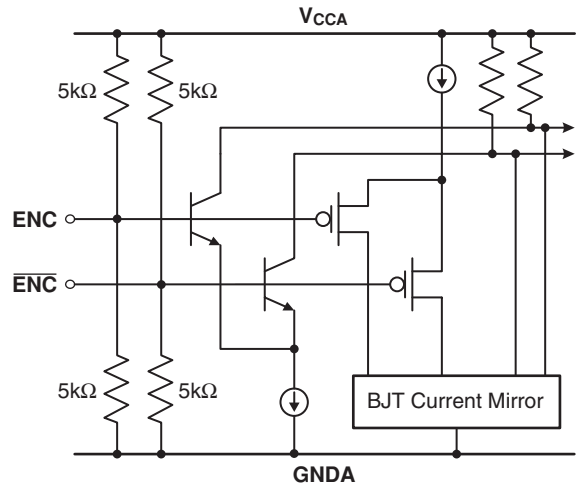


Figure 3: CLC5955 ENCODE Clock Inputs

The internal bias resistors simplify the clock interface to another center-tapped transformer as depicted in Figure 4. A low phase noise, RF synthesizer of moderate amplitude (1 - 4V<sub>pp</sub>) can drive the ADC through this interface.

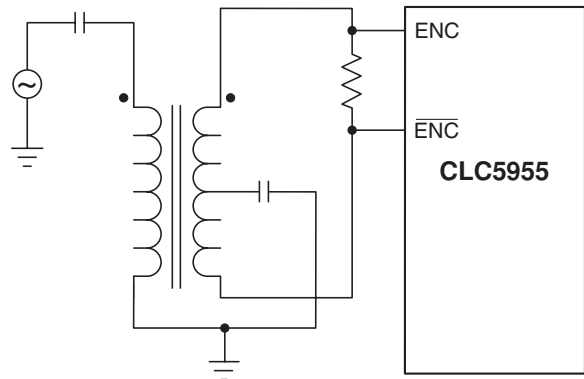


Figure 4: Transformer Coupled Clock Scheme



Figure 5 shows the clock interface scheme for square wave clock sources.

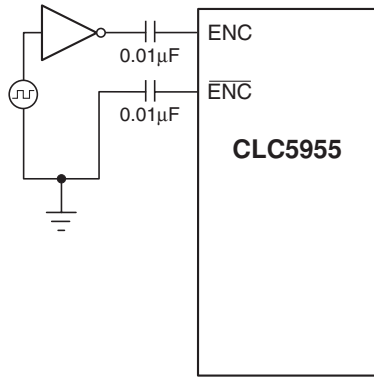


Figure 5: TTL, 3V or 5V CMOS Clock Scheme

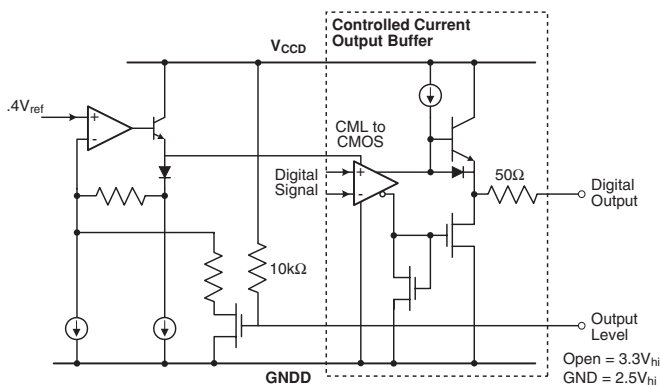


Figure 6: CLC5955 Digital Outputs

### Digital Outputs and Level Select

Figure 6 depicts the digital output buffer and bias used in the CLC5955. Although each of the eleven output bits uses a controlled current buffer to limit supply transients, it is recommended that parasitic loading of the outputs is minimized. Because these output transients are harmonically related to the analog input signal, excessive loading will degrade ADC performance at some frequencies.

The logic high level is slaved to the internal 2.4 voltage reference. The OUTLEV control pin selects either a 3.3V or 2.5V logic high level. An internal pullup resistor selects the 3.3 volt level as the default when the OUTLEV pin is left open. Grounding the OUTLEV pin selects the 2.5V logic high level.

To ease user interface to subsequent digital circuitry, the CLC5955 has a data valid clock output (DAV). In order to match delays over IC processing variables, this digital output also uses the same output buffer as the data bits. The DAV clock output is simply a delayed version of the ENCODE input clock. Since the ADC output data change is slaved to the falling edge of the ENCODE clock, the rising DAV clock edge occurs near the center of the data valid window (or eye) regardless of the sampling frequency.

### Minimum Conversion Rate

This ADC is optimized for high-speed operation. The internal bipolar track and hold circuits will cause droop errors at low sample rates. The point at which these errors cause a degradation of performance is listed on the specifications page as the minimum conversion rate. If a lower sample rate is desired, the ADC should be clocked at a higher rate, and the output data should be decimated. For example, to obtain a 10MSPS output, the ADC should be clocked at 20MHz, and every other output sample should be used. No significant power savings occurs at lower sample rates, since most of the power is used in analog circuits rather than digital circuits.

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**National Semiconductor Corporation**

Tel: 1(800) 272-9959  
Fax: 1(800) 737-7018  
E-mail: [support@nsc.com](mailto:support@nsc.com)  
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**National Semiconductor Europe**

Fax: +49 (0) 1 80-530 85 86  
E-mail: [europe.support@nsc.com](mailto:europe.support@nsc.com)  
Deutsch Tel: +49 (0) 1 69 9508 6208  
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