an Intel company

2.5 Gbit/s 4:1 Multiplexer GD16553

Preliminary

General Information

The GD16553 is a high performance 2.5 Gbit/s 4:1 Multiplexer with on-chip PLL and high-current laser driver designed for use in ITU-T STM16 or SONET OC-48 fiber optic communication systems.

The GD16553 multiplexes four 622.08 Mbit/s data streams into a single 2.488 Gbit/s data stream output using an external master clock at 38.8 MHz or 77.6 MHz.

Optionally the MUX may be bypassed allowing direct 2.5 Gbit/s input to the laser driver.

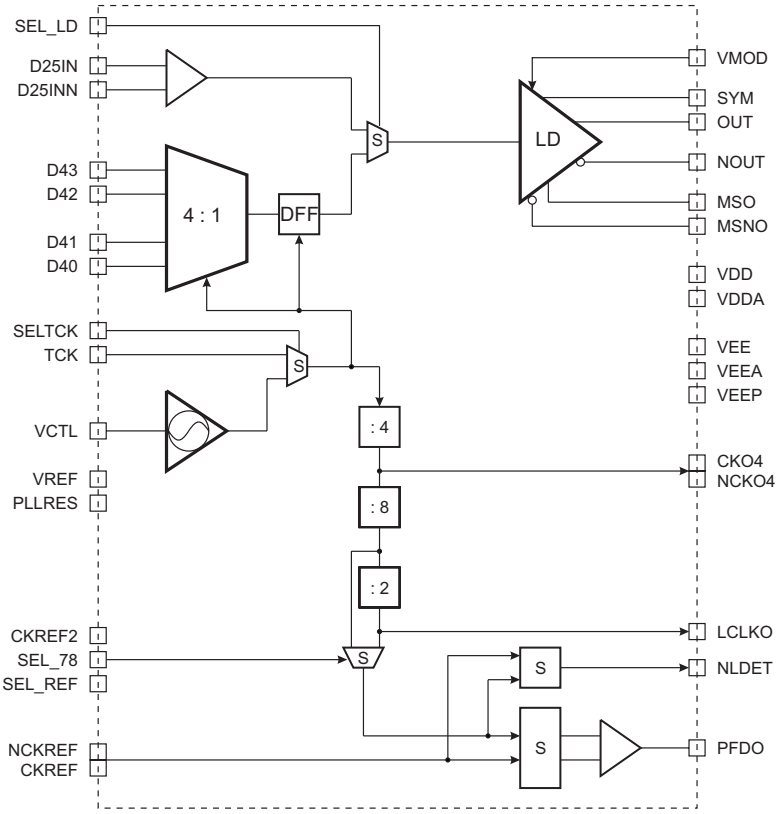
Internal clock synchronisation is provided by an on-chip PLL circuit requiring a simple passive external loop filter only. The PLL circuit features an NLDET pin output for simple implementation of a lock detect function, as shown overleaf.

The multiplexed data stream is output by a high modulation-current laser driver with a modulation-current sink capability of up to 60 mA (typ.)

The mark/space ratio of the output can be monitored as a dc voltage between the two pins MSO and MSNO, provided a decoupling capacitor is connected between the pins. The mark/space ratio can be controlled by SYM pin.

GD16553 requires a single -5 V supply only.

The device is available housed in a 48 pin JEDEC standard Thin Quad Flat Pack (TQFP-48L-EDQUAD) plastic high-speed package.



Features

- Complies with ITU-T STM-16 and SONET OC-48 standards.
- On-chip PLL ensures precise retiming of high-speed data controlled by external low frequency reference.
- On-chip LC type VCO ensures a low jitter generation of 4 mUI_{RMS} (typ.).
- PLL lock detect output.
- On-chip high modulation current laser driver (5 - 60 mA typ.).
- Output signal mark/space adjustment.
- Mark/space monitor.
- Single supply operation.
- ECL compatible data and clock inputs.
- Power dissipation: 0.95 W (typ.).
- Available in a 48 Pin JEDEC TQFP-48L-EDQUAD package

Applications

- Tele Communications systems:
  - SDH STM-16
  - SONET OC-48
- Data Communications

Functional Details

The GD16553 consists of three major functional parts:

- a 4:1 MUX unit
- a PLL system with on-chip VCO
- a Laser Driver.

The function of the MUX is to multiplex the 4-bit word D40-3 into a 4-bit serial data stream. The order of bits in the multiplexed bit stream is D40 as the first coming bit followed by D41, D42, and D43.

The multiplexed bit stream is retimed by the PLL system, buffered and converted to an output current in the laser driver in order to interface to a 25 Ω/50 Ω laser diode (or similar load). Data HI corresponds to output current in pin OUT On and output current in pin NOUT Off. The outputs OUT and NOUT are complementary outputs with the same electrical characteristics.

The internal VCO is locked to the frequency of the external reference (CKREF) selectable at either 38.8 MHz or 77.6 MHz by using the on-chip PLL.

The PLL system consists of:

- a Phase Frequency Detector
- a charge pump
- a low-jitter LC type VCO running at approximately 2.5 GHz.

The 4:1 MUX can be bypassed by setting the SEL_LD input low, thus selecting the 2.5 Gbit/s ECL inputs (D25IN / D25INN).

Application Details

PLL Loop Filter

For the PLL in the GD16553, GIGA recommends to use a loop filter composed, as shown in Figure 1 below. This simple low pass filter has been found suitable for keeping jitter performance within the specifications. GD16553 loop filter component values should be optimized for the specific application of GD16553.

Resistor (R1) connected between the pins PFDO and VCTL, is charge resistor for the capacitor C1 and furthermore helps to linearise the current source in the charge pump.

Resistor (R2) and capacitor (C1) complete the loop filter. The optimum component values with regard to jitter generation are affected by the reference clock phase-noise content.

In order to obtain best noise and jitter performance it is imperative that C1 is connected to VDDA in close proximity of the VCTL pin.

Lock Detect Circuit

A simple PLL lock detect function can be implemented by 3 external components, comprising a low-pass filter (R3 and C3) followed by a Schmitt trigger (ST1), as shown in Figure 1 below. Indicative values of 1 kΩ/100 nF for R3/C3 may be used.

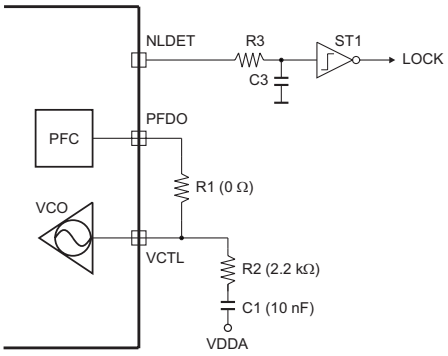


Figure 1. *PLL Loop Filter*

AC Coupled Output

When DC coupled the output swing will be limited by OUT output voltage specified to -2 V. For maximum output voltage swing the output should be AC coupled.

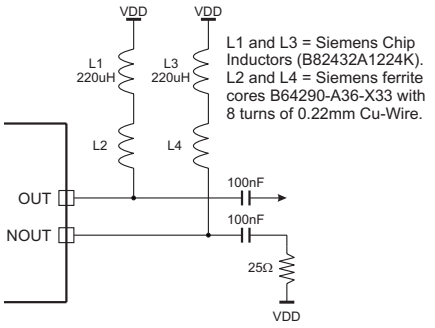


Figure 2. *AC Coupled Output*

Laser Driver Current Control

The output modulation current is controlled by the pin VMOD and can be controlled in the range from 5 mA to 60 mA.

The output voltage swing across the external load may be varied accordingly. The modulation current control on pin VMOD is implemented as a current mirror and therefore sinks a current proportional to the modulation current. The current sink into the VMOD pin is approximately 3/80 of the modulation current.

By using an external general-purpose operational amplifier the laser current may be controlled accurately and independently of environmental changes with a feed-back network as shown in Figure 3 below.

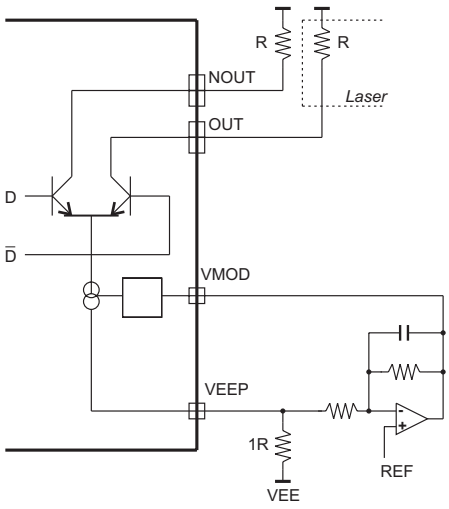


Figure 3. *Laser Drive Output*

The op-amp must be able to drive the VMOD pin input in the range VEE to VDD.

The Outputs / Inputs

The mark/space ratio of the output may be monitored as the DC signal between the MSO and MSNO pins. These outputs may be connected as shown in Figure 4 below.

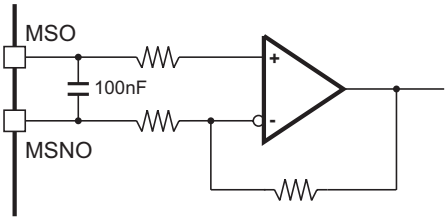


Figure 4. *External connection for MSO/MSNO*

The pulse width of the output signals OUT and NOUT from the laser driver can be adjusted by the SYM input. If the SYM is input left unused (open), the driver will automatically set the output waveform to symmetrical pulses. When left unconnected, the SYM terminal will have a voltage of approximately -2.5 V.

Inceasing the SYM voltage towards VDD will increase the pulse width of the OUT signal and decrease NOUT correspondingly as indicated in Figure 5. Reducing the SYM voltage will affect the output pulse width in the opposite direction.

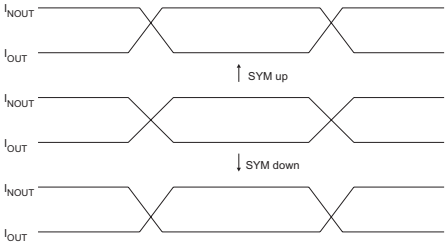


Figure 5. *Adjustment of SYM input*

Practical Considerations

The thermal pad under the package must be connected to VDD for optimum performance.

Loop filter capacitor must be connected to VDDA using shortest possible connection.

The laser driver output signals OUT and NOUT are duplicated on the package in order to accommodate high output currents and good match to transmission lines in the PCB. The duplicated output pins are connected in parallel inside the device. Both OUT (or NOUT) pins can be shortcircuited together and jointly connected to a transmission line conductor on the PCB.

Both the output connected to the laser as well as the complementary output connected to the balancing termination resistor should be deigned as transmission lines matching the impedance of the laser. Source termination of the transmission line driving the laser may be necessary to prevent oscillations, depending on the termination characteristics of the laser itself. If source termination is used, it should be placed as close as possible to the output pins of the package, and attention must be paid to avoid any ‘branches’ leading to RF stub effects.

General Hints

In order to obtain optimum performance at bit-rates in the gigabit range, it is imperative to keep signal traces designed as transmission lines, properly terminated. Smooth curvature should be used and sharp corners avoided. Signal leads should be kept shortest possible, and all power supply pins decoupled individually in close proximity to the device package.

Positive Supply Operation

If the device is driven from a positive power supply with VEE connected to the system 0V reference, a local VDD supply ’plane’ should be laid out for connection to the heat sink slug of the package, and to the supply pins. The VDD supply plane must then be decoupled at multiple points to the system signal reference plane.

Pin List

Mnemonic:	Pin No.:	Pin Type:	Description:
D40, D41 D42, D43	41, 40 39, 38	ECL IN	Single-ended data Inputs (622.08 Mbit/s). The order of bits in the multiplexed bit stream is D40 as the first coming bit, then D41, D42, and D43.
VREF	36	ANL I/O	ECL reference Input/Output
CKREF NCKREF	6 7	ECL IN ECL IN	Differential Clock Inputs. Selectable 38.8 MHz or 77.6 MHz. NCKREF internally biased at the ECL reference. This may be externally overridden.
SEL_78	1	ECL IN	Reference Clock Input Frequency select pin (“0" = 38.8 MHz, ”1" = 77.6 MHz).
PLLRES	42	ECL IN	PLL Reset Input (test only). Connect to VEE.
VMOD	26	ANL IN	Laser current control input. VMOD controls modulation current from 5 to 60 mA.
SYM	25	ANL IN	Laser Driver symmetry control
VCTL	4	ANL IN	VCO control-voltage Input.
TCK	48	ECL IN	Low frequency test clock. For test only. Leave open.
SELTCK	47	ECL IN	Test select input. For normal operation connect to VEE.
SEL_LD	33	ECL IN	Data select between D40..43 and inputs D25IN(N).
D25IN, D25INN	32, 31	ECL IN	Direct 2.488 Gbits input to laser driver
CKREF2	NC	ECL IN	Bonding option. Reference clock input with divide by two.
SEL_REF	NC	ECL IN	Bonding option. Select signal to select between optional reference input CKREF2 and CKREF. For normal operation bonded into cavity.
OUT NOUT	22, 23 19, 20	OPEN COLLECTOR OPEN COLLECTOR	Laser Driver Output (2.488 Gbit/s). Inverted Laser Driver Output (2.488 Gbit/s).
CKO4 NCKO4	14 15	ECL OUT ECL OUT	Clock Output (622.08 MHz). Inverted Clock Output (622.08 MHz).
LCLKO	13	ECL OUT	Clock output (38 MHz).
NLDET	10	ANL OUT	Inverted Lock-Detect Output.
MSO, MSNO	30, 29	ANL OUT	Mark/Space monitor output.
PFDO	8	ANL OUT	Phase/Frequency Detector Output,
VDD	17, 21, 24, 27, 34, 44	PWR	Ground pins. Supplies digital circuit of GD16553.
VDDA	2, 3, 11, 46, 16	PWR	Ground pins. Supplies PLL and laser circuits.
VEE	35, 37, 43	PWR	Negative supply pins. Supplies digital part of GD16553.
VEEA	5, 9, 12, 45	PWR	Negative supply pins. Supplies PLL circuit.
VEEP	18, 28	PWR	Negative supply pins. Supplies laser driver output.
Heat sink			Connected to VDD.

Package Pinout

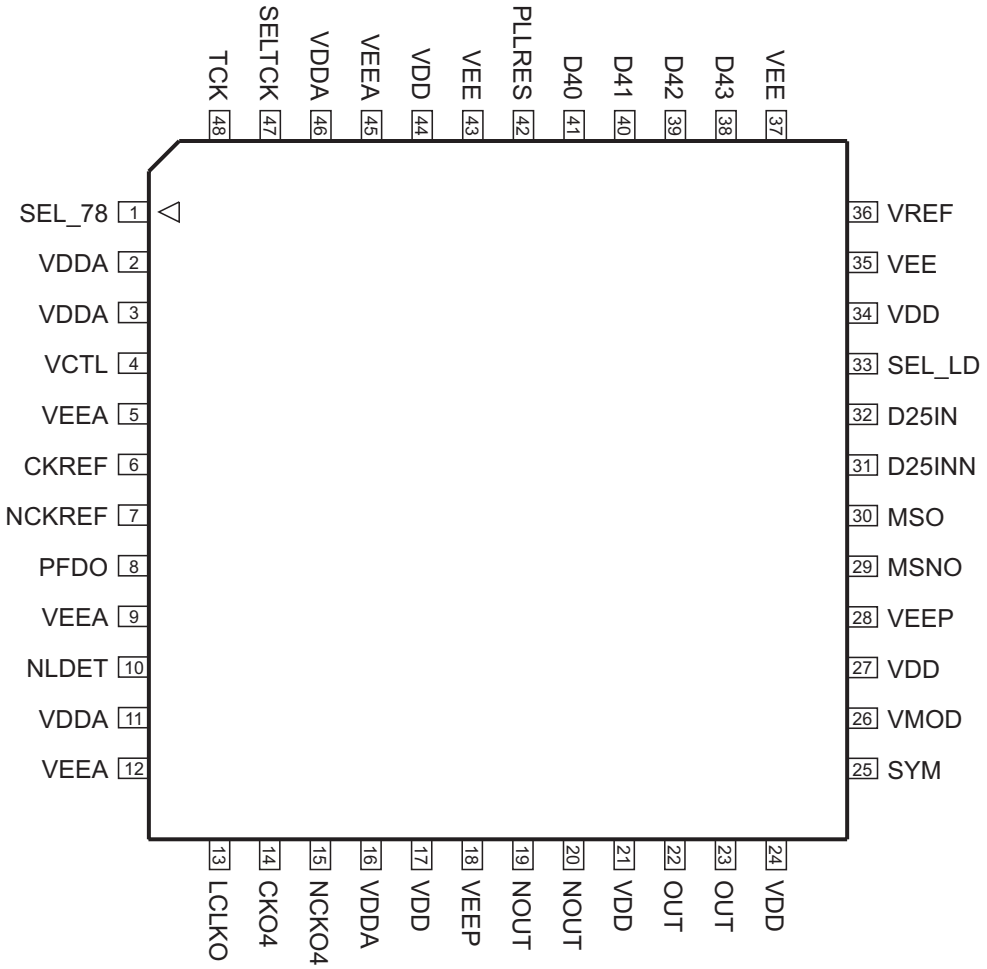


Figure 6. *Package Pinout, 48 Lead TQFP - Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages in the table are referred to VDD (Ground).
All currents in the table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE},V_{EEA},V_{EEP}	Power Supply		-6		0	V
V_O	Applied Voltage (All Outputs)		V_{EE} -0.5		0.5	
$V_{O\ OUT/NOUT}$	Applied Voltage OUT,NOUT		V_{EE} -0.5		2	V
$I_{O\ ECL}$	Output Current ECL		-10		40	mA
$I_{O\ NLDET}$	Output Current NLDET		-3		8	mA
$I_{O\ MSO,MSNO}$	Output Current MSO, MSNO		-4		4	mA
V_I	Applied Voltage		V_{EE} -0.5		0.5	V
$V_{IO\ ESD}$	ESD I/O Sensitivity	Note 2		±500		V
$I_{I\ ECL}$	Input Current ECL		-1		1	mA
$I_{I\ SYM}$	Input Current SYM		-4		4	mA
$I_{I\ VMOD}$	Input Current VMOD	Note 1	-6		6	mA
T_O	Operating Temperature	Channel	-40		+125	°C
T_S	Storage Temperature		-65		+150	°C

Note 1: Voltage and/or current should be externally limited to specified range.
Note 2: Human body model (100 pF, 1500 Ω) MIL 883 standard. Actual ESD level TBD.

DC Characteristics

T_{CASE} = 0 °C to 85 °C, appropriate heat sinking may be required.

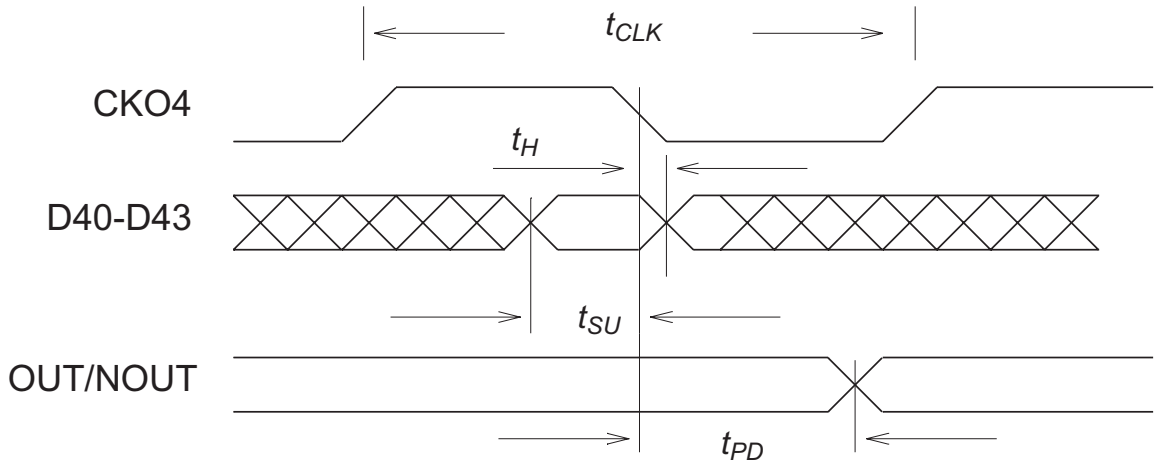
All voltages in table are referred to VDD.
All currents in table are defined positive out of the pin.

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{EE}, V_{EEA}, V_{EEP}	Power Supply		-5.5	-5.2	-4.7	V
I_{EE}	Negative Supply Current			200		mA
P_{DISS}	Power Dissipation	V_{EE} = -5.0V (Note 1)		0.95		W
V_{REF}	Internal ECL ref.	V_{EE} = -5.0V		-1.3		V
$V_{IH\ ECL}$	ECL Input HI Voltage	V_{REF}=-1.3V	-1.1		-0.7	V
$V_{IL\ ECL,}$	ECL Input LO Voltage	V_{REF}=-1.3V	-2		-1.5	V
$I_{IH\ ECL}$	ECL Input HI Current	@$V_{IH\ max}$		TBD		µA
$I_{IL\ ECL}$	ECL Input LO Current	@$V_{IL\ min}$		TBD		µA
$I_{IH\ CKREF,NCKREF}$	CKREF and NCKREF Input HI Current	@$V_{IH\ max}$		TBD		µA
$I_{IL\ CKREF,NCKREF}$	CKREF and NCKREF Input LO Current	@$V_{IL\ min}$		TBD		µA
$V_{I\ VMOD}$	VMOD Input Voltage		V_{EE}		V_{DD}	V
$V_{I\ VCTL}$	VCTL Input Voltage		V_{EE}		-0.5	V
$V_{I\ SYM}$	SYM Input Voltage		-4.5	-2.5	-0.5	V
$V_{O\ OUT,NOUT}$	OUT,NOUT Output Voltage	Note 3	-2.0		-0.05	V
$V_{O\ MSO,MSNO}$	MSO,MSNO Output Voltage	Note 4		-1.0	0	V
$I_{OH\ ECL}$	ECL Output HI Current	Note 2	20	23	30	mA
$I_{OL\ ECL}$	ECL Output LO Current	Note 2	-8.0	-5	0	mA
$V_{OH\ NLDET}$	NLDET Output HI Voltage		-1.2		0	V
$V_{OL\ NLDET}$	NLDET Output LO Voltage		V_{EE}		V_{EE}+1.2	V
$I_{OH\ NLDET}$	NLDET Output HI Current		1.0			mA
$I_{OL\ NLDET}$	NLDET Output LO Current		-1.0			mA
$I_{OH\ OUT,NOUT}$	OUT,NOUT HI Current	Note 3, 5	-60		-5	mA
$I_{OL\ OUT,NOUT}$	OUT,NOUT LO Current	Note 3	-3		1	mA
$I_{OH\ CHP}$	PFDO Source Current	Terminated to -2.5V		100		µA
$I_{OL\ CHP}$	PFDO Sink Current	Terminated to -2.5V		100		µA

Note 1: Laser Driver modulation current I_{OUT}, I_{NOUT} forced to 0 mA.
Note 2: R_{LOAD} = 50 Ω to V_{TT} = -2.0 V for all ECL outputs only.
Note 3: R_{LOAD} = 50 Ω to V_{DD}. Sink current is controlled by VMOD pin and may be adjusted in the range as specified.
Note 4: Output swings between -2.0 V and 0 V (typ.). Output impedance (resistive) is 4 kΩ (typ.).
Note 5: Typically the maximum sink current will be 60 mA.

AC Characteristics

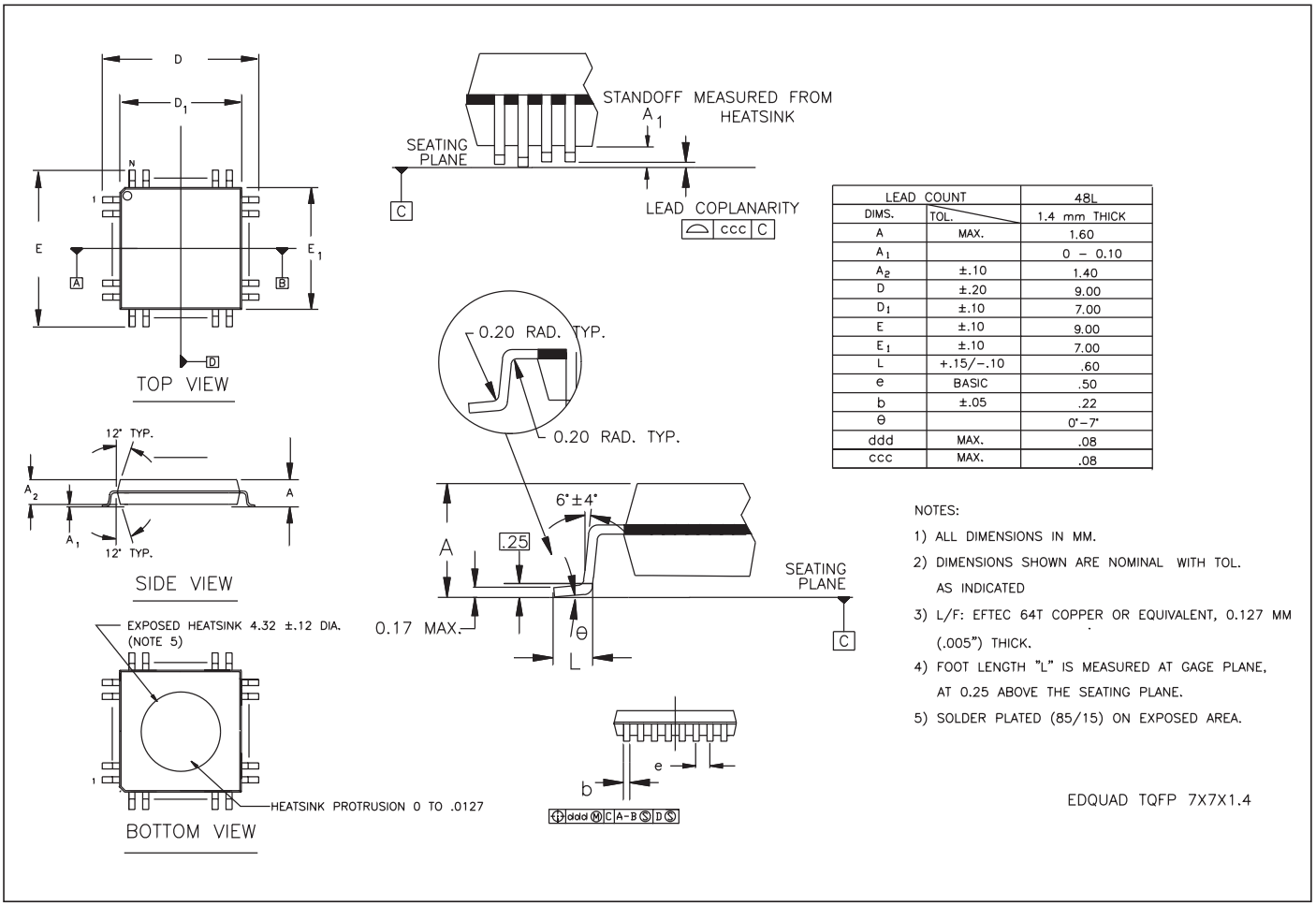
T_{CASE} = 0 °C to 85 °C, appropriate heat sinking may be required.



Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$f_{MAX\ CKREF}$	CKREF Input Frequency			77.8		MHz
$f_{MAX\ LCLKO}$	LCLKO Output Frequency			38.6		MHz
$f_{MAX\ CLKO4}$	CLKO4 Output Frequency			622		MHz
$f_{MAX\ D40-3}$	Data Input Frequency			622		Mbit/s
$f_{MAX\ OUT}$	Data Output Frequency			2488.32		Mbit/s
t_{CLK}	Output Clock Cycle		1538	1608	1739	ps
$t_{SU\ D40-3,CKO4}$	Data Input Set-up Time	Note 1, 2	405			ps
$t_{H\ D40-3,CKO4}$	Data Input Hold Time	Note 1, 2		-110	0	ps
$t_{RISE\ OUT}$	Output Rise Time	Note 3		100		ps
$t_{FALL\ OUT}$	Output Fall Time	Note 3		100		ps
$t_{PD\ CKO4}$	CKO4 Output Propagation Delay (CLK=CKREF).	Note 4		430		ps
t_{PW}	Output Pulse Width	Note 5		402		ps
$t_{PW,ADJ.}$	Output Pulse Width adj. +/-	Note 6	50			ps
K_{VCO}	VCO Gain Constant			200		MHz/V
$J_{rms}OUTJ_{pp}OUT$	OUT jitter (RMS) 12 kHz - 20 MHz OUT pp jitter 12 kHz - 20 MHz OUT pp jitter 1 MHz - 20 MHz	Note 7 Note 7 Note 7		4 40 36		mUI mUI mUI
f_{VCO}	VCO Frequency Range		2400	2488	2700	MHz

Note 1: See timing definitions above. PLL must be in phase-locked state.
Note 2: DATA = D40-3 set-up and hold times are referred to CLK = CKO4 (falling edge).
Note 3: R_{LOAD} = 50 Ω, terminated to *VDD*. I_{LD} = 60 mA. Rise/Fall times at 20 - 80% of HI/LO voltage levels.
Note 4: R_{LOAD} = 50 Ω, terminated to V_{TT} = -2.0 V. See timing definitions above.
Note 5: 2.5 Gbit/s operation assumed. I_{LD} =20 – 60 mA, V(SYM) = V_{EE}/2 +2.0 V (target specification).
Note 6: Pulse width may be adjusted by forcing internal bias of SYM +/-2.0 V max. from its internal value -2.5 V (R_{in} = 500 Ω).
Note 7: Assuming 2.5 Gbit/s operation with the PLL in lock and assuming that the reference clock jitter is insignificant within the loop bandwidth, that the loop filter is designed for < 0.1 dB peaking and a loop Q = 600 (BW = 2.075 MHz base band).

Package Outline



LEAD COUNT		48L
DIMS.	TOL.	1.4 mm THICK
A	MAX.	1.60
A_1		0 – 0.10
A_2	±.10	1.40
D	±.20	9.00
D_1	±.10	7.00
E	±.10	9.00
E_1	±.10	7.00
L	+.15/–.10	.60
e	BASIC	.50
b	±.05	.22
θ		0°–7°
ddd	MAX.	.08
ccc	MAX.	.08

Figure 7. *Package 48 Lead TQFP, Power Enchanded*

Device Marking

Figure 8. *Device Marking, Top View*

Ordering Information

To order, please specify as shown below:

Product Name:	**Intel Order Number**:	**Package Type:**	**Case Temperature Range:**
GD16553-48BA	**FAGD1655348BA** MM#: 836074	48 lead TQFP, EDQUAD	0..85 °C

an Intel company
Mileparken 22, DK-2740 Skovlunde
Denmark
Phone : +45 7010 1062
Fax : +45 7010 1063
E-mail : sales@giga.dk
Web site : http://www.intel.com/ixa

Please check our Internet web site for latest version of this data sheet.

Distributor: