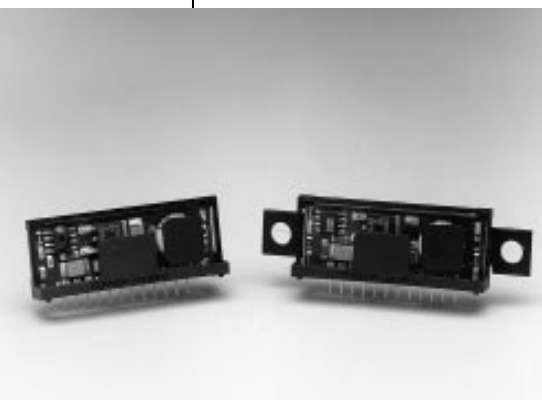
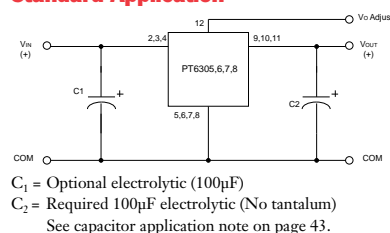


PT6305 Series**3 AMP HIGH-PERFORMANCE
ADJUSTABLE ISR**

- Single-Device 5V to 3V Power
- 85% Efficiency
- Small SIP Footprint:
0.36" x 2.00" x 0.60"(H)
- Wide Input Voltage Range:
+4.5V to +9.0V
- Internal Short Circuit Protection
- Over-Temperature Protection

The PT6305N is Power Trends' new high performance +5V to +3.3V, 3

Amp, 12-Pin SIP (Single In-line-Package) Integrated Switching Regulator (ISR). This high-performance ISR allows easy integration of low-power 3.3V logic IC's into existing 5V systems without redesigning the central power supply. Only one external capacitor is required for proper operation. The PT6306,7,8 can be used to power high-speed data buses (+2.1V), or the new GTL (+1.2V) logic buses.

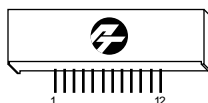
Standard Application**Specifications**

Characteristics (T _a =25°C unless noted)	Symbols	Conditions	PT6305 SERIES				
			Min	Typ	Max	Units	
Output Current	I _o	4.5 ≤ V _{in} ≤ V _{in} MAX	0.3	—	3.0**	ADC	
Current Limit	I _{cl}	V _{in} = +5V	—	3.6	5.0	ADC	
Short Circuit Current	I _{sc}	V _{in} = +5V	—	5.0	—	Apk	
Input Voltage Range	V _{in}	0.3A ≤ I _o ≤ 3.0A	PT6305N	4.5	—	9	VDC
			PT6306N	4.5	—	9	VDC
			PT6307N	4.5	—	9	VDC
			PT6308N	4.5	—	6.0	VDC
Static Voltage Tolerance	V _o	V _{in} = +5V, I _o = 3.0A 0°C ≤ T _a ≤ +70°C	PT6305N	3.2	3.3	3.4	VDC
			PT6306N	1.7	1.8	1.9	VDC
			PT6307N	2.0	2.1	2.2	VDC
			PT6308N	1.1	1.2	1.3	VDC
Line Regulation	Reg _{line}	4.5V ≤ V _{in} ≤ 5.5V, I _o = 3.0A	—	±25	±50	mV	
Load Regulation	Reg _{load}	V _{in} = +5V, 0.3 ≤ I _o ≤ 3.0A	—	±25	±50	mV	
V _o Ripple/Noise pk-pk	V _n	V _{in} = 5V, I _o = 3.0A	—	66	—	mV	
Transient Response with C ₂ = 100µF	t _{tr} V _{os}	I _o step between 1.5A and 3.0A V _o over/undershoot	—	200	—	µSec	
			—	200	—	mV	
Efficiency	η	V _{in} = +5V, I _o = 1.5A	PT6305N	—	85	—	%
			PT6306N	—	74	—	%
			PT6307N	—	77	—	%
			PT6308N	—	63	—	%
		V _{in} = +5V, I _o = 3.0A	PT6305N	—	80	—	%
			PT6306N	—	68	—	%
			PT6307N	—	72	—	%
			PT6308N	—	57	—	%
Switching Frequency	f _o	4.5 ≤ V _{in} ≤ V _{in} MAX 0.3A ≤ I _o ≤ 3.0A	500	650	800	KHz	
Operating Temperature	T _a	Free Air Convection (40-60 LFM) Over V _{in} and I _o Ranges	0	—	+70*	°C	
Thermal Resistance	θ _{ja}	Free Air Convection (40-60 LFM)	—	25	—	°C/W	
Storage Temperature	T _s	—	-40	—	+125	°C	
Mechanical Shock	Per Mil-STD-883D, Method 2002.3 Condition A, 1 msec, Half Sine, mounted to a fixture		—	—	500	G's	
Mechanical Vibration	Per Mil-STD-883D, Method 2007.2 Condition A, 20-2000 Hz		—	—	15	G's	
Weight	—	—	—	11.2	—	grams	
Relative Humidity	—	Non-condensing	0	—	95	%	

*See Thermal Derating chart. **The PT6305 Series can be easily paralleled to provide output current in multiples of 3 amps. Please contact a Power Trends' Application Engineer for the appropriate application note. **Note:** The PT6305 Series requires a 100µF electrolytic capacitor for proper operation in all applications.

Pin-Out Information

Pin No.	Function	Pin No.	Function
1	N/C	7	GND
2	V_{in}	8	GND
3	V_{in}	9	V_{out}
4	V_{in}	10	V_{out}
5	GND	11	V_{out}
6	GND	12	Adjust (See page 40.)

**Ordering Information**

PT6305□ = +3.3 Volts

PT6306□ = +1.8 Volts

PT6307□ = +2.1 Volts

PT6308□ = +1.2 Volts

(For dimensions, see page 66.)

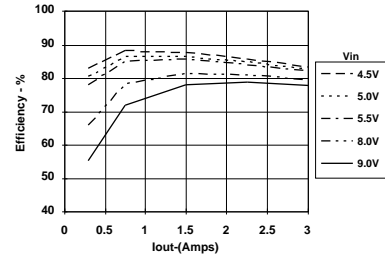
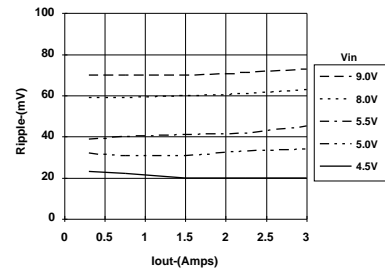
PT Series Suffix (PT1234X)

Case/Pin Configuration	Heat Tab Configuration	
	None	Side
Vertical Through-Hole	N	R
Horizontal Through-Hole	A	G
Horizontal Surface Mount	C	B

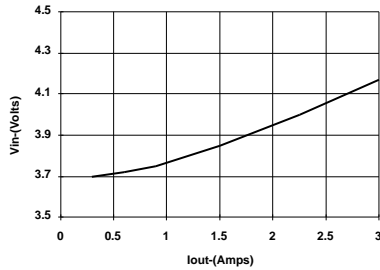
(See Thermal Application Notes on page 44 for heat tab application data.)

CHARACTERISTIC DATA**PT6305, 3.3 VDC**

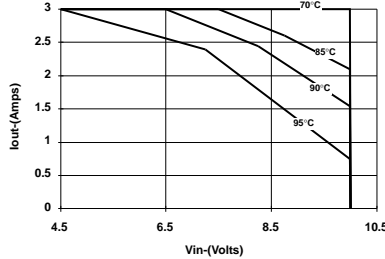
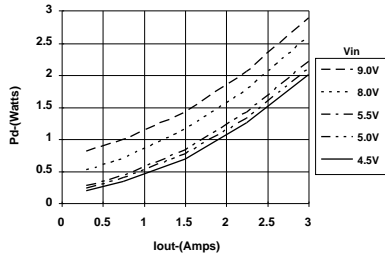
(See Note 1)

Efficiency vs Output Current**Ripple vs Output Current****Minimum Input Voltage**

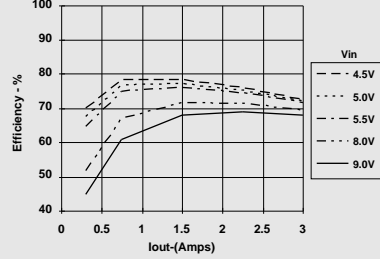
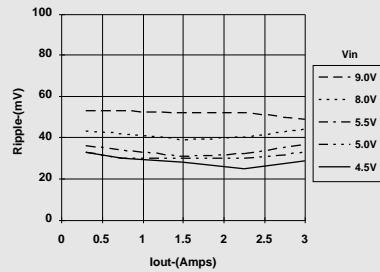
(See Note 2)

**Thermal Derating (T_a)**

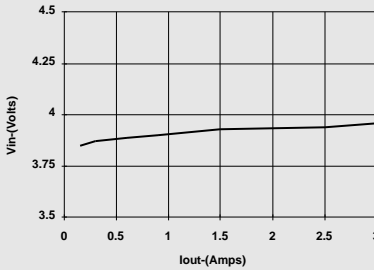
(See Note 3)

**Power Dissipation vs Output Current****PT6307, 2.1 VDC**

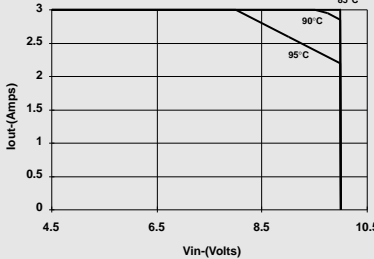
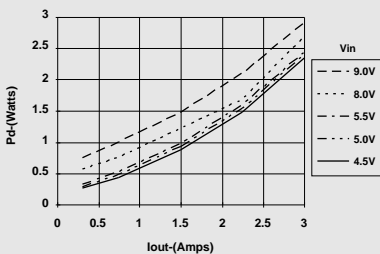
(See Note 1)

Efficiency vs Output Current**Ripple vs Output Current****Minimum Input Voltage**

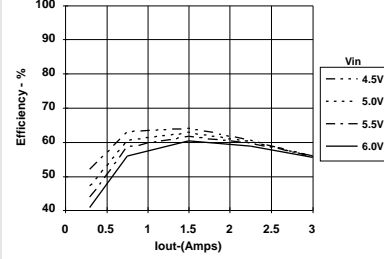
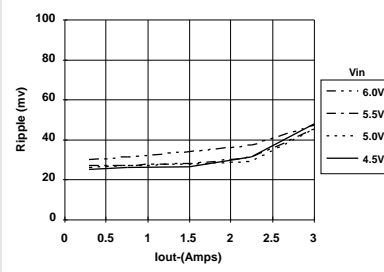
(See Note 2)

**Thermal Derating (T_a)**

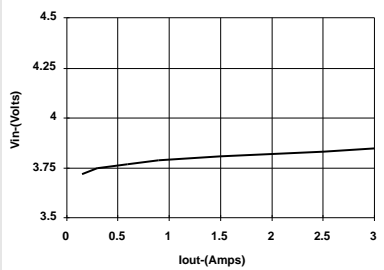
(See Note 3)

**Power Dissipation vs Output Current****PT6308, 1.2 VDC**

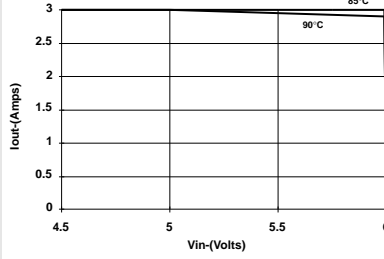
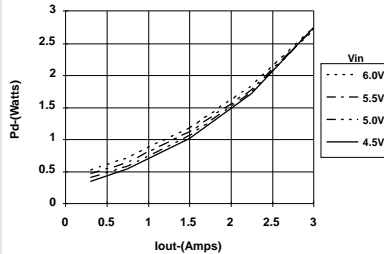
(See Note 1)

Efficiency vs Output Current**Ripple vs Output Current****Minimum Input Voltage**

(See Note 2)

**Thermal Derating (T_a)**

(See Note 3)

**Power Dissipation vs Output Current****Note 1:** All data listed in the above graphs, except for derating data, has been developed from actual products tested at 25°C. This data is considered typical data for the ISR.**Note 2:** Minimum V_{in} data is typical and is not guaranteed. The data corresponds to a 2% output voltage drop.**Note 3:** Thermal derating graphs are developed in free air convection cooling of 40-60 LFM with no optional heat tab soldered in a printed circuit board. (See Thermal Application Notes).

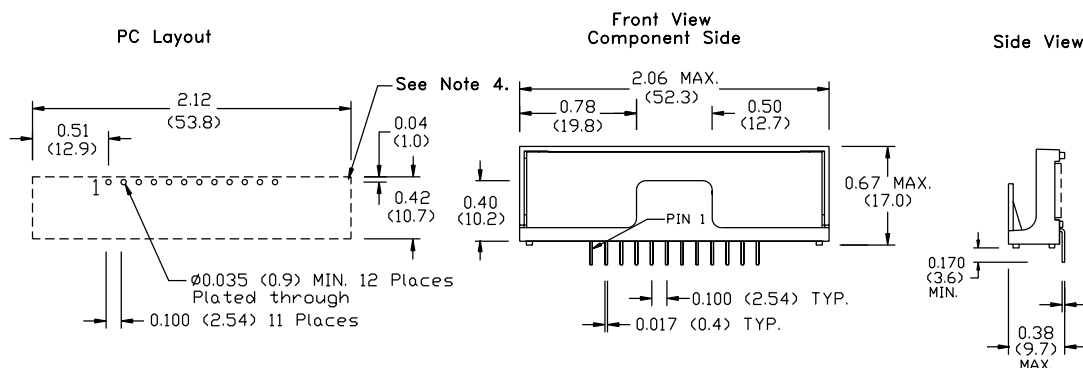
Package Style 300

Suffix A, C, D, E, N, P

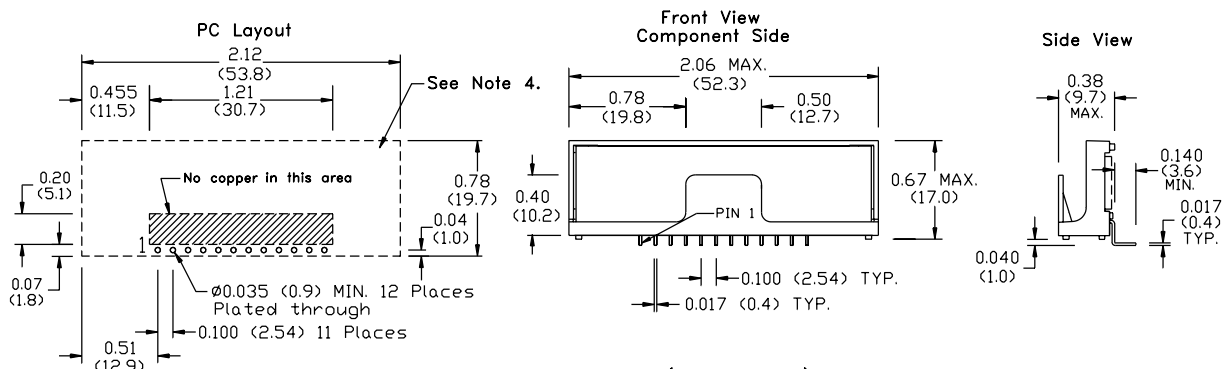
PACKAGE INFORMATION AND DIMENSIONS

Revised 2/11/2000

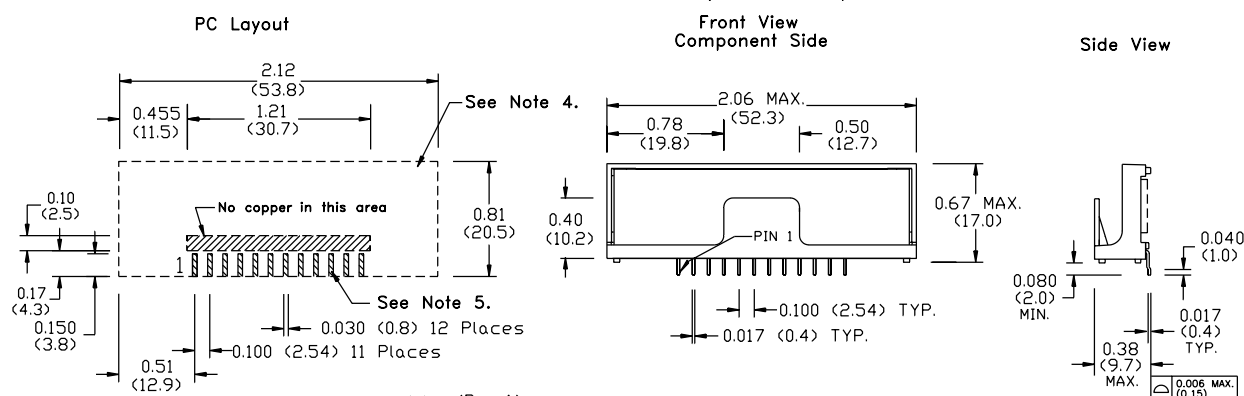
Vertical Through-Hole Mount (Suffix N & P)



Horizontal Through-Hole Mount (Suffix A & D)



Surface Mount (Suffix C & E)



Notes: (Rev.A)

- 1: All dimensions are in inches (mm).
- 2: 2 place decimals are ± 0.030 (± 0.8 mm).
- 3: 3 place decimals are ± 0.010 (± 0.3 mm).
- 4: Recommended mechanical keep out area.
- 5: Power pin connections should utilize two or more vias per input, ground and output pin.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PT6306A	LIFEBUY	SIP MODULE	ECA	12		TBD	Call TI	Call TI	0 to 70		
PT6306B	LIFEBUY	SIP MODULE	ECK	12		TBD	Call TI	Call TI	0 to 70		
PT6306C	LIFEBUY	SIP MODULE	ECC	12		TBD	Call TI	Call TI	0 to 70		
PT6306G	LIFEBUY	SIP MODULE	ECG	12		TBD	Call TI	Call TI	0 to 70		
PT6306R	LIFEBUY	SIP MODULE	ECE	12		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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