National Semiconductor

LMX2310U/LMX2311U/ LMX2312U/LMX2313U

OBSOLETE
October 18, 2011

PLLatinum™ Ultra Low Power Frequency Synthesizer for RF Personal Communications

LMX2310U 2.5 GHz LMX2311U 2.0 GHz
LMX2312U 1.2 GHz LMX2313U 600 MHz

General Description

The LMX2310/1/2/3U are high performance frequency synthesizers. The LMX2310/1/2U use a selectable, dual modulus 32/33 and 16/17 prescaler. The LMX2313U uses a selectable, dual modulus 16/17 and 8/9 prescaler. The device, when combined with a high quality reference oscillator and a voltage controlled oscillator, generates very stable, low noise local oscillator signals for up and down conversion in wireless communication devices.

Serial data is transferred into LMX2310/1/2/3U via a three-wire interface (Data, Enable, Clock) that can be directly interfaced with low voltage baseband processors. Supply voltage can range from 2.7V to 5.5V. LMX2310U features very low current consumption, typically 2.3 mA at 3.0V.

The LMX2310/1/2/3U are manufactured using National's 0.5µ ABiC V silicon BiCMOS process and is available in 20-pin CSP packages.

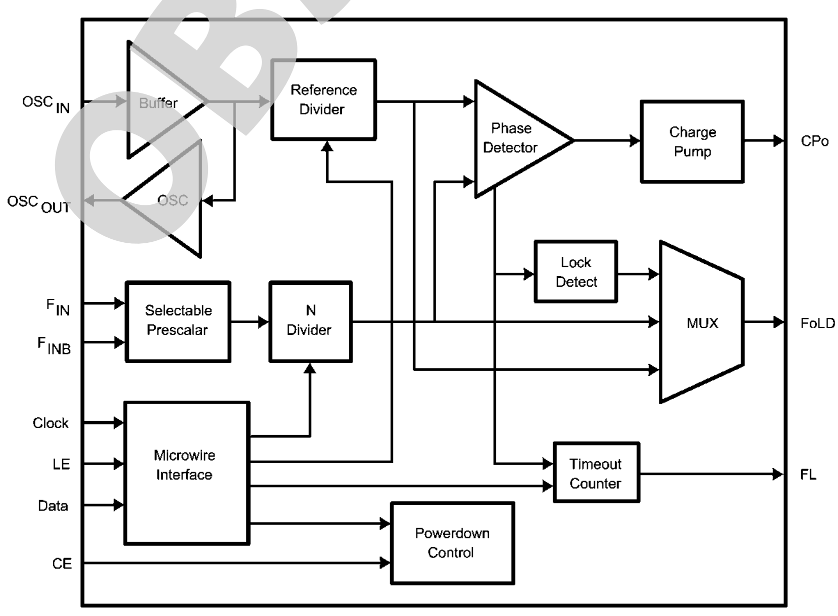
Features

- RF operation up to 2.5 GHz
- 2.7V to 5.5V operation
- Ultra Low Current Consumption
- Low prescaler values
  - LMX2310/1/2U 32/33 or 16/17
  - LMX2313U 16/17 or 8/9
- Excellent Phase Noise
- Internal balanced, low leakage charge pump
- Selectable Charge Pump Current Levels
- Selectable Fastlock mode with Time-Out Counter
- Low Voltage MICROWIRE interface (1.72V to V_{CC})
- Digital and Analog Lock Detect
- Small 20-pad Thin Chip Scale Package

Applications

- Cellular DCS, PCS, WCDMA telephone systems
- Wireless Local Area Networks (WLAN)
- Global Positioning Systems (GPS)
- Other wireless communications systems

Functional Block Diagram



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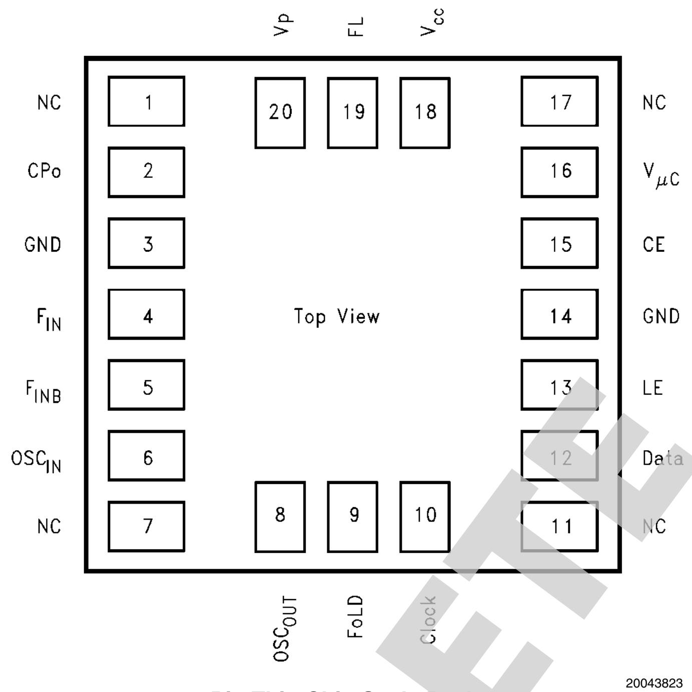
LMX2310U/LMX2311U/LMX2312U/LMX2313U PLLatinum Ultra Low Power Frequency Synthesizer for RF Personal Communications

Connection Diagram



20-Pin Thin Chip Scale Package
NS Package Number SLD20A

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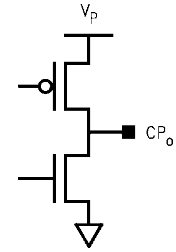
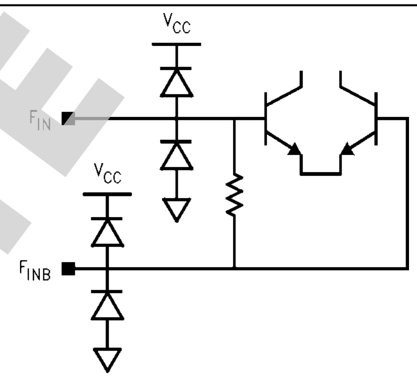
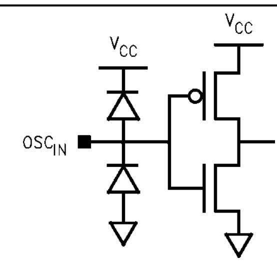
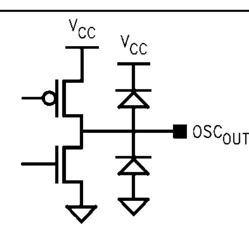
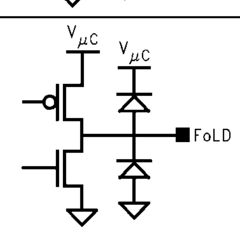
Pin Descriptions

Pin Number	Pin Name	I/O	Description	I/O Circuit Configuration
1	NC	—	No Connect.	
2	CP_o	O	Charge Pump output. For connection to a loop filter for driving the voltage control input of an external VCO.	
3	GND	—	Analog ground.	
4	F_{IN}	I	RF prescaler input. Small signal input from the VCO.	
5	F_{INB}	I	RF prescaler complementary input. For single ended operation, this pin should be AC grounded. The LMX2310/1/2/3U can be driven differentially when a bypass capacitor is omitted.	
6	OSC_{IN}	I	Oscillator input. An input to a CMOS low noise inverting buffer. The input can be driven from an external CMOS or TTL logic gate.	
7	NC	—	No Connect.	
8	OSC_{OUT}	O	Oscillator output. The OSC_{IN} low noise buffer drives an independent oscillator buffer. Its output is connected to the OSC_{OUT} pin. It can be used as a buffer to provide the reference oscillator frequency to other circuitry or as a crystal oscillator.	
9	FoLD	O	Multi-function CMOS output pin that provides multiplexed access to digital lock detect, open drain analog lock detect, as well as the outputs of the R and N counters. The FoLD pin is internally referenced to $V_{\mu C}$.	

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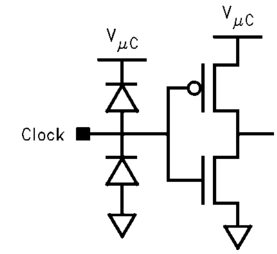
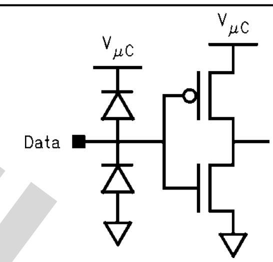
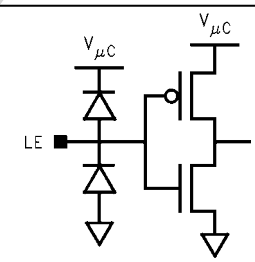
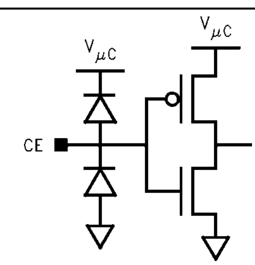
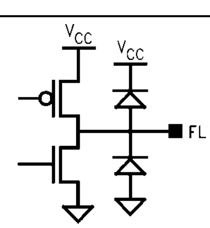
Pin Number	Pin Name	I/O	Description	I/O Circuit Configuration
10	Clock	I	High impedance CMOS Clock input. Data for the counters is clocked in on the rising edge, into the 22-bit shift register. The Clock is internally referenced to $V_{\mu C}$.	
11	NC	—	No Connect.	
12	Data	I	High impedance CMOS Data input. Serial Data is entered MSB first. The last two bits are the address for the target registers. The Data is internally referenced to $V_{\mu C}$.	
13	LE	I	High impedance CMOS LE input. When Latch Enable goes HIGH, data stored in the 22-bit shift register is loaded into one the 3 control registers, based on the address field. The Latch Enable is internally referenced to $V_{\mu C}$.	
14	GND	—	Digital ground.	
15	CE	I	High impedance CMOS Chip Enable input. Provides logical power-down control of the device. Pull-up to $V_{\mu C}$ if unused. The Chip Enable is internally referenced to $V_{\mu C}$.	
16	$V_{\mu C}$	—	Power supply for MICROWIRE circuitry. Must be ≤ V_{CC}. Typically connected to same supply level as microprocessor or baseband controller to enable programming at low voltages.	
17	NC	—	No Connect.	
18	V_{CC}	—	Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.	
19	FL	O	Fastlock mode output. In Fastlock mode this pin is at logic low. When not in Fastlock mode, this pin is in TRI-STATE mode. This pin can also be forced to TRI-STATE, forced low or forced high by the programming of the first two-bits of the Timeout Counter.	
20	V_P	—	Power supply for charge pump. Must be ≥ V_{CC}.	

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Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage, (V_{CC}, V_P, $V_{\mu C}$)	−0.3V to +6.5V
Voltage on any pin with GND=0V	
CP_o, FL, F_{IN}, OSC_{IN}, OSC_{OUT} (V_i)	−0.3V to V_{CC} + 0.3V
Data, Clock, LE, CE, FoLD (V_i)	−0.3V to $V_{\mu C}$ + 0.3V
Storage Temperature Range, (T_S)	−65°C to +150°C
Lead Temp. (solder 4 sec.), (T_L)	+260°C

Recommended Operating Conditions (Note 1)

	Min	Max	Unit
Power Supply Voltage			
(V_{CC})	2.7	5.5	V
(V_P)	V_{CC}	5.5	V
($V_{\mu C}$)	1.72	V_{CC}	V
Operating Temperature, (T_A)	−40	+85	°C

Electrical Characteristics

$V_{CC} = V_P = V_{\mu C}$ = 3.0V, −40°C < T_A < +85°C unless specified otherwise.

Symbol	Parameter		Conditions (Note 3)	Min	Typ	Max	Units
I_{CC}							
I_{CC}	Power Supply Current	LMX2310U	(Note 4)		2.3	3.0	mA
			V_{CC} = 5.5V (Note 4)			3.4	mA
		LMX2311U	(Note 4)		2.0	2.7	mA
			V_{CC} = 5.5V (Note 4)			3.2	mA
		LMX2312U	(Note 4)		1.4	2.0	mA
			V_{CC} = 5.5V (Note 4)			2.4	mA
		LMX2313U	(Note 4)		1.0	1.3	mA
			V_{CC} = 5.5V (Note 4)			1.6	mA
$I_{CC-PWDN}$	Power-Down Current		Clock, Data and LE = GND CE = GND		1	10	µA
RF PRESCALER							
F_{IN}	Operating Frequency	LMX2310U		0.5		2.5	GHz
		LMX2311U		0.5		2.0	GHz
		LMX2312U		0.2		1.2	GHz
		LMX2313U		45		600	MHz
PF_{IN}	Input Sensitivity, RF Prescaler		2.7 ≤ V_{CC} ≤3.0V (Note 5)	−15		0	dBm
			3.0V < V_{CC} ≤ 5.5V (Note 5)	−10		0	dBm
PHASE DETECTOR							
Fφ	Phase Detector Frequency					10	MHz
REFERENCE OSCILLATOR							
F_{OSC}	Operating Frequency, Reference Oscillator Input			2		50	MHz
$V_{OSC_{IN}}$	Input Sensitivity, Reference Oscillator Input		(Note 6)	0.5		V_{CC}	V_{P-P}
I_{IH}	OSC_{IN} Input Current		$V_{IH} = V_{CC}$ = 5.5V			100	µA
I_{IL}	OSC_{IN} Input Current		V_{IL} = 0, V_{CC} = 5.5V	−100			µA
$V_{OSC_{OUT}}$	OSC_{OUT} Bias Level		OSC_{IN} Open		1.5		V
$D_{OSC_{OUT}}$	OSC_{OUT} Duty Cycle		OSC_{IN} = 20 MHz, 0.5 V_{P-P}, OSC_{IN} Duty Cycle = 50%		50		%
$V_{OSC_{OUT}}$	OSC_{OUT} Level		OSC_{IN} = 20 MHz, 0.5 V_{P-P} , OSC_{OUT} Load = 10 pF ǁ 10 k Ohm		2.6		V_{P-P}
V_{OH}	OSC_{OUT} Output Voltage		I_{OH} = -500 µA	2.6	2.8		V
V_{OL}	OSC_{OUT} Output Voltage		I_{OL} = 500 µA		0.2	0.4	V
I_{OH}	OSC_{OUT} Output Current		V_{OH} = 2.25 V		-1.1		mA

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Symbol	Parameter	Conditions (Note 3)	Min	Typ	Max	Units
I_{OL}	OSC_{OUT} Output Current	V_{OL} = 0.75 V		1.1		mA
CHARGE PUMP						
ICPo-$_{source}$	Charge Pump Output Current (Note 7)	VCPo = Vp/2, **ICPo_4X** = 0	0.8	1.0	1.2	mA
ICPo-$_{sink}$		VCPo = Vp/2, **ICPo_4X** = 0	−0.8	−1.0	−1.2	mA
ICPo-$_{source}$		VCPo = Vp/2, **ICPo_4X** = 1	3.2	4.0	4.8	mA
ICPo-$_{sink}$		VCPo = Vp/2, **ICPo_4X** = 1	−3.2	−4.0	−4.8	mA
ICPo-$_{tri}$	Charge Pump TRI-STATE Current	0.5V ≤ VCPo ≤ V_P − 0.5V	−2.5		2.5	nA
ICPo-$_{sink}$ vs. ICPo-$_{source}$	CP Sink vs. Source Mismatch	VCPo = Vp/2 T_A = 25°C (Note 8)		3	10	%
ICPo vs VCPo	CP Current vs. Voltage	0.5V ≤ VCPo ≤ V_P − 0.5V T_A = 25°C (Note 8)		8	15	%
ICPo vs T_A	CP Current vs. Temperature	VCPo = Vp/2V (Note 7)		8		%
DIGITAL INTERFACE (Data, Clock, LE, CE)						
V_{IH}	High-level Input Voltage	$V_{\mu C}$ = 1.72V to 5.5V	0.8 $V_{\mu C}$			V
V_{IL}	Low-level Input Voltage	$V_{\mu C}$ = 1.72V to 5.5V			0.2 $V_{\mu C}$	V
I_{IH}	High-level Input Current	V_{IH} = $V_{\mu C}$= 5.5V	−1.0		1.0	μA
I_{IL}	Low-level Input Current	V_{IL} = 0V, $V_{\mu C}$ = 5.5V	−1.0		1.0	μA
V_{OH}	High-level Output Voltage (Pin 7–FoLD)	I_{OH} = 500 μA	$V_{\mu C}$ − 0.4			V
	High-level Output Voltage (Pin 15–FL)	I_{OH} = −500 μA	V_{CC} − 0.4			V
V_{OL}	Low-level Output Voltage	I_{OL} = 1.0 mA (Note 9)		0.1	0.4	V
MICROWIRE TIMING (Data, Clock, LE, CE)						
t_{CS}	Data to Clock Set Up Time	(Note 10)	50			ns
t_{CH}	Data to Clock Hold Time	(Note 10)	20			ns
t_{CWH}	Clock Pulse Width High	(Note 10)	50			ns
t_{CWL}	Clock Pulse Width Low	(Note 10)	50			ns
t_{ES}	Clock to Load Enable Set Up Time	(Note 10)	50			ns
t_{EW}	Load Enable Pulse Width	(Note 10)	50			ns
PHASE NOISE CHARACTERISTICS						
$L_N(f)$	Normalized Single Side-Band Phase Noise	F_φ = 200 kHz F_{OSC} = 10 MHz V_{OSC} = 1.0 V_{PP} ICP_O = 4 mA T_A = 25°C (Note 11)		−159		dBc/Hz

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Symbol	Parameter	Conditions (Note 3)	Min	Typ	Max	Units
L(f)	Single Side-Band Phase Noise	LMX2310U F_{IN} = 2450 MHz F_{φ} = 200 kHz F_{OSC} = 10 MHz V_{OSC} = 1.0 V_{PP} ICP_O = 4 mA T_A = 25°C (Note 12)		−78		dBc/Hz
		LMX2311U F_{IN} = 1960 MHz F_{φ} = 200 kHz F_{OSC} = 10 MHz V_{OSC} = 1.0 V_{PP} ICP_O = 4 mA T_A = 25°C (Note 12)		−80		dBc/Hz
		LMX2312U F_{IN} = 902 MHz F_{φ} = 200 kHz F_{OSC} = 10 MHz V_{OSC} = 1.0 V_{PP} ICP_O = 4 mA T_A = 25°C (Note 12)		−85		dBc/Hz
		LMX2313U F_{IN} = 450 MHz F_{φ} = 50 kHz F_{OSC} = 10 MHz V_{OSC} = 1.0 V_{PP} ICP_O = 4 mA T_A = 25°C (Note 12)		−85		dBc/Hz

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the conditions listed.

Note 2: This device is a high performance RF integrated circuit with an ESD rating <2 kV. Handling and assembly of this device should only be done at ESD free workstations.

Note 3: Typical Conditions are at a T_A of 25°C.

Note 4: Icc current is measured with Clock, Data and LE pins connected to GND. OSCin and Fin pins are connected to Vcc. PWDN bit is program to 0. Icc current is the current into Vcc pin.

Note 5: See F_{IN} Sensitivity Test Setup.

Note 6: See OSC_{IN} Sensitivity Test Setup.

Note 7: Charge Pump Magnitude is controlled by CPo_4X bit [R18].

Note 8: See Charge Pump Measurement Definition for detail on how these measurements are made.

Note 9: Analog Lock Detect open drain output pin only can be pulled up to V_{ext} that will not exceed 6.5V.

Note 10: See Serial Input Data Timing.

Note 11: Normalized Single-Side Band Phase Noise is defined as: $L_N(f) = L(f) - 20 \log (F_{IN}/ F_{\varphi})$, where L(f) is defined as the Single Side-Band Phase Noise.

Note 12: Phase Noise is measured using a reference evaluation board with a loop bandwidth of approximately 12 kHz. The phase noise specification is the composite average of 3 measurements made at frequency offsets of 2.0 kHz, 2.5 kHz and 3.0 kHz.

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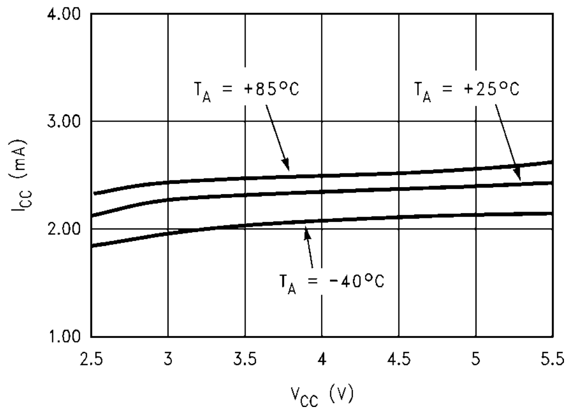
Typical Performance Characteristics

I_{cc} vs V_{cc} LMX2310U



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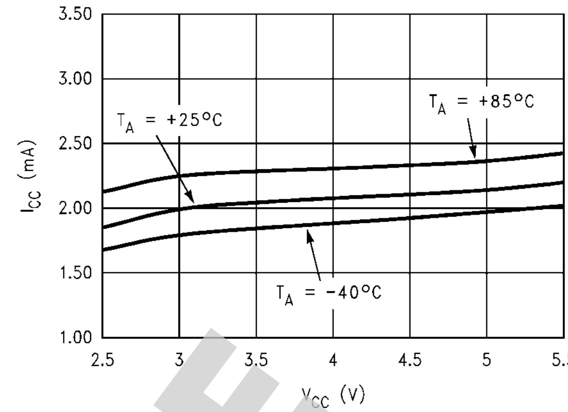
I_{cc} vs V_{cc} LMX2311U



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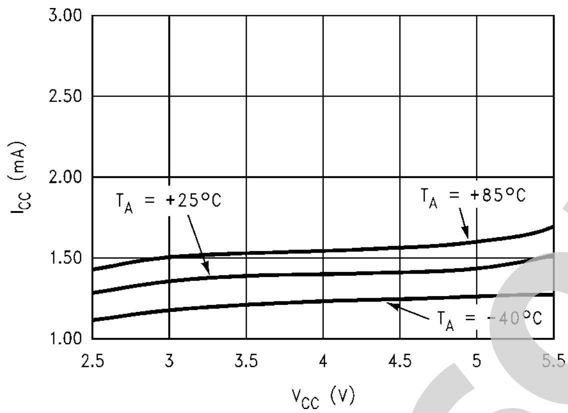
I_{cc} vs V_{cc} LMX2312U



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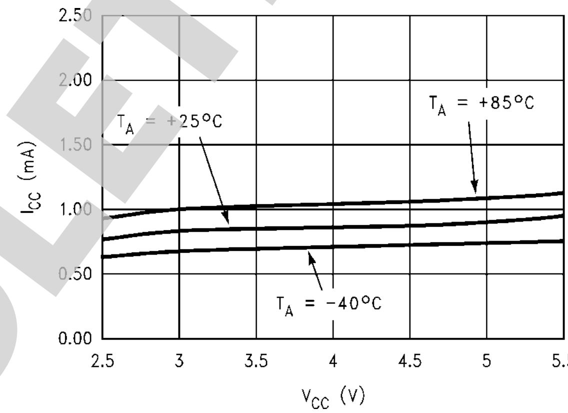
I_{cc} vs V_{cc} LMX2313U



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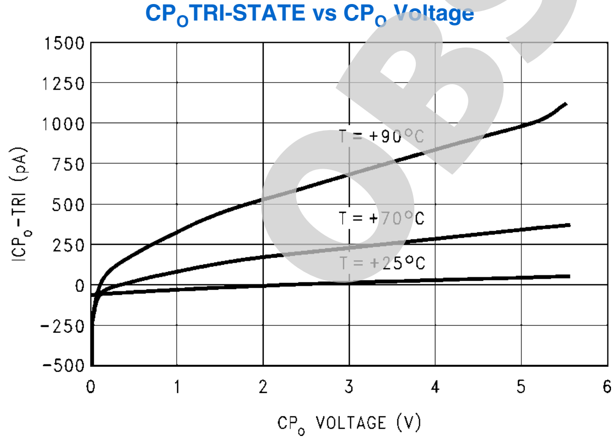
CP_OTRI-STATE vs CP_O Voltage



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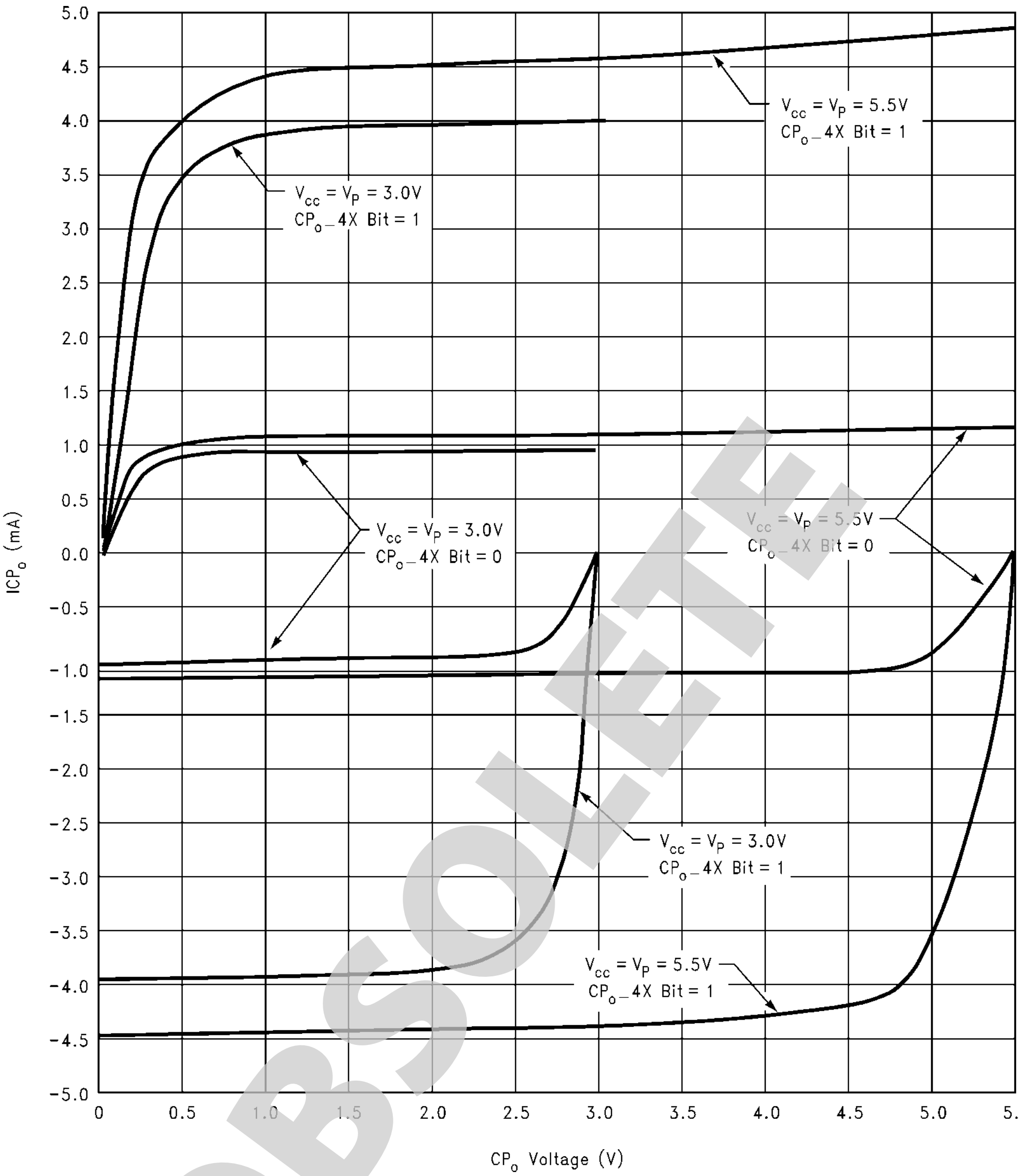
LMX231xU Charge Pump Sweeps



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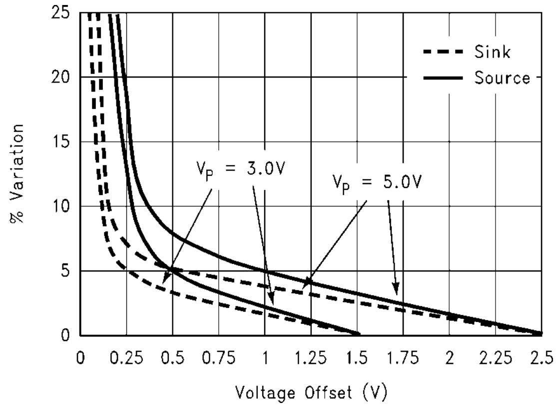
Charge Pump Current Variation (See formula under Charge Pump Current Specification Definitions)



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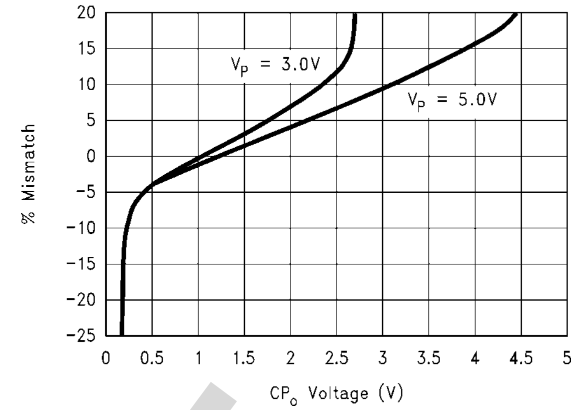
Sink Vs Source Mismatch (See formula under Charge Pump Current Specification Definitions)



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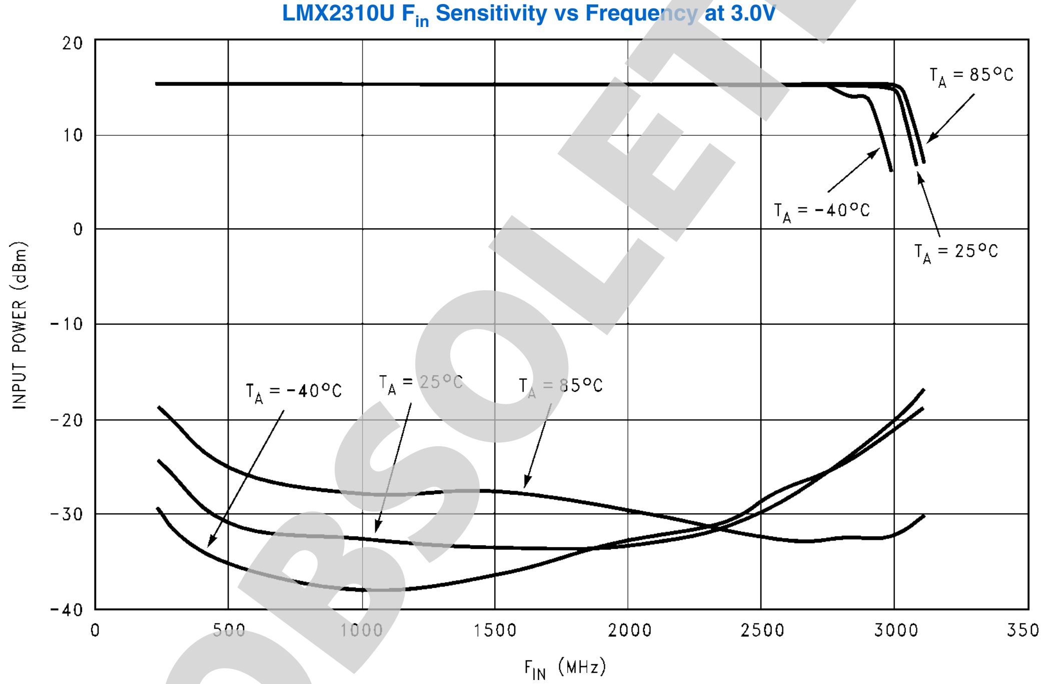
LMX2310U F_{in} Sensitivity vs Frequency at 3.0V



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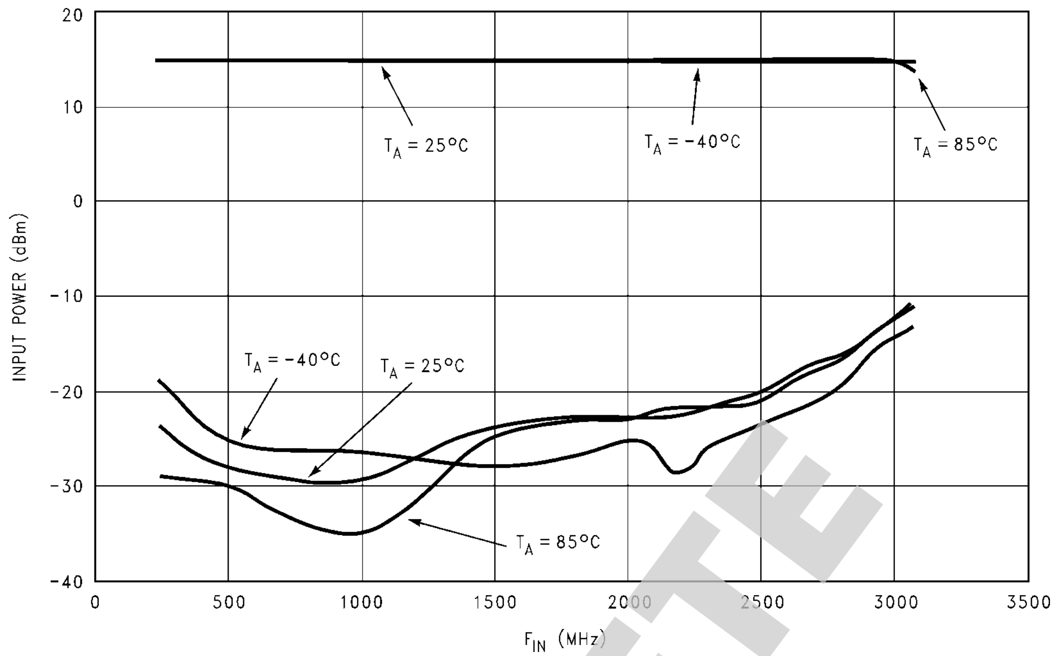
LMX2310U F_{in} Sensitivity vs Frequency at 5.5V



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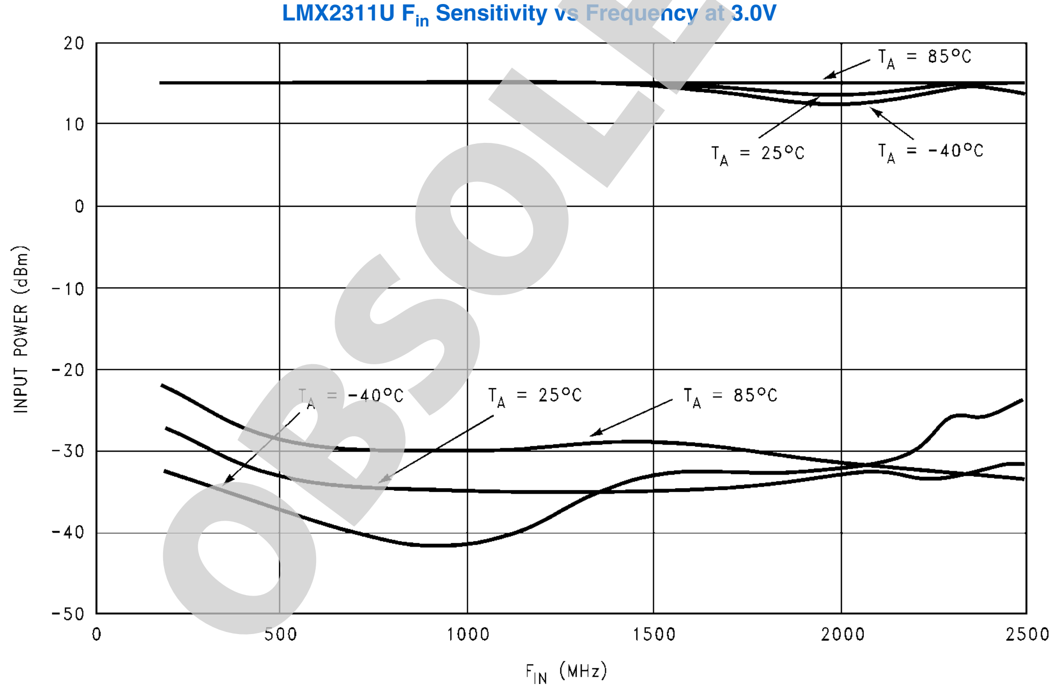
LMX2311U F_{in} Sensitivity vs Frequency at 3.0V



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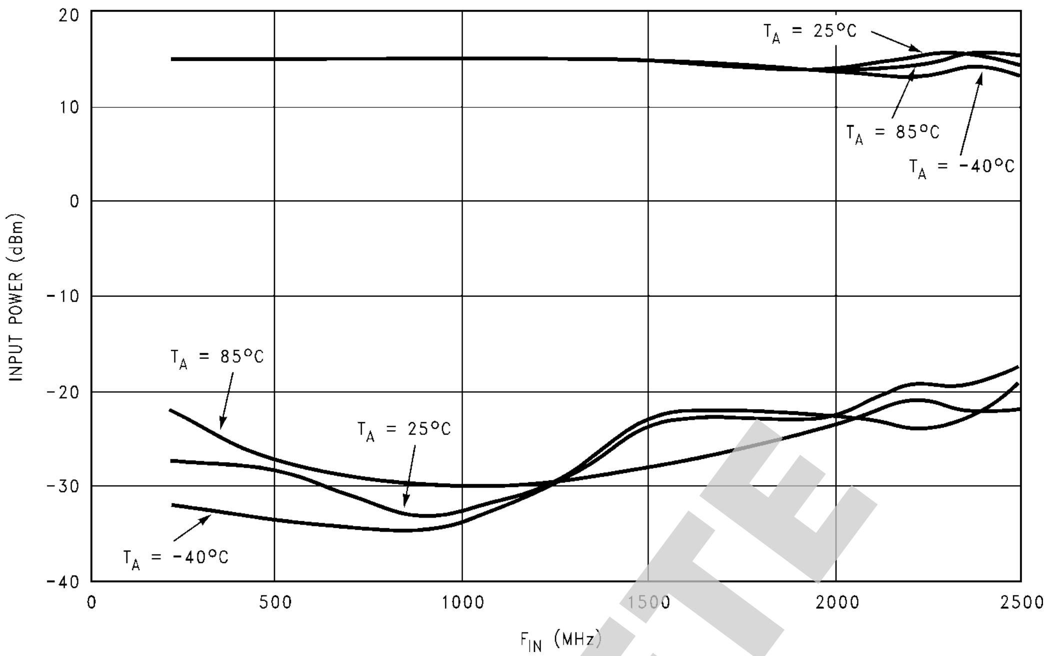
LMX2311U F_{in} Sensitivity vs Frequency at 5.5V



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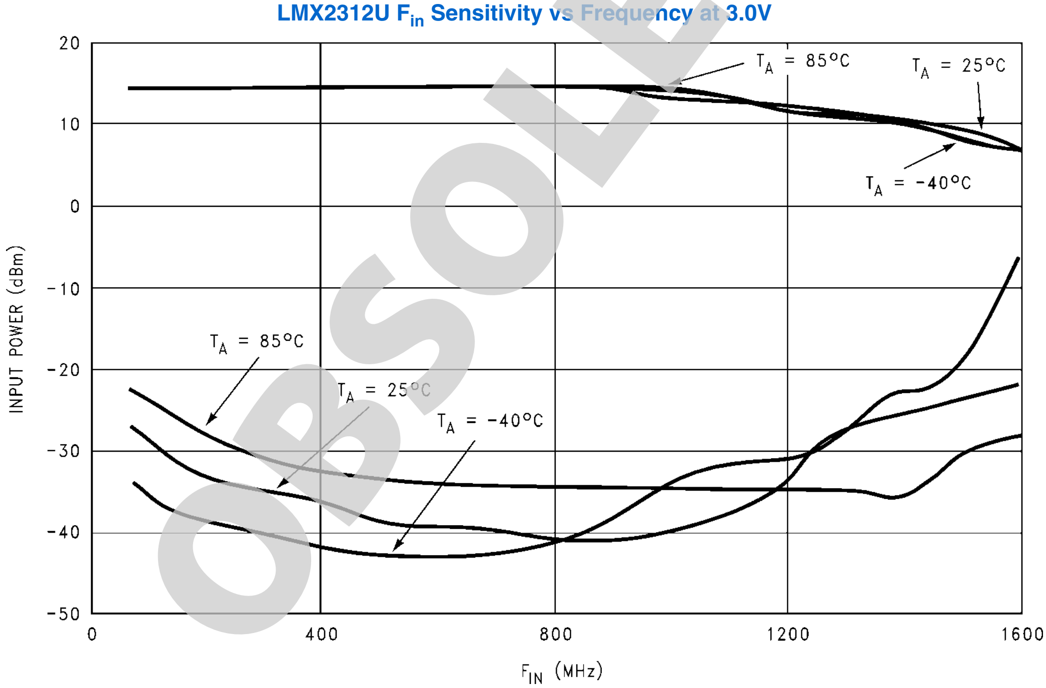
LMX2312U F_{in} Sensitivity vs Frequency at 3.0V



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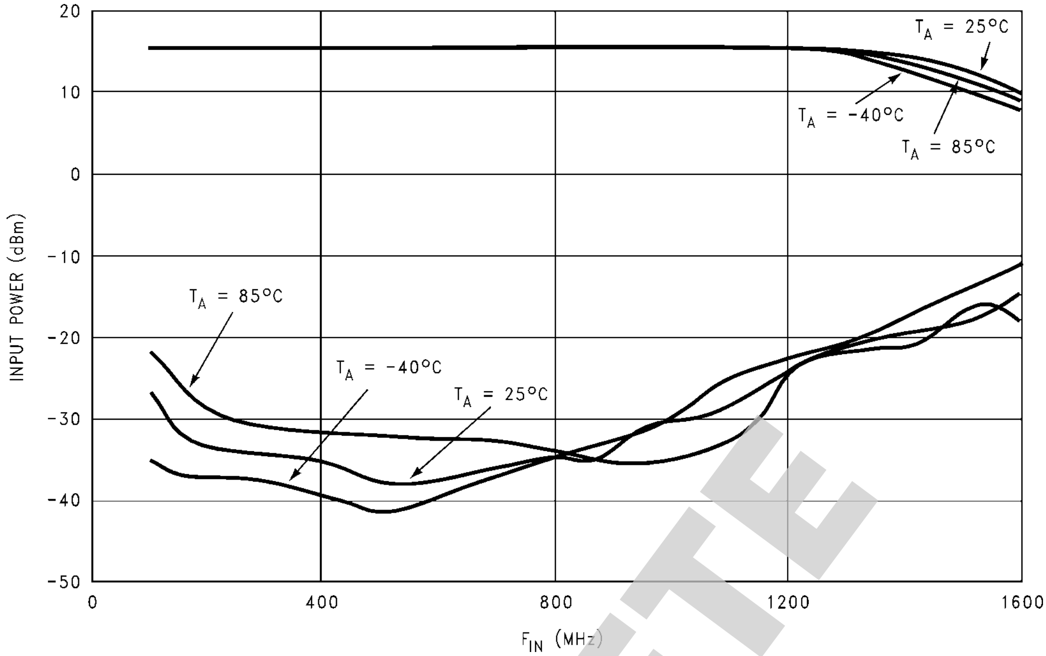
LMX2312U F_{in} Sensitivity vs Frequency at 5.5V



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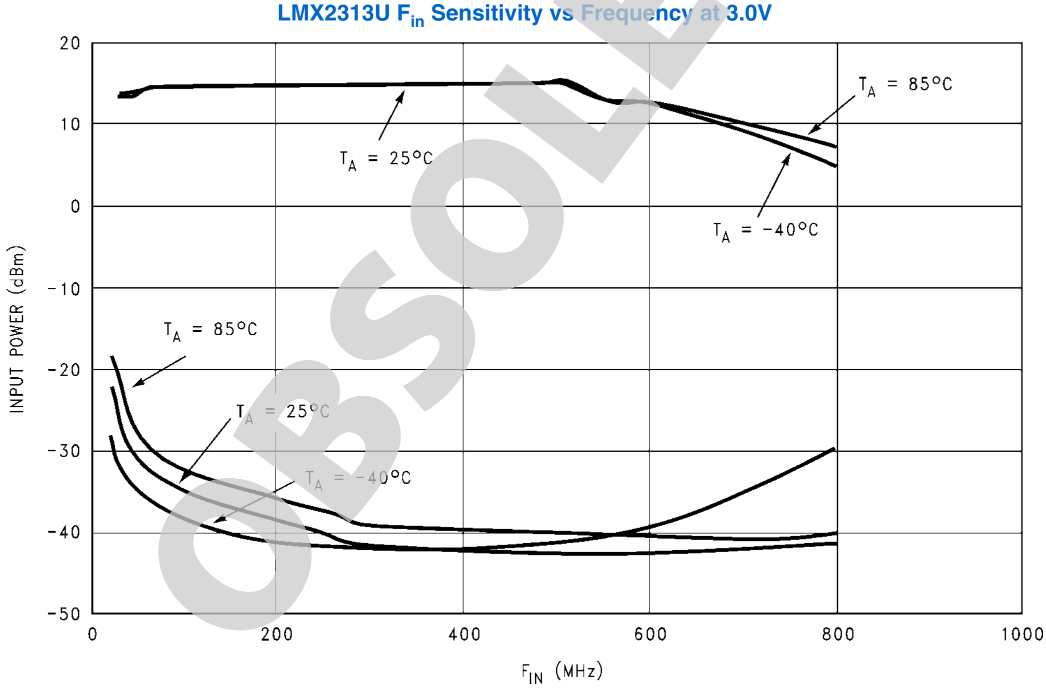
LMX2313U F_{in} Sensitivity vs Frequency at 3.0V



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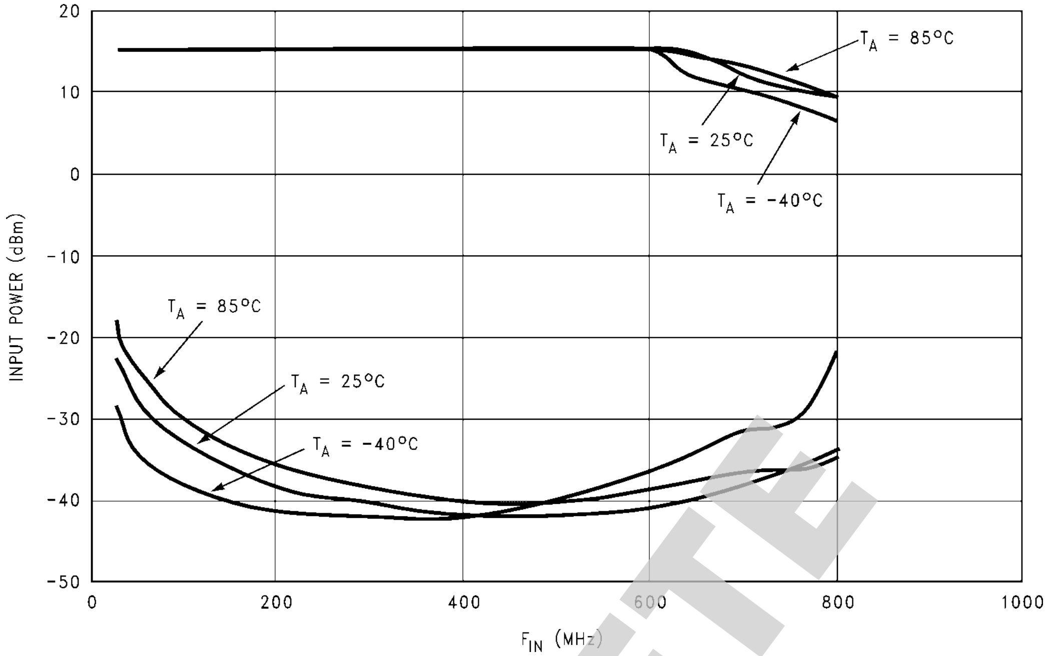
LMX2313U F_{in} Sensitivity vs Frequency at 5.5V



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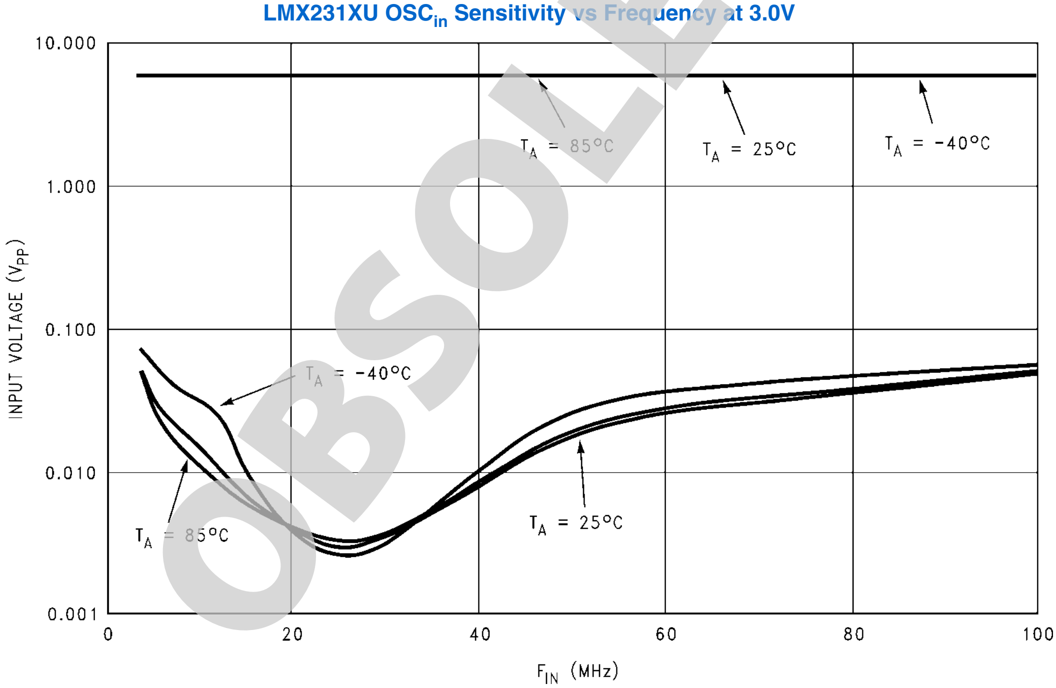
LMX231XU OSC_{in} Sensitivity vs Frequency at 3.0V



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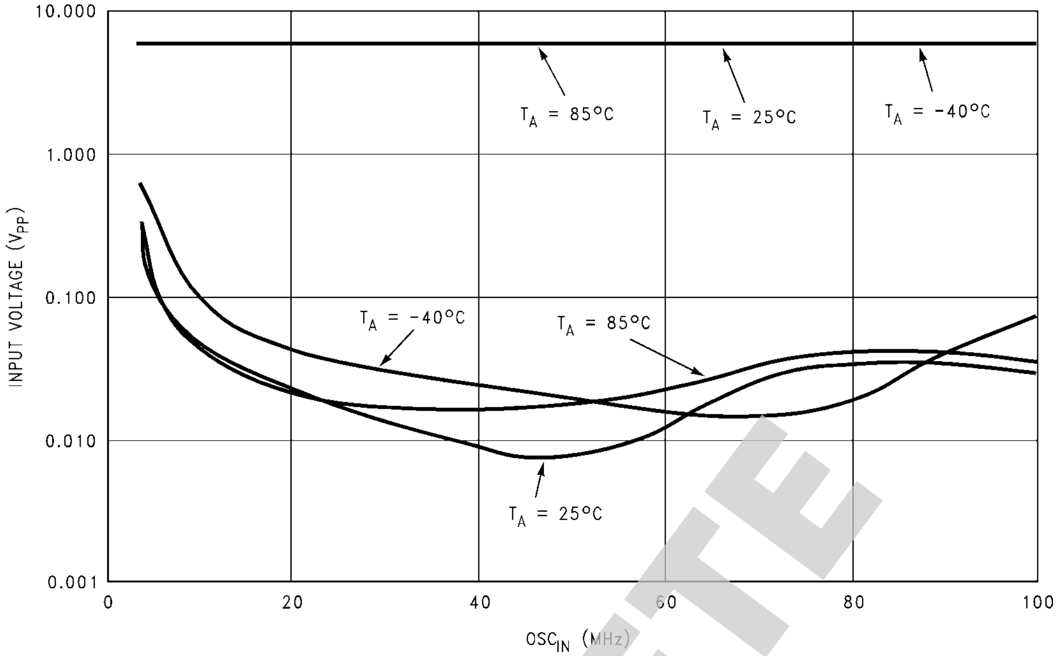
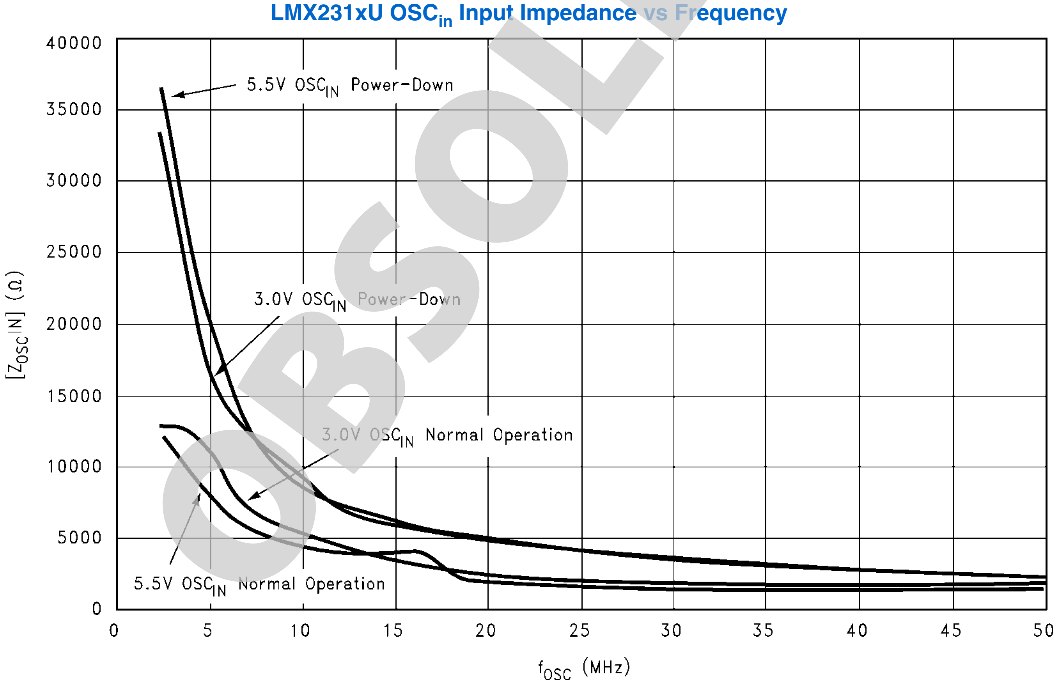
LMX231XU OSC$_{in}$ Sensitivity vs Frequency at 5.5V



20043855

LMX231xU OSC$_{in}$ Input Impedance vs Frequency



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LMX231xUSLD OSC_{IN} IMPEDANCE												
	V_{CC} = 3.0V (T_A = 25°C)						V_{CC} = 5.5V (T_A = 25°C)					
	OSC_{IN} BUFFER NORMAL OPERATION			OSC_{IN} BUFFER POWERED-DOWN MODE			OSC_{IN} BUFFER NORMAL OPERATION			OSC_{IN} BUFFER POWERED-DOWN MODE		
F_{OSC} (MHz)	Real $ZOSC_{IN}$ (Ω)	Imaginary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)	Real $ZOSC_{IN}$ (Ω)	Imaginary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)	Real $ZOSC_{IN}$ (Ω)	Imaginary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)	Real $ZOSC_{IN}$ (Ω)	Imaginary $ZOSC_{IN}$ (Ω)	$\|ZOSC_{IN}\|$ (Ω)
2	12900	−1500	13000	9000	−33000	34200	10000	−7400	12400	12000	−35000	37000
4	5200	−10900	12100	2000	−20000	20100	5500	−7800	9500	12200	−21000	24300
7	2400	−7500	7900	1100	−13000	13000	2700	−5700	6300	1300	−13000	13100
10	1350	−5400	5600	410	−9500	9500	1600	−4500	4800	800	−9100	9100
13	920	−4300	4400	350	−7000	7000	1000	−3500	3600	300	−7800	7800
16	820	−3600	3700	450	−5900	5900	800	−3900	4000	400	−6000	6000
19	630	−3100	3200	220	−5000	5000	630	−2500	2600	310	−5100	5100
22	570	−2600	2700	200	−4300	4300	540	−2100	2200	280	−4400	4400
25	420	−2100	2100	150	−3800	3800	450	−1900	2000	180	−3900	3900
28	440	−2000	2000	140	−3400	3400	400	−1700	1700	140	−3500	3500
31	390	−1900	1900	140	−3000	3000	350	−1500	1500	120	−3100	3100
34	360	−1800	1800	80	−2700	2700	330	−1400	1440	110	−2900	2900
37	340	−1700	1700	100	−2500	2500	310	−1300	1340	100	−2600	2600
40	330	−1500	1500	100	−2400	2400	300	−1200	1240	120	−2400	2400
43	300	−1400	1400	95	−2200	2200	280	−1100	1140	100	−2300	2300
46	290	−1400	1400	80	−2100	2100	270	−1000	1040	90	−2100	2100
49	280	−1300	1300	70	−1900	1900	260	−1000	1030	80	−2000	2000
50	280	−1300	1300	70	−1900	1900	260	−990	1020	100	−2000	2000

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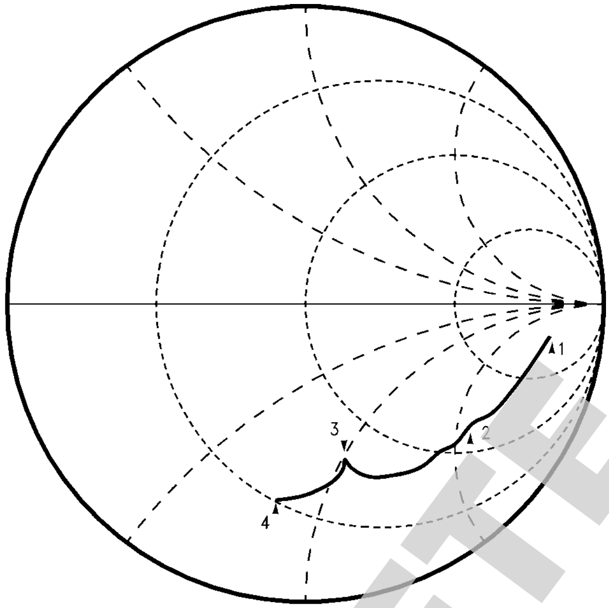
LMX231xU F_{in} Input Impedance vs Frequency
V_{CC} =3.0V, T_A = 25°C



Marker 1 = 100 MHz
Marker 2 = 1 GHz
Marker 3 = 2 GHz
Marker 4 = 2.5 GHz

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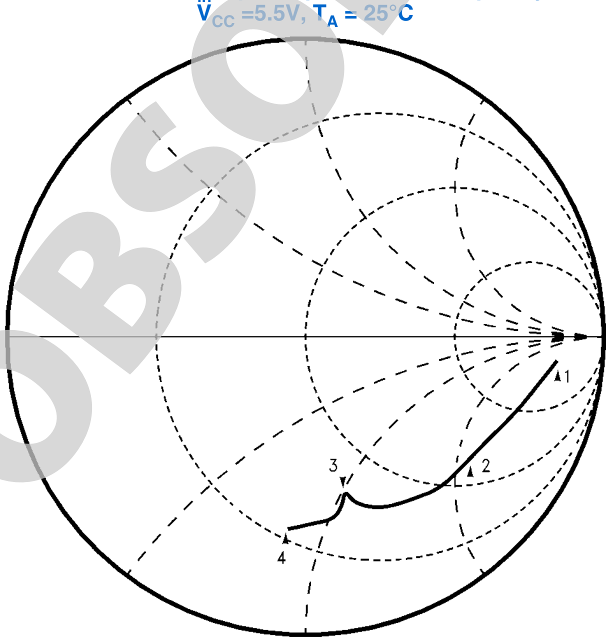
LMX231xU F_{in} Input Impedance vs Frequency
V_{CC} =5.5V, T_A = 25°C



Marker 1 = 100 MHz
Marker 2 = 1 GHz
Marker 3 = 2 GHz
Marker 4 = 2.5 GHz

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LMX231xUSLD F_{IN} IMPEDANCE

	V_{CC} = 3.0V (T_A = 25°C)						V_{CC} = 5.5V (T_A = 25°C)					
	F_{IN} POWERED-UP			F_{IN} POWERED-DOWN			F_{IN} POWERED-UP			F_{IN} POWERED-DOWN		
F_{IN} (MHz)	Real ZF_{IN} (Ω)	Imaginary ZF_{IN} (Ω)	$\lvert ZF_{IN}\rvert$ (Ω)	Real ZF_{IN} (Ω)	Imaginary ZF_{IN} (Ω)	$\lvert ZF_{IN}\rvert$ (Ω)	Real ZF_{IN} (Ω)	Imaginary ZF_{IN} (Ω)	$\lvert ZF_{IN}\rvert$ (Ω)	Real ZF_{IN} (Ω)	Imaginary ZF_{IN} (Ω)	$\lvert ZF_{IN}\rvert$ (Ω)
100	452	–325	557	440	–337	554	460	–325	563	444	–333	555
200	305	–278	413	300	–276	408	313	–277	418	312	–275	416
300	225	–243	331	225	–242	330	235	–244	339	237	–244	340
400	180	–219	283	179	–217	281	190	–221	291	189	–221	291
500	147	–197	246	145	–195	243	155	–200	253	155	–200	253
600	120	–175	212	118	–173	209	127	–179	219	126	–179	219
700	102	–158	188	100	–156	185	108	–162	195	107	–161	193
800	88	–141	166	86	–139	163	94	–146	174	91	–143	169
900	78	–126	148	75	–123	144	83	–131	155	81	–129	152
1000	73	–117	138	72	–113	134	78	–118	141	75	–116	138
1100	64	–109	126	63	–106	123	69	–112	132	68	–111	130
1200	57	–98	113	55	–95	110	61	–102	119	59	–100	116
1300	52	–90	104	52	–86	100	55	–95	110	55	–91	106
1400	46	–84	96	46	–83	95	49	–88	101	50	–87	100
1500	41	–75	85	40	–73	83	44	–79	90	42	–78	89
1600	39	–69	79	37	–66	76	41	–73	84	40	–70	81
1700	35	–61	70	34	–59	68	37	–65	75	36	–63	73
1800	34	–55	65	33	–52	62	35	–58	68	34	–56	66
1900	35	–50	61	35	–47	59	35	–52	63	35	–50	61
2000	37	–50	62	37	–48	61	38	–50	63	38	–48	61
2100	34	–52	62	33	–51	61	36	–52	63	34	–51	61
2200	29	–50	58	27	–48	55	32	–51	60	30	–50	58
2300	25	–48	54	23	–45	51	27	–50	57	25	–48	54
2400	20	–44	48	19	–42	46	23	–47	52	21	–44	49
2500	18	–41	45	16	–38	41	20	–43	47	18	–41	45

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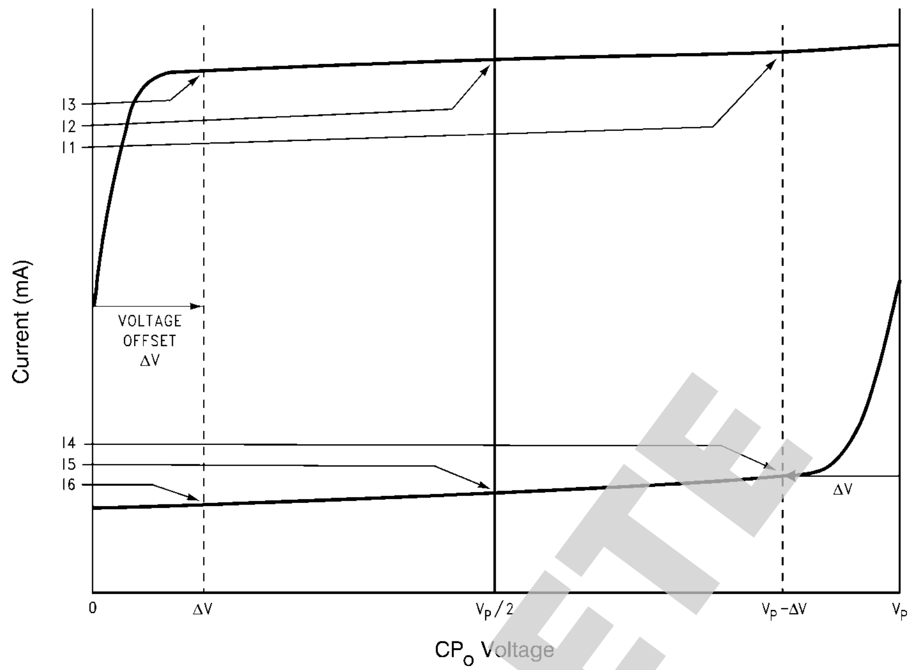
Charge Pump Measurement Definitions



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$I1 = CP_o$ sink current at $VCP_o = V_P - \Delta V$
$I2 = CP_o$ sink current at $VCP_o = V_P/2$
$I3 = CP_o$ sink current at $VCP_o = \Delta V$
$I4 = CP_o$ source current at $VCP_o = V_P - \Delta V$
$I5 = CP_o$ source current at $VCP_o = V_P/2$
$I6 = CP_o$ source current at $VCP_o = \Delta V$
$\Delta V = 0.5V$

Charge Pump Output Current Magnitude Variation Vs Charge Pump Output Voltage

$$ICP_o \text{ Vs } VCP_o = \frac{\frac{1}{2}(|I1| - |I3|)}{\frac{1}{2}(|I1| + |I3|)} \times 100\%$$

$$= \frac{\frac{1}{2}(|I4| - |I6|)}{\frac{1}{2}(|I4| + |I6|)} \times 100\%$$

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Charge Pump Output Current Sink Vs Charge Pump Output Current Source Mismatch

$$ICP_o \text{ SINK Vs } ICP_o \text{ SOURCE} = \frac{|I2| - |I5|}{\frac{1}{2}(|I2| + |I5|)} \times 100\%$$

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Charge Pump Output Current Magnitude Variation Vs Temperature

$$ICP_o \text{ Vs } T_A = \frac{|I_2|\big|_{T_A} - |I_2|\big|_{T_A = 25°C}}{|I_2|\big|_{T_A = 25°C}} \times 100\%$$

$$= \frac{|I_5|\big|_{T_A} - |I_5|\big|_{T_A = 25°C}}{|I_5|\big|_{T_A = 25°C}} \times 100\%$$

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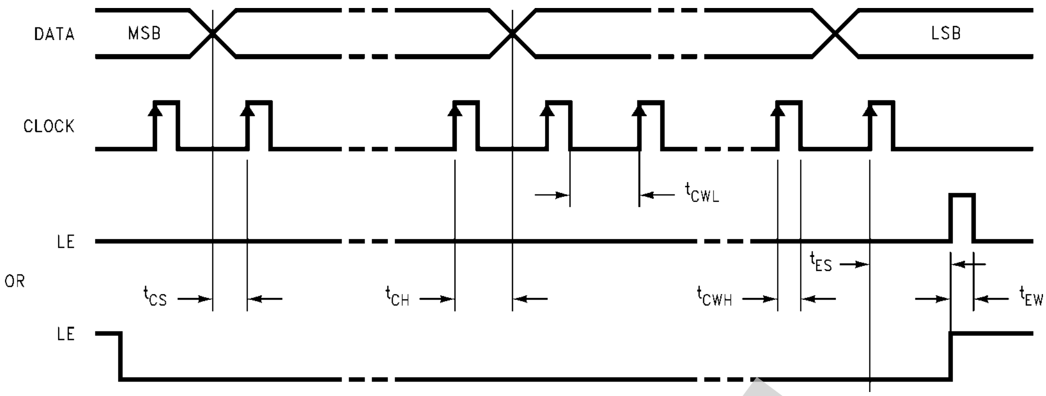
Serial Data Input Timing

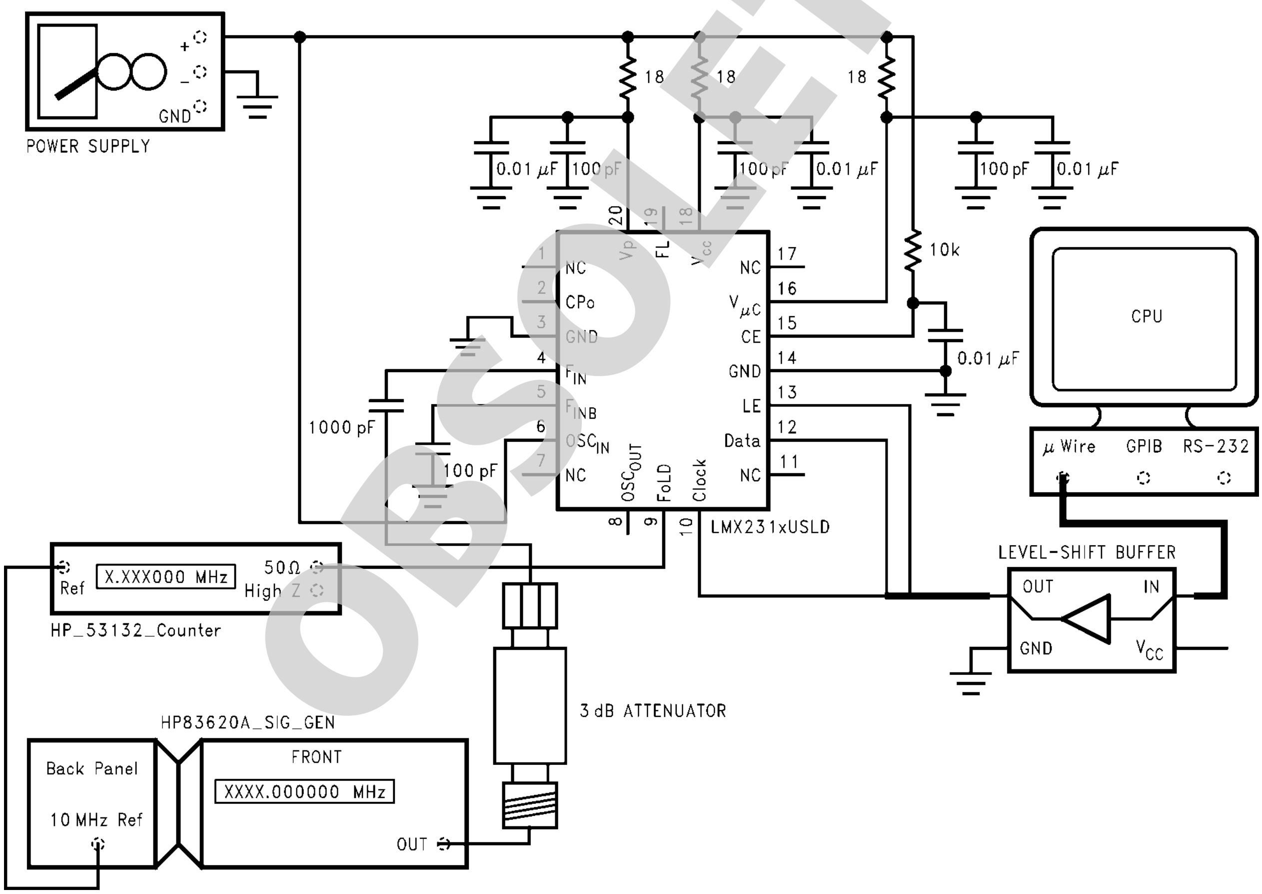


20043810

Notes:

1. Data shifted into register on Clock rising edge.
2. Data is shifted in MSB first.

F_{IN} Sensitivity Test Setup



20043830

Notes:

1. LMX2310/1/2U Test Conditions: NA_CNTR = 16, NB_CNTR = 312, P = 1, FoLD2 = 1, FoLD1 = 1, FoLD0 = 0, PWDN = 0.
2. LMX2313U Test Conditions: NA_CNTR = 0, NB_CNTR = 625, P = 1, FoLD2 = 1, FoLD1 = 1, FoLD0 = 0, PWDN = 0.
3. Sensitivity limit is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz.

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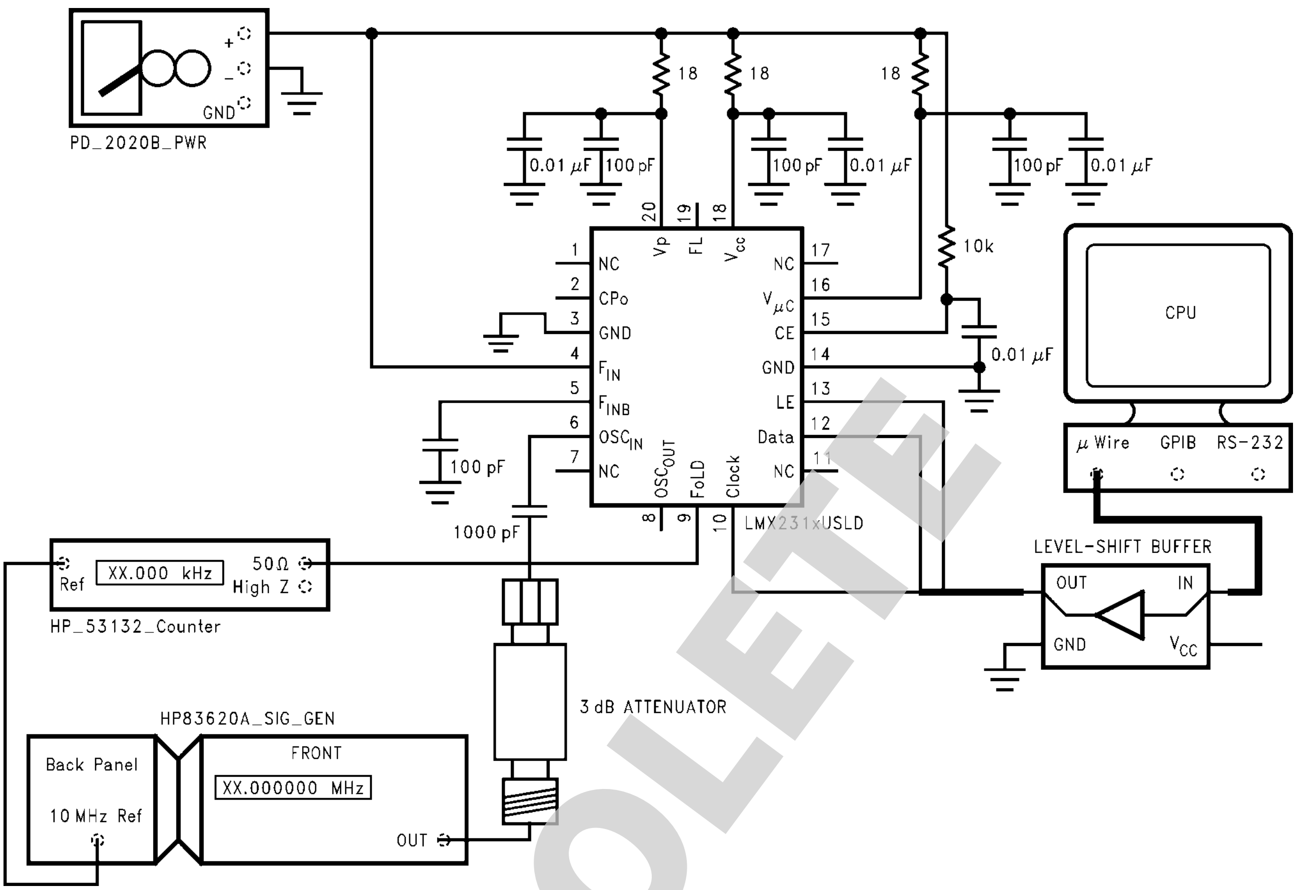
OSC_{IN} Sensitivity Test Setup



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Notes:

1. Test Conditions: R_CNTR = 1000, FoLD2 = 1, FoLD1 = 0, FoLD0 = 1, PWDN = 0.
2. Sensitivity limit is reached when the frequency error of the divided RF input is greater than or equal to 1 Hz.

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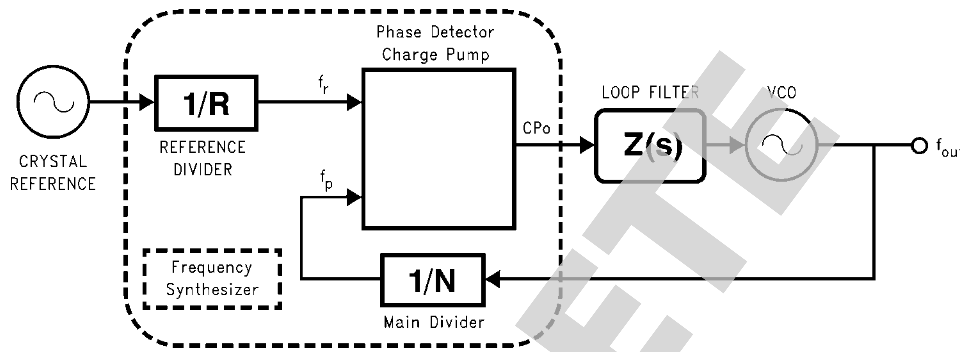
1.0 Functional Description

The basic phase-lock-loop (PLL) configuration consists of a high-stability crystal reference oscillator, a frequency synthesizer such as the National Semiconductor LMX2310/1/2/3U, a voltage controlled oscillator (VCO), and a passive loop filter. The frequency synthesizer includes a phase detector, a current mode charge pump, as well as a programmable reference divider and feedback frequency divider. The VCO frequency is established by dividing the crystal reference signal down via the reference divider to obtain a frequency that sets the comparison frequency. This reference signal, f_r, is then presented to the input of a phase/frequency detector and compared with another signal, f_p, which was obtained by dividing the VCO frequency down by way of the feedback counter. The phase/frequency detector measures the phase error between the f_r and f_p signals and outputs control signals that are directly proportional to the phase error. The charge pump then pumps charge into or out of the loop filter based on the magnitude and direction of the phase error. The loop filter converts the charge into a stable control voltage for the VCO. The phase/frequency detector's function is to adjust the voltage presented to the VCO until the feedback signal's frequency and phase match that of the reference signal. When this "phase-locked" condition exists, the RF VCO frequency will be N times that of the comparison frequency, where N is the feedback divider ratio.



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1.1 REFERENCE OSCILLATOR

The reference oscillator frequency for the RF PLL is provided from the external source via the OSC_{in} pin. The low noise reference buffer circuit supports frequencies from 2 MHz to 50 MHz with a minimum input sensitivity of 0.5 V_{pp}. The input can be driven from an external CMOS or TTL logic gate. The output of this buffer drives the R COUNTER. The output of the buffer also connects to an oscillator/buffer circuit. Its output connects to the OSC_{out} pin. The oscillator/buffer circuit can be used as a buffer to provide the reference frequency to other circuitry. It can also be used as an oscillator with a crystal/resonator with proper components connected between OSC_{in} and OSC_{out} pins to generate a reference frequency.

1.2 REFERENCE DIVIDER (R COUNTER)

The reference divider is comprised of a 15-bit CMOS binary counter that supports a continuous integer divide range from 2 to 32,767. The divide ratio should be chosen such that the maximum phase comparison frequency of 10 MHz is not exceeded. The reference divider circuit is clocked by the output of the reference buffer circuit. The output of the reference divider circuit feeds the reference input of the phase detector circuit. The frequency of the reference input to the phase detector (also referred to as the comparison frequency) is equal to reference oscillator frequency divided by the reference divider ratio. Refer to Section 3.2.1 for details on programming the R COUNTER.

1.3 PRESCALERS

The LMX2310/1/2U contains a selectable, dual modulus 32/33 and 16/17 prescaler. The LMX2313U contains a selectable, dual modulus 16/17 and 8/9 prescaler.

PLL Input Frequency	PLL Part Numbers	Allowable Prescaler Values
F_{IN} > 1.2 GHz	LMX2310/1U	32/33
F_{IN} ≤ 1.2 GHz	LMX2310/1/2U	16/17 or 32/33
F_{IN} ≤ 600 MHz	LMX2313U	8/9 or 16/17

The complimentary F_{IN} and F_{INB} input pins drive the input of a bipolar, differential-pair amplifier. The output of the bipolar, differential-pair amplifier drives a chain of ECL D-type flip-flops in a dual modulus configuration. The output of the prescaler is used to clock the subsequent programmable feedback divider. Refer to Section 3.3.2 for details on programming the Prescaler Value.

1.4 FEEDBACK DIVIDER (N COUNTER)

The N COUNTER is clocked by the output of the prescaler. The N COUNTER is composed of a 13-bit programmable integer divider. The 5-bit swallow counter is part of the prescaler. Selecting a 32/33 prescaler provides a minimum continuous divider range from 992 to 262,143 while selecting a 16/17 prescaler value allows for continuous divider values from 240 to 131,071. In the LMX2313U, selecting a 8/9 prescaler provides a minimum continuous divider range from 56 to 65535.

N = (P x NB_CNTR) + NA_CNTR	
$F_{IN} = N \times F_{\varphi}$	
Definitions	
F_{φ}	Phase Detector Comparison Frequency
F_{IN}	RF Input Frequency
P	Prescaler Value
NA_CNTR	A Counter Value
NB_CNTR	B Counter Value

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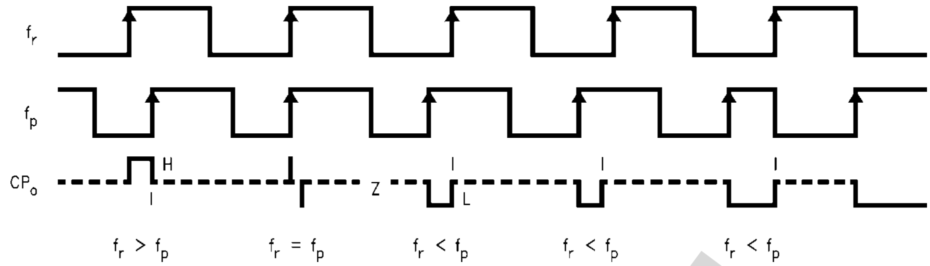
1.5 PHASE/FREQUENCY DETECTORS

The phase/frequency detector is driven from the N and R COUNTER outputs. The maximum frequency at the phase detector inputs is 10 MHz. The phase detector outputs control the charge pump. The polarity of the pump-up or pump-down control signals are programmed using the PD_POL control bit, depending on whether the RF VCO tuning characteristics are positive or negative (see programming description in Section 3.2.2). The phase/frequency detector has a detection range of −2π to +2π.

Phase Comparator and Internal Charge Pump Characteristics



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Note 13: The minimum width of the pump up and pump down current pulses occur at the CP_o pin when the loop is phase-locked.

Note 14: The diagram assumes that PD_POL = 1

Note 15: f_r is the phase comparator input from the R Divider

Note 16: f_p is the phase comparator input from the N Divider

Note 17: CP_o is charge pump output

1.6 CHARGE PUMP

The charge pumps directs charge into or out of an external loop filter. The loop filter converts the charge into a stable control voltage which is applied to the tuning input of a VCO. The charge pump steers the VCO control voltage towards V_P during pump-up events and towards GND during pump-down events. When locked, CP_o is primarily in a TRI-STATE condition with small corrections occurring at the phase comparison rate. The charge pump output current magnitude can be selected as 1.0 mA or 4.0 mA by programming the ICPo_4X bits. When TO_CNTR[11:0] = 1, the charge pump output current magnitude is set to 4.0 mA. Refer to Section 3.2.3 and 3.4.2 for details on programming the charge pump output current magnitude.

1.7 MICROWIRE SERIAL INTERFACE

The programmable register set is accessed through the MICROWIRE serial interface. The interface is comprised of three signal pins: CLOCK, DATA and LE (Latch Enable). The MICROWIRE circuitry is referenced to $V_{\mu C}$, which allows the circuitry to operate down to a 1.72V source. Serial data is clocked into a 22-bit shift register from DATA on the rising edge of CLOCK. The serial data is clocked in MSB first. The last two bits decode the internal register address. On the rising edge of LE, the data stored in the shift register is loaded into one of the three latches based on the address bits. The synthesizer can be programmed even in the power-down state. A complete programming description is in Section 3.0.

1.8 MULTI-FUNCTION OUTPUTS

The LMX2310/1/2/3U FoLD output pin is a multi-function output that can be configured as an analog lock detect, a digital lock detect, and a monitor of the output of the reference divider and the feedback divider circuits. The FoLD output pin is referenced to the $V_{\mu C}$ supply. The FoLD0, FoLD1 and FoLD2 bits are used to select the desired output function. A complete programming description of the FoLD output pin is in Section 3.2.5.

1.8.1 Analog Lock Detect

When programmed for analog lock detect, the analog lock detect status is available on the FoLD output pin. When the charge pump is inactive, the lock detect output goes to a high impedance in the open drain configuration and to a $V_{\mu C}$ source in a push-pull configuration. It goes low when the charge pump is active during a comparison cycle. The analog lock detect status can be programmed in either an open drain or push-pull configuration. The push-pull output is referenced to $V_{\mu C}$.

1.8.2 Digital Lock Detect

When programmed for digital lock detect, the digital lock detect status is available on the FoLD pin. The digital lock detect filter compares the phase difference of the inputs from the phase detector to a RC generated delay of approximately 15 ns. To enter the locked state (LD = High), the phase error must be less than the 15 ns RC delay for 5 consecutive reference cycles. Once in lock, the RC delay is changed to approximately 30 ns. To exit the locked state, the phase error must be greater than the 30 ns RC delay. When a PLL is in power-down mode, the respective lock detect output is always low. A flow chart of the digital lock detect filter follows:

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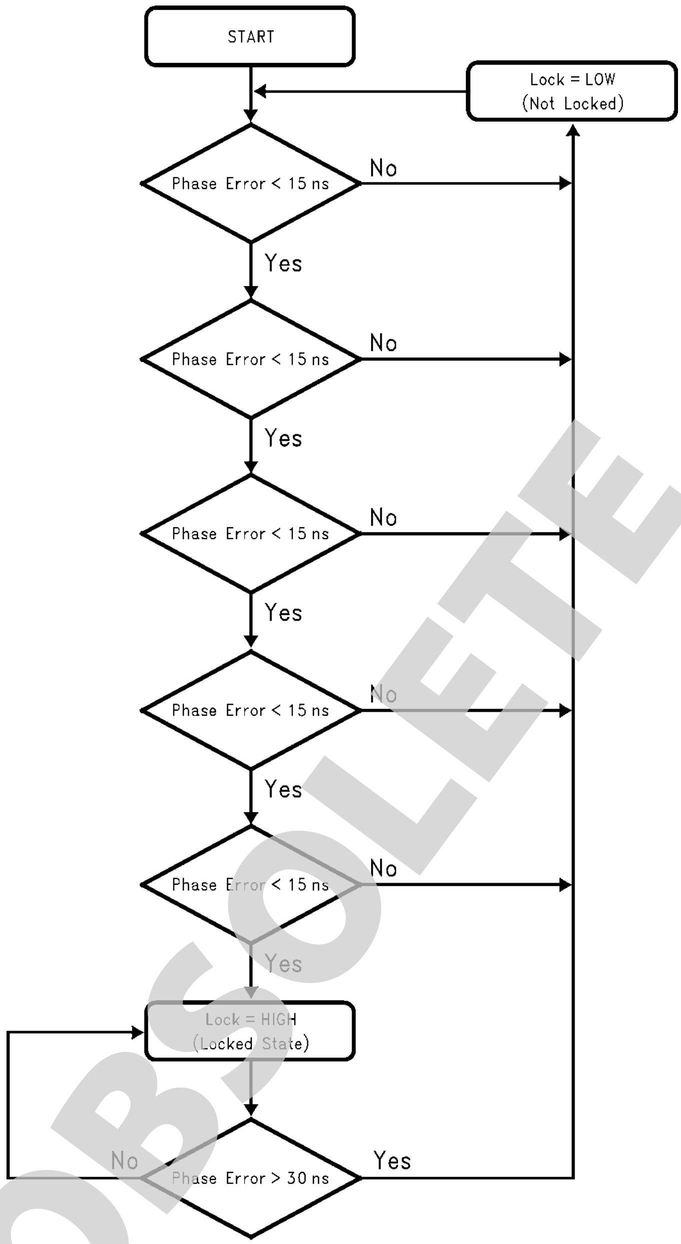

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1.9 Fastlock™ OUTPUT

The FL pin can be used as the Fastlock output. The FL pin can also be programmed as constant low, constant high (referenced to V_{CC}), or constant high impedance, selectable through the T register. When the device is configured in Fastlock mode, the charge pump current can be increased 4x while maintaining loop stability by synchronously switching a parallel loop filter resistor to ground with the FL pin, resulting in a ~2x increase in loop bandwidth. The loop bandwidth, the zero gain crossover point of the open loop gain, is effectively shifted up in frequency by a factor of the square root of 4 = 2 during Fastlock mode. For $\omega' = 2\,\omega$, the phase margin during Fastlock also will remain constant. The user calculates the loop filter component values for the normal steady state considerations. The device configuration ensures that as long as a second resistor, equal to the primary resistor value, is wired in appropriately, the loop will lock faster without any additional stability considerations.

The PLL can be configured to be in either the Fastlock mode continuously or in the Fastlock mode that uses a timeout counter to switch it back to the normal mode. In the Fastlock mode the charge pump current is set to 4 mA and the FL pin is set low. If the user sets the PLL to be in the Fastlock mode continuously he can send the R register with CPo_4X set low (R[18] = 0) and sets TO_CNTR[11:0] to 1. The user can set the PLL to normal mode (1 mA mode and set the FL pin to TRI-STATE mode) by programming TO_CNTR[11:0] to 0. If the user elects to use the timeout counter, he can program the timeout counter from 4 to 4095. The timeout counter will count down the programmed number of phase detector reference cycles. After the programmed number of phase detector reference cycles is reached, it will automatically set the charge pump current to the 1 mA mode and set the FL pin to TRI-STATE mode. A complete programming description is in Section 3.4.2.

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2.0 Power-Down

The LMX2310/1/2/3U are power controlled through logical control of the CE pin in conjunction with programming of the PDWN and CPo_TRI bits. A truth table is provided that describes how the state of the CE pin, the PDWN bit and CPo_TRI bit set the operating mode of the device. A complete programming description of Power-Down is provided in Section 3.3.1.

CE	PWDN	CPo_TRI	Operating Mode
0	X	X	Power-down (Asynchronous)
1	0	0	Normal Operation
1	1	0	Power-down (Synchronous)
1	1	1	Power-down (Asynchronous)

X = Don't Care

When the device enters the power-down mode, the oscillator buffer, RF prescaler, phase detector, and charge pump circuits are all disabled. The OSC_{IN}, CPo, F_{IN}, F_{INB}, LD pins are all forced to a high impedance state. The reference divider and feedback divider circuits are disabled and held at the load point during power-down. When the device is programmed to normal operation, the oscillator buffer, RF prescaler, phase detector, and charge pump circuits are all powered on. The feedback divider and the reference divider are held at the load point. This allows the RF prescaler, feedback divider, reference oscillator, the reference divider and prescaler circuitry to reach proper bias levels. After a 1.5 µs delay, the feedback and reference divider are enabled and they resume counting in "close" alignment (The maximum error is one prescaler cycle). The MICROWIRE control register remains active and capable of loading and latching in data while in the power-down mode.

The synchronous power-down function is gated by the charge pump. When the device is configured for synchronous power-down, the device will enter the power-down mode upon the completion of the next charge pump pulse event.

The asynchronous power-down function is NOT gated by the completion of a charge pump pulse event. When the device is configured for asynchronous power-down, the part will go into power-down mode immediately.

3.0 Programming Description

3.1 MICROWIRE INTERFACE

The MICROWIRE interface is comprised of a 22-bit shift register and three control registers. The shift register consists of a 20-bit DATA field and a 2-bit address (ADDR) field as shown below. Data is loaded into the shift register on the rising edges of the CLOCK signal MSB first. When Latch Enable transitions HIGH, data stored in the shift register is loaded into either the R, N or T register depending on the state of the ADDR bit. The DATA field assignments for the R, N and T registers are shown in Section 3.1.1.

MSB	LSB
DATA	ADDRESS
21 2	0

ADDR	Target Register
0	R register
1	N register
2	T register

3.1.1 Register Map

Register	Most Significant Bit							SHIFT REGISTER BIT LOCATION									Least Significant Bit					
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
R	FoLD1	FoLD0	CPo_ TRI	CP0_ 4x	PD_ POL	R_CNTR[14:0]															0	0
N	PWDN	P	B_CNTR[12:0]													A_CNTR[4:0]					0	1
T	0	0	0	0	0	0	0	FoLD2	TO_CNTR[11:0]												1	0

3.2 R REGISTER

The R register contains the R_CNTR control word and PD_POL, CPo_4X, CP_TRI, FoLD0, FoLD1 control bits. The detailed descriptions and programming information for each control word is discussed in the following sections.

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Register	Most Significant Bit				SHIFT REGISTER BIT LOCATION															Least Significant Bit	
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
R	FoLD1	FoLD0	CPo_TRI	CPo_4X	PD_POL	R_CNTR[14:0]															0	0

3.2.1 R_CNTR[14:0] Reference Divider (R COUNTER) R[16:2]

The reference divider can be programmed to support divide ratios from 2 to 32,767. Divide ratios of less than 2 are prohibited.

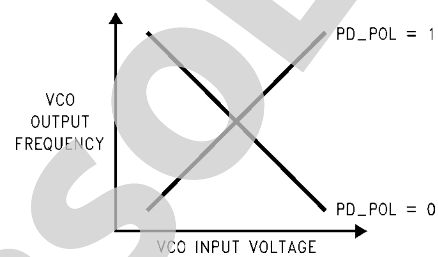
Divider Value	R_CNTR[14:0]														
2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32,767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

3.2.2 PD_POL Phase Detector Polarity R[17]

The PD_POL control bit is used to set the polarity of the phase detector based on the VCO tuning characteristic.

Control Bit	Register Location	Description	Function	
			0	1
PD_POL	R[17]	Phase Detector Polarity	Negative VCO Tuning Characteristic	Positive VCO Tuning Characteristic

VCO Characteristics



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3.2.3 CPo_4X Charge Pump Output Current R[18]

The CPo_4X control bit allows the charge pump output current magnitude to be switched from 1 mA to 4 mA. This happens asynchronously or immediately with the change in CPo_4X bit.

Control Bit	Register Location	Description	Function	
			0	1
CPo_4X	R[18]	Charge Pump Output Current Magnitude	1X Current	4X Current

3.2.4 CPo_TRI Charge Pump TRI-STATE R[19]

The CPo_TRI control bit allows the charge pump to be switched between a normal operating mode and a high impedance output state. This happens asynchronously or immediately with the change in CPo_TRI bit.

Control Bit	Register Location	Description	Function	
			0	1
CPo_TRI	R[19]	Charge Pump TRI-STATE	Charge Pump Operates Normal	Charge Pump Output in High Impedance State

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3.2.5 FoLD2,1,0 FoLD Output Truth Table T[14],R[21],R[20]

The FoLD2, FoLD1 and FoLD0 are used to select which signal is routed to FoLD pin.

T[14]	R[21]	R[20]	FoLD Output State
FoLD2	FoLD1	FoLD0	
0	0	0	Disabled (TRI-STATE FoLD)
0	0	1	Lock Detect—Analog (Push/Pull), Reference to $V_{\mu c}$
0	1	0	Lock Detect—Analog (Open Drain)
0	1	1	Reset R and N Dividers and TRI-STATE Charge Pump
1	0	0	Lock Detect—Digital (Push/Pull), Reference to $V_{\mu C}$
1	0	1	R COUNTER Output (Push/Pull), Reference to $V_{\mu C}$
1	1	0	N Counter Output (Push/Pull), Reference to $V_{\mu C}$
1	1	1	Reserved (Do Not Use)

3.3 N REGISTER

The N register contains the PWDN (Power-Down), P (Prescaler), NA_CNTR, and NB_CNTR control words. The detailed descriptions and programming information for each control word is discussed in the following sections.

Register	Most Significant Bit							SHIFT REGISTER BIT LOCATION												Least Significant Bit	
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
N	PWDN	P	B_CNTR[12:0]													A_CNTR[4:0]					0	1

3.3.1 PWDN Power-Down N[21]

The PWDN control bit along with CP_{o}_TRI control bit is used to power-down the PLL. The LMX2310/1/2/3U can be synchronous or asynchronous powered down by first setting the CP_{o}_TRI bit and then setting the PWDN bit. To power up from the synchronous Power-Down mode, the CP_{o}_TRI bit will have to be reset to 0.

N[21]	R[19]	Operating Mode
PWDN	CP_{o}_TRI	
0	0	Normal Operation
1	0	Power-down (Synchronous)
1	1	Power-down (Asynchronous)

3.3.2 P Prescaler N[20]

The LMX2310/1/2/3U contains two dual modulus prescalers. The P control bit is used to set the prescaler value.

N[20]	Prescaler Value LMX2310/1/2U	Prescaler Value LMX2313U
0	16/17	8/9
1	32/33	16/17

PLL Input Frequency	Allowable Prescaler Values
F_{IN} > 1.2 GHz	32/33
$F_{IN} \leq$ 1.2 GHz	16/17 or 32/33
$F_{IN} \leq$ 600 MHz	8/9 or 16/17

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3.3.3 B_CNTR[12:0] B COUNTER N[19:7]

The NB_CNTR control word is used to program the B counter. The B counter is a 13-bit binary counter used in the programmable feedback divider. The B counter can be programmed to values ranging from 3 to 8,191. See Section 1.4 for details on how the value of the B counter should be selected.

Divider Value	B_CNTR[12:0]												
3	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	1	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•
8,191	1	1	1	1	1	1	1	1	1	1	1	1	1

NOTE: B counter divide ratio must be ≥ 3.

3.3.4 A_CNTR[4:0] A Counter N[6:2]

The NA_CNTR control word is used to program the A counter. The A counter is a 5-bit swallow counter used in the programmable feedback divider. The A counter can be programmed to values ranging from 0 to 31. See Section 1.4 for details on how the value of the A counter should be selected.

Divide Ratio	A_CNTR[4:0]				
0	0	0	0	0	0
1	0	0	0	0	1
•	•	•	•	•	•
31	1	1	1	1	1

NOTES: A counter divide ratio must be ≤ P and A counter divide ratio must be ≤ B counter divide ratio.

3.4 T REGISTER

The T register contains the TO_CNTR control word and FoLD2 control bit. The detailed descriptions and programming information for each control word is discussed in the following sections.

Register	Most Significant Bit							SHIFT REGISTER BIT LOCATION										Least Significant Bit				
	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Data Field																				*Address Field*	
T	0	0	0	0	0	0	0	FoLD2	TO_CNTR[11:0]												1	0

3.4.1 FoLD2 FoLD Output (P/O Output Truth Table) T[14]

See Section 3.2.5 for FoLD Output Truth Table details.

3.4.2 TO_CNTR[11:0] Timeout Counter Table T[13:2]

When the Fastlock Timeout counter (TO_CNTR) is loaded with 0, Fastlock is off, the FL pin will be in TRI-STATE mode, and the charge pump current will be the value specified by the Charge Pump Magnitude bit, R[18]. When the Timeout counter is loaded with 1, the FL pin is 0 (pulled low) and the charge pump current will be at the 4X state. When the Timeout counter is loaded with 2, the FL pin will again be set to 0 (pulled low), but the charge pump current will be controlled by R[18]. When the Timeout counter is loaded with 3, the FL pin is 1 (pulled high) with the charge pump current will be controlled by R[18]. When loaded with 4 through 4095, Fastlock is active and will time-out after the specified number of phase detector events.

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Count	TO_CNTR[11:0]												Notes
FL Pin Forced TRI-STATE	0	0	0	0	0	0	0	0	0	0	0	0	C_P current controlled by R[18]
FL Pin Forced Low	0	0	0	0	0	0	0	0	0	0	0	1	C_P = 4 mA (manual Fastlock mode)
FL Pin Forced Low	0	0	0	0	0	0	0	0	0	0	1	0	C_P current controlled by R[18]
FL Pin Forced High	0	0	0	0	0	0	0	0	0	0	1	1	C_P current controlled by R[18]
Min Count (4)	0	0	0	0	0	0	0	0	0	1	0	0	C_P Current set to 4 mA, switches to 1 mA when count reaches 0
•	•	•	•	•	•	•	•	•	•	•	•	•	
Max Count (4095)	1	1	1	1	1	1	1	1	1	1	1	1	

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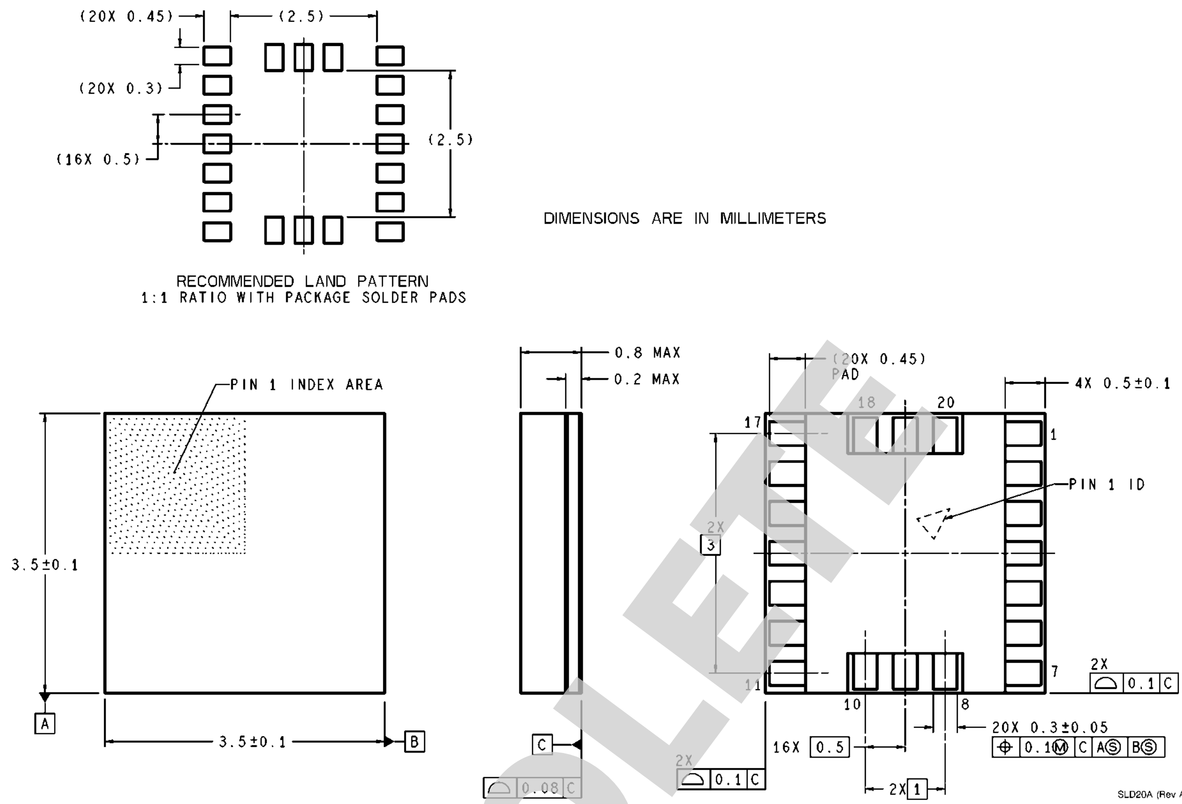
Physical Dimensions inches (millimeters) unless otherwise noted



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Notes

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Notes

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