

# CIC61508

Functional Safety Companion Chip

Data Sheet

V1.2 2011-06

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# CIC61508

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**CIC61508 Data Sheet****Revision History: V1.2 2011-06**

Previous Versions: V1.0, V1.1

Page	Subjects (major changes since last revision)
<b>20</b>	Typical SPI timing parameters are replaced by limit values.

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# 1 Overview

## 1.1 Features

The CIC61508 has the following features:

- Power supply monitor for over- and under-voltage
- Sequencer
- Task monitor
- Data comparison and verification functions
- SPI communication monitor
- Safety path control (enable/disable)
- Configurable Wake-Up Timer
- Wide range of voltage supply supported (3.3V or 5.0V +/-10%)
- TSSOP-38 package available

## 1.2 Ordering Information

For the available ordering codes for the CIC61508, please refer to your responsible sales representative or your local distributor.

This document describes the device types shown in [Table 1-1](#).

**Table 1-1** CIC61508 Device Types

Device Type	Power Supply	Ambient Temperature Range
SAA-CIC61508-OSRF 5V	5.0 V	-40 to 140 °C
SAA-CIC61508-OSRF 3V	3.3 V	-40 to 140 °C

## 1.3 Functional Summary

The CIC61508 is a Companion Safety Monitor Chip to build up functional safety applications; examples include airbag, Electrical Powered Steering (EPS) and damping systems. The chip is responsible for monitoring the host microcontroller's behaviour. It can monitor the host microcontroller's power supply and verify the host microcontroller's requests. It therefore serves as an independent diagnostic monitoring device to allow the host microcontroller system to be SIL3 approved.

## 1.4 Pin Configuration

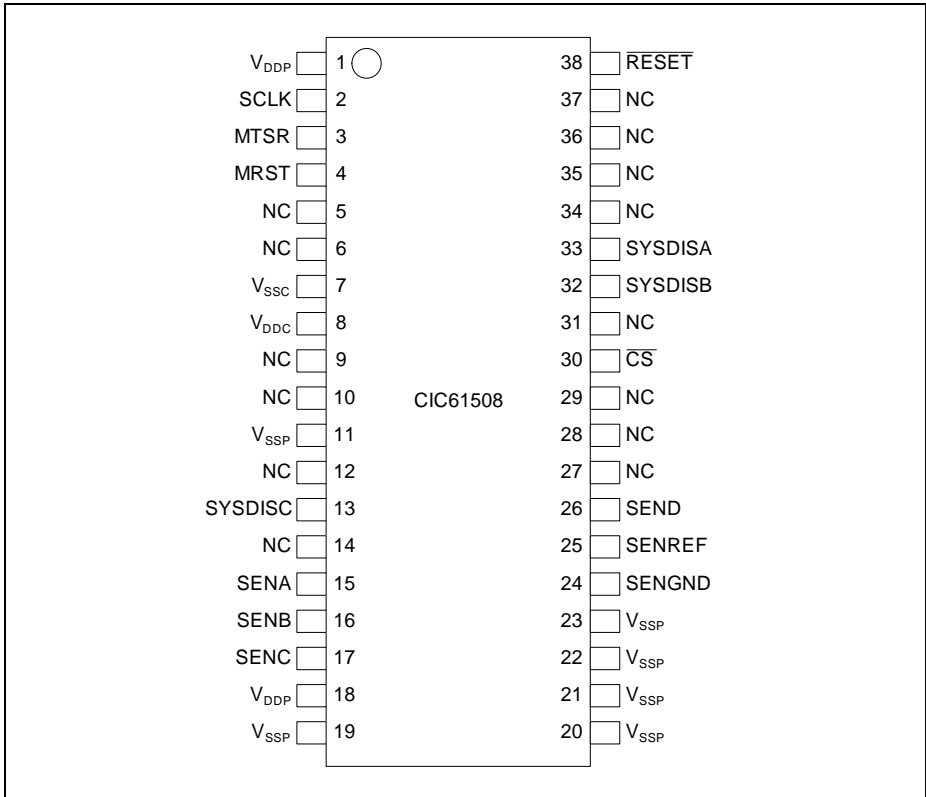


Figure 1-1 CIC61508 Pinout (PG-TSSOP-38)

Table 1-2 Pin Definitions and Functions (PG-TSSOP-38)

Pin Number	Type	Reset State <sup>1)</sup>	Symbol	Function
1	-	-	V <sub>DDP</sub>	Voltage Supply
2	I	Hi-Z	SCLK	SPI Clock
3	I	Hi-Z	MTSR	SPI Input
4	O	Hi-Z	MRST	SPI Output
5	-	-	NC	Not connected

**Table 1-2 Pin Definitions and Functions (PG-TSSOP-38)**

Pin Number	Type	Reset State <sup>1)</sup>	Symbol	Function
6	-	-	NC	Not connected
7	-	-	V <sub>SSC</sub>	Supply Ground (Digital)
8	-	-	V <sub>DDC</sub>	Core Supply Monitor
9	-	-	NC	Not connected
10	-	-	NC	Not connected
11	-	-	V <sub>SSP</sub>	Supply Ground
12	-	-	NC	Not connected
13	O	PU	SYSDISC	System Disable C
14	-	-	NC	Not connected
15	I	Hi-Z	SENA	Analog Input A
16	I	Hi-Z	SENB	Analog Input B
17	I	Hi-Z	SENC	Analog Input C
18	-	-	V <sub>DDP</sub>	Voltage Supply
19	-	-	V <sub>SSP</sub>	Supply Ground
20	-	-	V <sub>SSP</sub>	Supply Ground
21	-	-	V <sub>SSP</sub>	Supply Ground
22	-	-	V <sub>SSP</sub>	Supply Ground
23	-	-	V <sub>SSP</sub>	Supply Ground
24	-	-	SENGND	Analog Ground
25	-	-	SENREF	Analog Reference
26	I	Hi-Z	SEND	Analog Input D
27	-	-	NC	Not connected
28	-	-	NC	Not connected
29	-	-	NC	Not connected
30	I/O	PD	$\overline{CS}$	Chip Select / Wake-Up Output
31	-	-	NC	Not connected
32	O	Hi-Z	SYSDISB	System Disable B
33	O	Hi-Z	SYSDISA	System Disable A
34	-	-	NC	Not connected
35	-	-	NC	Not connected



**Table 1-2 Pin Definitions and Functions (PG-TSSOP-38)**

Pin Number	Type	Reset State <sup>1)</sup>	Symbol	Function
36	-	-	NC	Not connected
37	-	-	NC	Not connected
38	I	PU	$\overline{\text{RESET}}$	Reset Input

1) Abbreviations: PU - Pull up; PD - Pull down; Hi-Z - High impedance.

### 1.5 Power Supply and Reset

The power supply to the CIC61508 is regulated by the internal voltage regulator that comes with detection circuitries to ensure that the supplied voltages are within the specified operating range.

The CIC61508 microcontroller requires a power supply voltage level ( $V_{DDP}$ ) of 3.3 V or 5.0 V, which must be provided from the external power supply pin.

$V_{DDP}$  is used to power up the CIC61508. In order to power up the chip properly, the external reset pin  $\overline{\text{RESET}}$  must be asserted until the internal working voltage ( $V_{DDC}$ ) reaches 90% of its intended voltage of 2.5 V. The delay of external reset can be realized by an external capacitor at  $\overline{\text{RESET}}$  pin. This capacitor value must be selected so that  $V_{\overline{\text{RESET}}}$  reaches 0.4 V, but not before  $V_{DDC}$  reaches  $0.9 \cdot V_{DDC}$ .

A typical application example is shown in **Figure 1-2**.  $V_{DDP}$  capacitor value is 300 nF.  $V_{DDC}$  capacitor value is 220 nF. The capacitor connected to  $\overline{\text{RESET}}$  pin is 100 nF.

Typically, the time taken for  $V_{DDC}$  to reach  $0.9 \cdot V_{DDC}$  is less than 50  $\mu\text{s}$  once  $V_{DDP}$  reaches 2.3V. Hence, based on the condition that 10% to 90%  $V_{DDP}$  (slew rate) is less than 500  $\mu\text{s}$ , the  $\overline{\text{RESET}}$  pin should be held low for 500  $\mu\text{s}$  typically. See **Figure 1-3**.

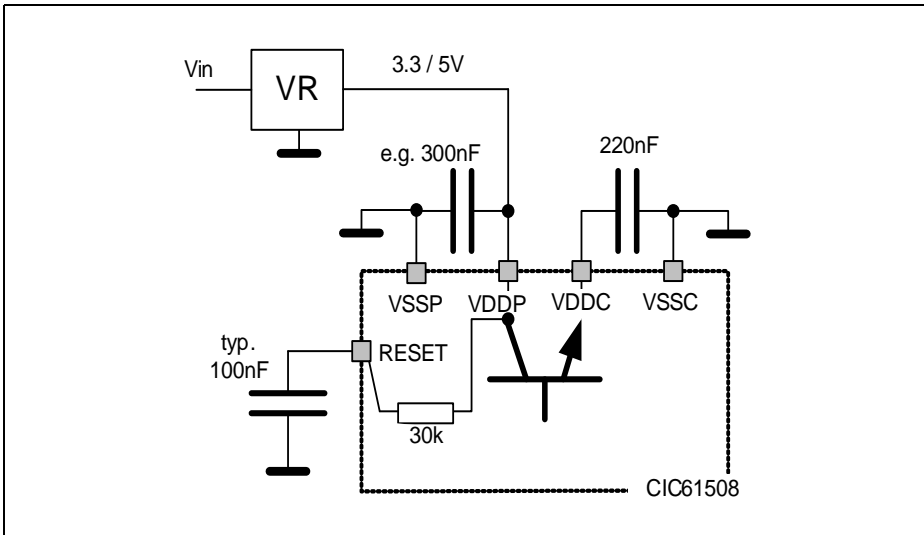
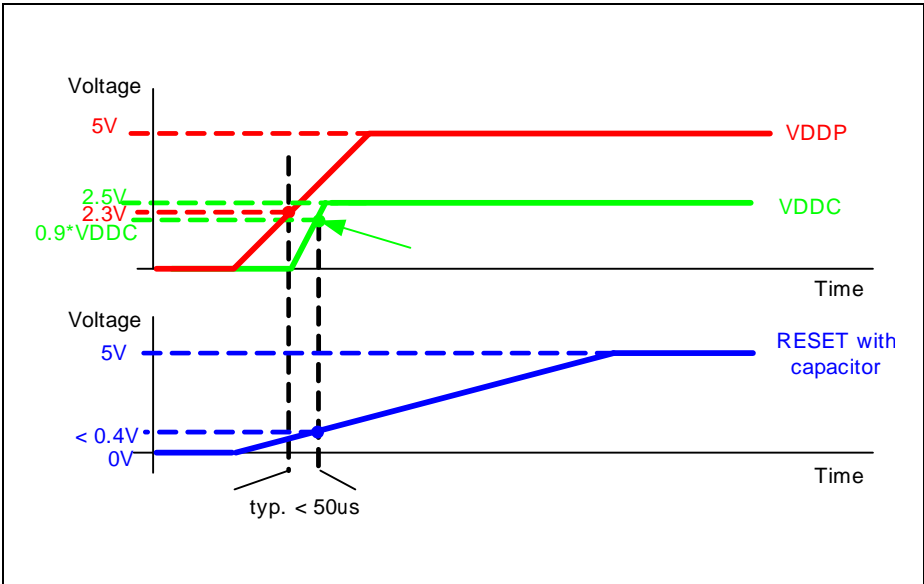


Figure 1-2 Reset Circuitry



**Figure 1-3**  $V_{DDP}$ ,  $V_{DDC}$  and  $V_{RESET}$  during Power-on Reset

An external hardware reset is triggered when the reset input pin  $\overline{RESET}$  is asserted and held low for at least 100 ns.

$V_{DDC}$  detector in the internal voltage regulator detects brownout when the core supply voltage  $V_{DDC}$  dips below the threshold voltage  $V_{DDC\_TH}$  (2.1 V). The brownout will cause the device to be reset.

Both the hardware reset and the brownout reset have the same effect as a power-on reset, therefore the SYSDISx pins will be reset to their default states shown in [Table 1-2](#).

## 2 Electrical Parameters

**Chapter 2** provides the characteristics of the electrical parameters which are implementation-specific for the CIC61508.

### 2.1 General Parameters

The general parameters are described here to aid the users in interpreting the parameters mainly in [Section 2.2](#) and [Section 2.3](#).

#### 2.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the CIC61508 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

- **CC**  
These parameters indicate **Chip Characteristics**, which are distinctive features of the CIC61508 and must be regarded for a system design.
- **SR**  
These parameters indicate **System Requirements**, which must be provided by the system in which the CIC61508 is designed in.

**2.1.2 Absolute Maximum Rating**

Maximum ratings are the extreme limits to which the CIC61508 can be subjected to without permanent damage.

**Table 1 Absolute Maximum Rating Parameters**

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Ambient temperature	$T_A$	-40	140	°C	under bias
Storage temperature	$T_{ST}$	-65	150	°C	
Junction temperature	$T_J$	-40	150	°C	under bias
Voltage on power supply pin with respect to $V_{SS}$	$V_{DDP}$	-0.5	6	V	
Voltage on any pin with respect to $V_{SS}$	$V_{IN}$	-0.5	$V_{DDP} + 0.5$ or max. 6	V	whichever is lower

*Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During absolute maximum rating overload conditions ( $V_{IN} > V_{DDP}$  or  $V_{IN} < V_{SS}$ ) the voltage on  $V_{DDP}$  pin with respect to ground ( $V_{SS}$ ) must not exceed the values defined by the absolute maximum ratings.*

### 2.1.3 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the CIC61508. All parameters mentioned in the following table refer to these operating conditions, unless otherwise noted.

**Table 2 Operating Condition Parameters**

Parameter	Symbol	Limit Values			Unit	Notes/ Conditions
		min.	typ.	max.		
Digital power supply voltage	$V_{DDP}$	3.0	-	3.6	V	3.3V Variant
Digital power supply voltage	$V_{DDP}$	4.5	-	5.5		5.0V Variant
Digital ground voltage	$V_{SS}$	0			V	
Operating Clock Frequency <sup>1)</sup>	$f_{CLK}$	-	26.7	-	MHz	
Ambient temperature	$T_A$	-40	-	140	°C	

1) Some parts of the CIC61508 run at 80 MHz frequency. These frequencies are internal working frequencies of the CIC61508.

## 2.2 DC Parameters

The electrical characteristics of the DC Parameters are detailed in this section.

### 2.2.1 Input/Output Characteristics

**Table 3** provides the characteristics of the input/output pins of the CIC61508.

**Table 3 Input/Output Characteristics (Operating Conditions apply)**

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
<b><math>V_{DDP} = 5\text{ V Range}</math></b>						
Output low voltage	$V_{OL}$	CC	-	1.0	V	$I_{OL} = 15\text{ mA}$
			-	0.4	V	$I_{OL} = 5\text{ mA}$
Output high voltage	$V_{OH}$	CC	$V_{DDP} - 1.0$	-	V	$I_{OH} = -15\text{ mA}$
			$V_{DDP} - 0.4$	-	V	$I_{OH} = -5\text{ mA}$
Input low voltage on port pins	$V_{ILP}$	SR	-	$0.3 \times V_{DDP}$	V	CMOS Mode
Input low voltage on $\overline{\text{RESET}}$ pin	$V_{ILR}$	SR	-	$0.3 \times V_{DDP}$	V	CMOS Mode
Input high voltage on port pins	$V_{IHP}$	SR	$0.7 \times V_{DDP}$	-	V	CMOS Mode
Input high voltage on $\overline{\text{RESET}}$ pin	$V_{IHR}$	SR	$0.7 \times V_{DDP}$	-	V	CMOS Mode
Input Hysteresis on port pins <sup>1)</sup>	$HYS_{P}$	CC	$0.08 \times V_{DDP}$	-	V	CMOS Mode
Pull-up current	$I_{PU}$	SR	-	-10	$\mu\text{A}$	$V_{IH,min}$
			-150	-	$\mu\text{A}$	$V_{IL,max}$
Pull-down current	$I_{PD}$	SR	-	10	$\mu\text{A}$	$V_{IL,max}$
			150	-	$\mu\text{A}$	$V_{IH,min}$
Input leakage current <sup>2)3)</sup>	$I_{OZ1}$	CC	-0.5	0.5	$\mu\text{A}$	$0 < V_{IN} < V_{DDP}$ , $T_A \leq 140^\circ\text{C}$
Overload current on any pin	$I_{OV}$	SR	-5	5	mA	

**Electrical Parameters**
**Table 3 Input/Output Characteristics (Operating Conditions apply) (cont'd)**

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Absolute sum of overload currents	$\Sigma I_{OV} $	SR	–	25	mA	<sup>3)</sup>
Voltage on any pin during $V_{DDP}$ power off	$V_{PO}$	SR	–	0.3	V	<sup>4)</sup>
Maximum current per pin (excluding $V_{DDP}$ and $V_{SS}$ )	$I_M$	SR SR	–	15	mA	
Maximum current for all pins (excluding $V_{DDP}$ and $V_{SS}$ )	$\Sigma I_M $	SR	–	60	mA	
Maximum current into $V_{DDP}$	$I_{MVDDP}$	SR	–	80	mA	
Maximum current out of $V_{SS}$	$I_{MVSS}$	SR	–	80	mA	
<b><math>V_{DDP} = 3.3</math> V Range</b>						
Output low voltage	$V_{OL}$	CC	–	1.0	V	$I_{OL} = 8$ mA
			–	0.4	V	$I_{OL} = 2.5$ mA
Output high voltage	$V_{OH}$	CC	$V_{DDP} - 1.0$	–	V	$I_{OH} = -8$ mA
			$V_{DDP} - 0.4$	–	V	$I_{OH} = -2.5$ mA
Input low voltage on port pins	$V_{ILP}$	SR	–	$0.3 \times V_{DDP}$	V	CMOS Mode
Input low voltage on RESET pin	$V_{ILR}$	SR	–	$0.3 \times V_{DDP}$	V	CMOS Mode
Input high voltage on port pins	$V_{IHP}$	SR	$0.7 \times V_{DDP}$	–	V	CMOS Mode
Input high voltage on RESET pin	$V_{IHR}$	SR	$0.7 \times V_{DDP}$	–	V	CMOS Mode
Input Hysteresis <sup>1)</sup>	$HYS$	CC	$0.03 \times V_{DDP}$	–	V	CMOS Mode
Pull-up current	$I_{PU}$	SR	–	-5	$\mu$ A	$V_{IH,min}$
			-50	–	$\mu$ A	$V_{IL,max}$



**Electrical Parameters**
**Table 3 Input/Output Characteristics (Operating Conditions apply) (cont'd)**

Parameter	Symbol		Limit Values		Unit	Test Conditions
			min.	max.		
Pull-down current	$I_{PD}$	SR	–	5	$\mu\text{A}$	$V_{IL,max}$
			50	–	$\mu\text{A}$	$V_{IH,min}$
Input leakage current <sup>2)3)</sup>	$I_{OZ1}$	CC	-0.5	0.5	$\mu\text{A}$	$0 < V_{IN} < V_{DDP}$ , $T_A \leq 140^\circ\text{C}$
Overload current on any pin	$I_{OV}$	SR	-5	5	$\text{mA}$	
Absolute sum of overload currents	$\Sigma I_{OV} $	SR	–	25	$\text{mA}$	<sup>3)</sup>
Voltage on any pin during $V_{DDP}$ power off	$V_{PO}$	SR	–	0.3	$\text{V}$	<sup>4)</sup>
Maximum current per pin (excluding $V_{DDP}$ and $V_{SS}$ )	$I_M$	SR SR	–	15	$\text{mA}$	
Maximum current for all pins (excluding $V_{DDP}$ and $V_{SS}$ )	$\Sigma I_M $	SR	–	60	$\text{mA}$	
Maximum current into $V_{DDP}$	$I_{MVDDP}$	SR	–	80	$\text{mA}$	
Maximum current out of $V_{SS}$	$I_{MVSS}$	SR	–	80	$\text{mA}$	

1) Not subjected to production test, verified by design/characterization. Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.

2) An additional error current ( $I_{INJ}$ ) will flow if an overload current flows through an adjacent pin.  $\overline{\text{RESET}}$  pin has internal pull devices and is not included in the input leakage current characteristic.

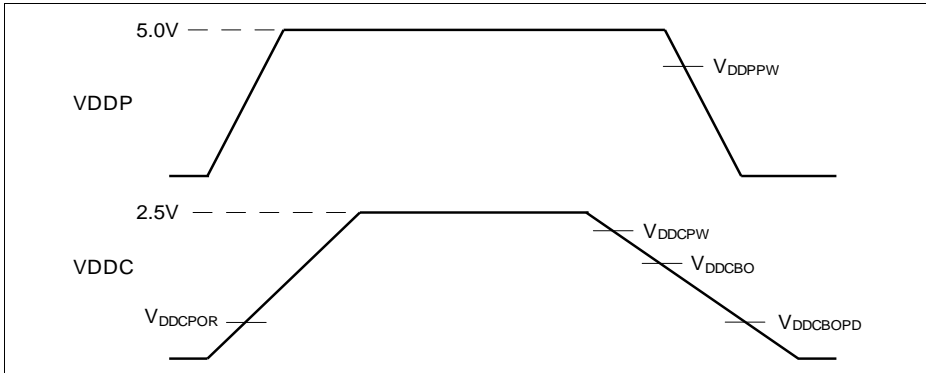
3) Not subjected to production test, verified by design/characterization.

4) Not subjected to production test, verified by design/characterization. However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any pin when  $V_{DDP}$  is powered off.

### 2.2.2 Supply Threshold Characteristics

**Table 4** provides the characteristics of the supply threshold in the CIC61508.

*Note:*  $V_{DDC}$  is an internal working voltage used by some parts of the CIC61508.



**Figure 1** Supply Threshold Parameters

**Table 4** Supply Threshold Parameters (Operating Conditions apply)

Parameters	Symbol		Limit Values			Unit
			min.	typ.	max.	
$V_{DDC}$ prewarning voltage <sup>1)</sup>	$V_{DDCPW}$	CC	2.2	2.3	2.4	V
$V_{DDC}$ brownout voltage in active mode <sup>1)</sup>	$V_{DDCBO}$	CC	2.0	2.1	2.2	V
$V_{DDC}$ brownout voltage in power-down mode <sup>2)</sup>	$V_{DDCBOPD}$	CC	1.3	1.5	1.7	V
$V_{DDP}$ prewarning voltage <sup>3)</sup>	$V_{DDPPW}$	CC	3.4	4.0	4.65	V
Power-on reset voltage <sup>2)</sup>	$V_{DDCPOR}$	CC	1.3	1.5	1.7	V

1) Detection is disabled in power-down mode.

2) Detection is enabled in both active and power-down mode.

3) Detection is enabled for external power supply of 5.0V.  
Detection is disabled for external power supply of 3.3V.

### 2.2.3 Voltage Monitor Characteristics

All ground pins ( $V_{SS}$ ) must be externally connected to one single star point in the system. The voltage difference between the ground pins must not exceed 200mV.

**Table 1 Voltage Monitor Characteristics (Operating Conditions apply)**

Parameter	Symbol		Limit Values			Unit	Test Conditions/ Remarks
			min.	typ .	max.		
Analog reference voltage	$V_{AREF}$	SR	$V_{AGND} + 1$	$V_{DDP}$	$V_{DDP} + 0.05$	V	
Analog reference ground	$V_{AGND}$	SR	$V_{SS} - 0.05$	$V_{SS}$	$V_{AREF} - 1$	V	
Analog input voltage range	$V_{AIN}$	SR	$V_{AGND}$	–	$V_{AREF}$	V	
Total unadjusted error (for 10-bit conversion)	TUE	CC	–	–	2	LSB	5V variant
			–	–	3	LSB	3.3V variant
Switched capacitance at the reference voltage input	$C_{AREFSW}$	CC	–	10	20	pF	<sup>1)2)</sup>
Switched capacitance at the analog voltage inputs	$C_{AINSW}$	CC	–	5	7	pF	<sup>1)3)</sup>
Input resistance of the reference input	$R_{AREF}$	CC	–	1	2	k $\Omega$	<sup>1)</sup>
Input resistance of the selected analog channel	$R_{AIN}$	CC	–	1	1.5	k $\Omega$	<sup>1)</sup>

- 1) Not subject to production test, verified by design/characterization.
- 2) This represents an equivalent switched capacitance. This capacitance is not switched to the reference voltage at once. Instead of this, smaller capacitances are successively switched to the reference voltage.
- 3) The sampling capacity of the conversion C-Network is pre-charged to  $V_{AREF}/2$  before connecting the input to the C-Network. Because of the parasitic elements, the voltage measured at ANx is lower than  $V_{AREF}/2$ .

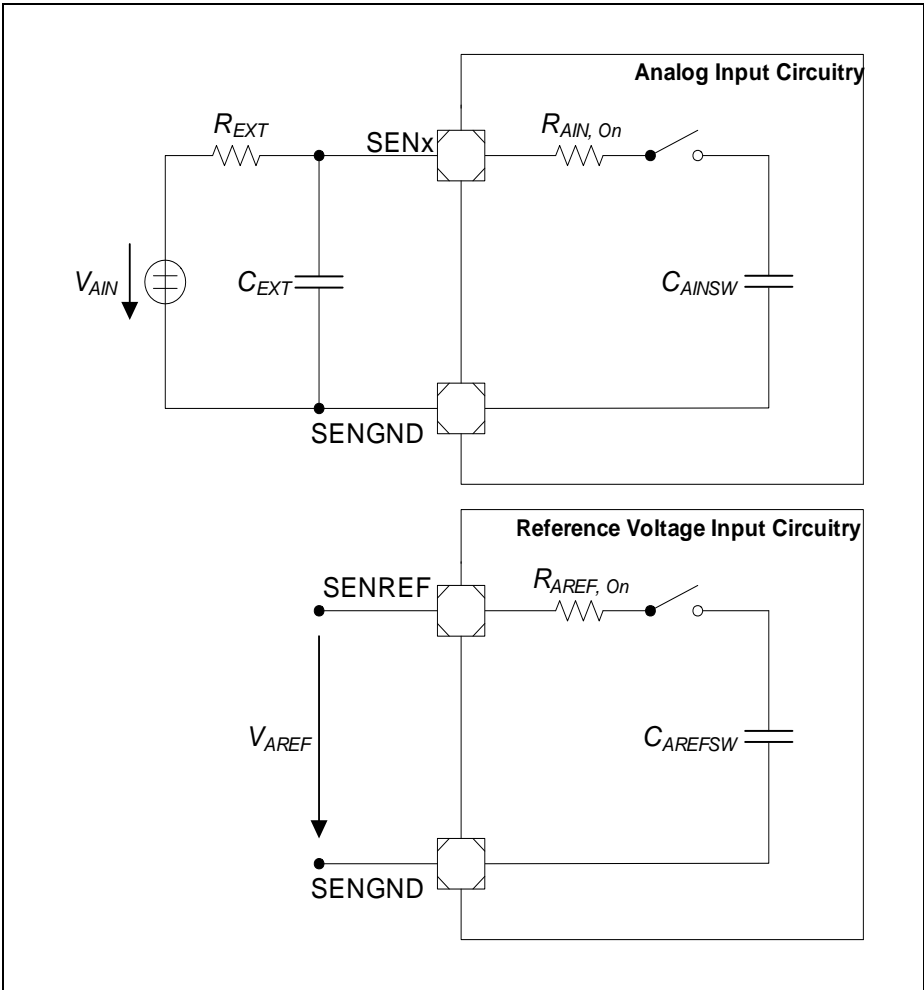


Figure 2 Voltage Monitor Input Circuits

### 2.2.4 Power Supply Current

**Table 2** provides the characteristics of the power supply current in the CIC61508.

**Table 2 Power Supply Current Parameters (Operating Conditions apply)**

Parameter	Symbol	Limit Values		Unit	Test Condition
		typ. <sup>1)</sup>	max. <sup>2)</sup>		
Active Mode	$I_{DDP}$	22.6	24.5	mA	
Periodic Wake-up (low current) Mode <sup>3)</sup>	$I_{PWU}$	4.1	-	mA	<sup>4)</sup>

1) The typical current values are based on preliminary measurements and are to be used as reference only. These values are periodically measured at  $T_A = +25\text{ °C}$  and  $V_{DDP} = 5.0\text{ V}$ .

2) The maximum current values are measured under worst case conditions ( $T_A = +140\text{ °C}$  and  $V_{DDP} = 5.5\text{ V}$ ).

3) The periodic wake-up or low current mode is entered once the wake-up timer functionality is enabled.

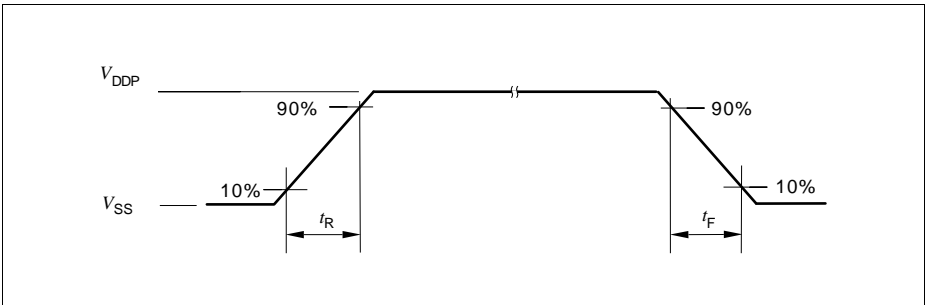
4) Not subjected to production test, verified by design/characterization.

## 2.3 AC Parameters

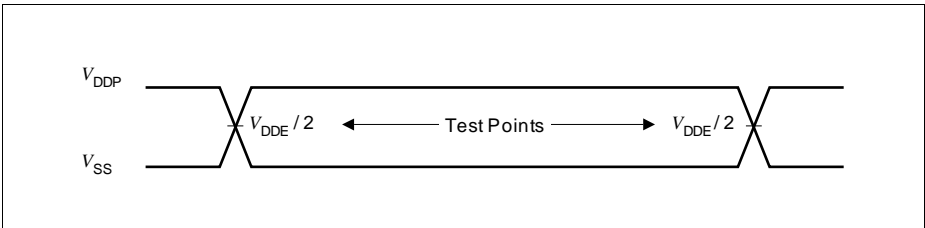
The electrical characteristics of the AC Parameters are detailed in this section.

### 2.3.1 Testing Waveforms

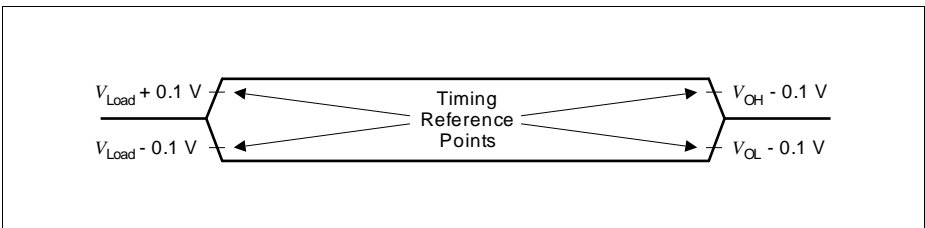
The testing waveforms for rise/fall time, output delay and output high impedance are shown in [Figure 3](#), [Figure 4](#) and [Figure 5](#).



**Figure 3** Rise/Fall Time Parameters



**Figure 4** Testing Waveform, Output Delay



**Figure 5** Testing Waveform, Output High Impedance

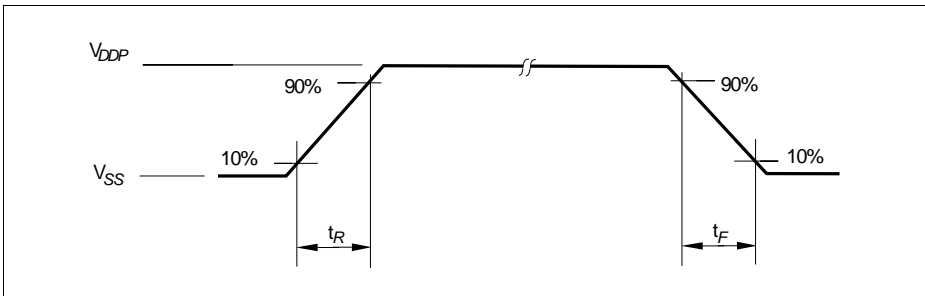
### 2.3.2 Output Rise/Fall Times

**Table 1** provides the characteristics of the output rise/fall times in the CIC61508.

**Table 1 Output Rise/Fall Times Parameters (Operating Conditions apply)**

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
<b><math>V_{DDP} = 5V</math> Range</b>					
Rise/fall times <sup>1) 2)</sup>	$t_R, t_F$	–	10	ns	20 pF. <sup>3)</sup>
<b><math>V_{DDP} = 3.3V</math> Range</b>					
Rise/fall times <sup>1) 2)</sup>	$t_R, t_F$	–	10	ns	20 pF. <sup>4)</sup>

- 1) Rise/Fall time measurements are taken with 10% - 90% of pad supply.
- 2) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.
- 3) Additional rise/fall time valid for  $C_L = 20pF - 100pF @ 0.125 ns/pF$ .
- 4) Additional rise/fall time valid for  $C_L = 20pF - 100pF @ 0.225 ns/pF$ .



**Figure 6 Rise/Fall Times Parameters**

### 2.3.3 Reset Timing

**Table 3** provides the characteristics of the reset timing in the CIC61508.

**Table 2 Reset Timing (Operating Conditions apply)**

Parameter	Symbol		Limit Values			Unit	Test Conditions
			min.	typ.	max.		
Start-up time from an immediate wake-up timer reset <sup>1)</sup>	$t_{SWU}$	CC	–	55.8	–	ms	<sup>2)</sup>

1) The start-up time is measured from the time the immediate wake-up timer reset is triggered to the time the start-up BIST is completed. The immediate wake-up timer reset is triggered by a SFR write command to the WAKERELOAD SFR while WAKEPRESCALAR SFR is configured with the value  $8X_H$ .

2) Not subjected to production test, verified by design/characterization.



### 2.3.4 SPI Timing

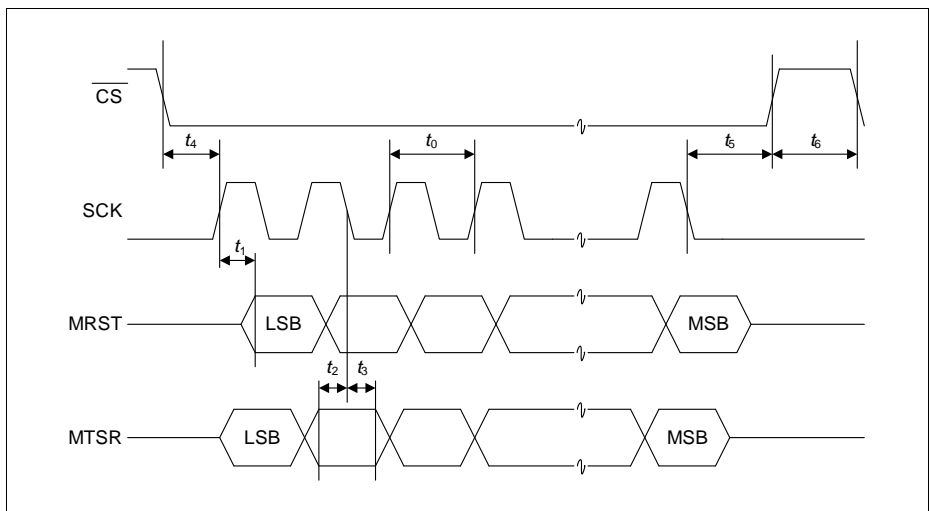
**Table 3** provides the characteristics of the SPI timing in the CIC61508.

*Note: These parameters are not subject to production test but verified by design and/or characterization.*

**Table 3 SPI Timing (Operating Conditions apply; CL = 50 pF)**

Parameter	Symbol		Limit Values		Unit
			min.	max.	
SCLK clock period	$t_0$	SR	500	2000	ns
Data valid	$t_1$	CC	0	–	ns
Data setup time	$t_2$	SR	22	–	ns
Data hold time	$t_3$	SR	0	–	ns
Clock active after $\overline{CS}$ becomes valid	$t_4$	SR	2.0	3.5	$\mu$ s
Clock inactive before $\overline{CS}$ becomes invalid	$t_5$	SR	0	2.8	$\mu$ s
Time between active $\overline{CS}^{1)}$	$t_6$	SR	60.7	65	$\mu$ s

1) The typical value is based on 8 consecutive 16-bit data transfers per heartbeat, at a baud rate of 2 Mbaud.



**Figure 4 SPI Timing**

### 3 Package and Quality Declaration

**Chapter 3** provides the information of the CIC61508 package and reliability section.

#### 3.1 Package Parameters

**Table 3** provides the thermal characteristics of the package used in CIC61508.

**Table 3 Thermal Characteristics of the Package**

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
<b>PG-TSSOP-38</b>					
Thermal resistance junction case <sup>1)</sup>	$R_{TJC}$ CC	-	15.7	K/W	-
Thermal resistance junction lead <sup>1)</sup>	$R_{TJL}$ CC	-	39.2	K/W	-

1) The thermal resistances between the case and the ambient ( $R_{TCA}$ ), the lead and the ambient ( $R_{TLA}$ ) are to be combined with the thermal resistances between the junction and the case ( $R_{TJC}$ ), the junction and the lead ( $R_{TJL}$ ) given above, in order to calculate the total thermal resistance between the junction and the ambient ( $R_{TJA}$ ). The thermal resistances between the case and the ambient ( $R_{TCA}$ ), the lead and the ambient ( $R_{TLA}$ ) depend on the external system (PCB, case) characteristics, and are under user responsibility.

The junction temperature can be calculated using the following equation:  $T_J = T_A + R_{TJA} \times P_D$ , where the  $R_{TJA}$  is the total thermal resistance between the junction and the ambient, while  $P_D$  is given by the multiplication of the max.  $V_{DDP}$  and max.  $I_{DDP}$ . The total junction ambient resistance  $R_{TJA}$  can be obtained from the upper four partial thermal resistances, by

- a) simply adding only the two thermal resistances (junction lead and lead ambient), or
- b) by taking all four resistances into account, depending on the precision needed.

### 3.2 Package Outline

Figure 7 show the package outline of the CIC61508.

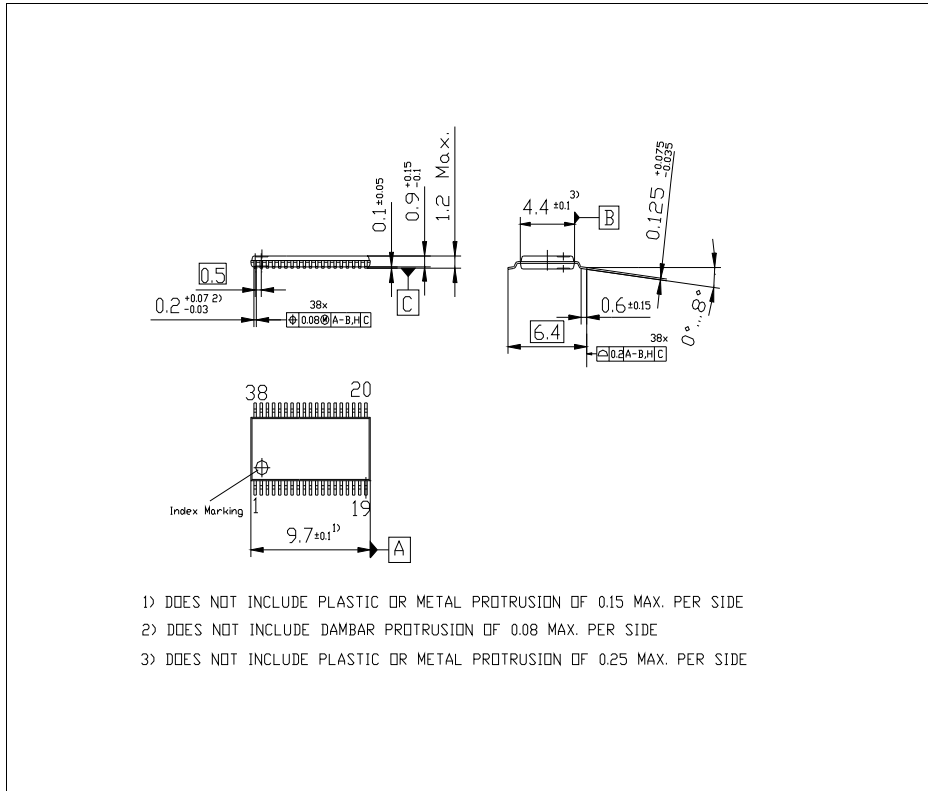


Figure 7 PG-TSSOP-38 Package Outline

### 3.3 Quality Declaration

**Table 4** shows the characteristics of the quality parameters in the CIC61508.

**Table 4 Quality Parameters<sup>1)</sup>**

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	Typ.	Max.		
Operation Lifetime when the device is used at the four stated $T_A$ <sup>2)</sup>	$t_{OP}$	-	-	1500	hours	$T_A = 140^\circ\text{C}$
		-	-	2000	hours	$T_A = 125^\circ\text{C}$
		-	-	10000	hours	$T_A = 85^\circ\text{C}$
		-	-	1500	hours	$T_A = -40^\circ\text{C}$
Operation Lifetime when the device is used at the two stated $T_A$ <sup>2)</sup>	$t_{OP2}$	-	-	18000	hours	$T_A = 108^\circ\text{C}$
		-	-	130000	hours	$T_A = 27^\circ\text{C}$
Weighted Average Temperature <sup>3)</sup>	$T_{WA}$	-	106	-	$^\circ\text{C}$	For 15000 hours
ESD susceptibility according to Human Body Model (HBM) for all pins (except $V_{DDC}$ )	$V_{HBM}$	-	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Human Body Model (HBM) for $V_{DDC}$	$V_{HBMC}$			600		Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	$V_{CDM}$	-	-	750	V	Conforming to JESD22-C101-C

1) Not all parameters are 100% tested, but are verified by design/characterization and test correlation.

2) This lifetime refers only to the time when the device is powered-on.

3) This parameter is derived based on the Arrhenius model.

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