

# High-Speed CMOS Bus Interface 18-Bit Universal Register in QVSOP™

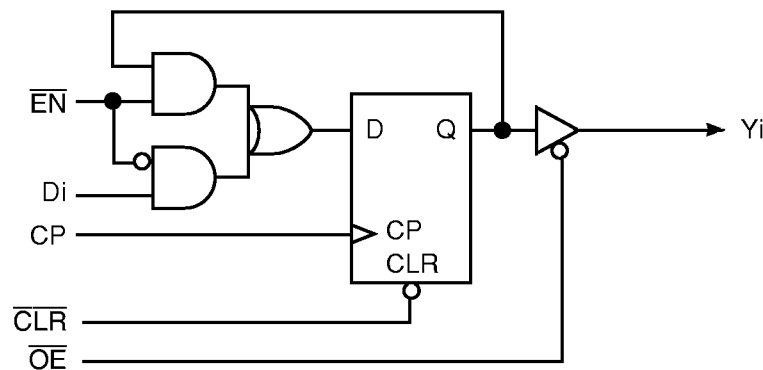
## FEATURES/BENEFITS

- Function compatible to the 74F823, 74FCT823 and 74FCT823T
- CMOS power levels: <15mW static
- Undershoot clamp diodes on all inputs
- Fastest CMOS logic family available
- JEDEC-FCT spec compatible
- TTL-compatible input and output levels
- Ground bounce controlled outputs
- Reduced output swing of 0-3.5V
- Available in 48-pin 0.4mm pitch QVSOP (Q1)
- A speed grades with 10.0ns
- $I_{OL} = 48\text{mA Ind.}$

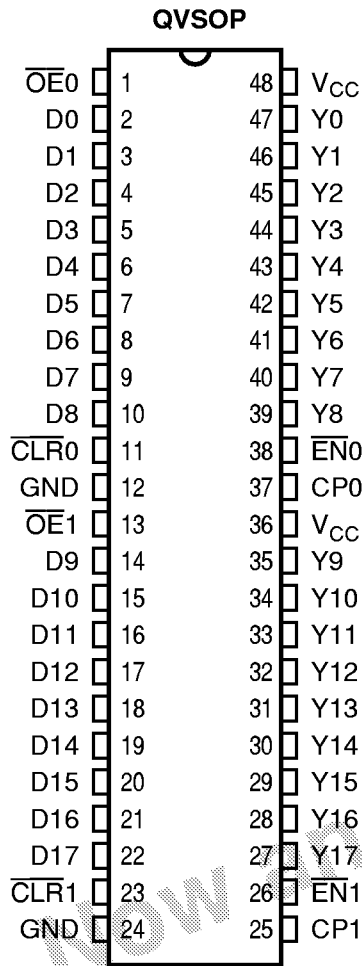
## DESCRIPTION

The QS74FCT2X823T is an 18-bit high-speed CMOS TTL-compatible buffered register with three-state outputs that is ideal for driving high capacitance loads such as memory and address buses. All inputs have clamp diodes for undershoot noise suppression. All outputs have ground bounce suppression (see QSI Application Note AN-001), and outputs will not load an active bus when  $V_{CC}$  is removed from the device.

Figure 1. Functional Block Diagram



**Figure 2. Pin Configurations**  
(All Pins Top View)



**Table 1. Pin Description**

Name	I/O	Description
Di	I	Data Inputs
Yi	O	Data Outputs-Three State
CPi	I	Clock Pulse
$\overline{OE}$	I	Output Enable
$\overline{EN}i$	I	Clock Enable
$\overline{CLR}i$	I	Asynchronous Reset

**Table 2. Function Table**

Inputs					Int.	O/P	Function
$\overline{OE}i$	$\overline{CLR}i$	$\overline{EN}i$	Di	CPi	Qi	Yi	
H	X	L	L	↑	L	Hi-Z	High Z
H	X	L	H	↑	H	Hi-Z	High Z
H	L	X	X	X	L	Hi-Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Hi-Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	L	↑	L	Hi-Z	Load
H	H	L	H	↑	H	Hi-Z	Load
L	H	L	L	↑	L	L	Load
L	H	L	H	↑	H	H	Load

**Table 3. Absolute Maximum Ratings**

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50mA
DC Output Current Max. Sink Current/Pin .....	120mA
Maximum Power Dissipation .....	0.5 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to QSI devices that result in functional or reliability type failures.

**Table 4. Capacitance**

$T_A = 25^\circ\text{C}$ ,  $f = 1\text{MHz}$ ,  $V_{IN} = 0\text{V}$ ,  $V_{OUT} = 0\text{V}$

Pins	Max	Unit
1-11, 13-23, 25-35, 37-47	8	pF

**Note:** Capacitance is characterized but not production tested.

**Table 5. Power Supply Characteristics**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Max	Unit
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$ , Freq = 0 $0\text{V} \leq V_{IN} \leq 0.2\text{V}$ or $V_{CC}-0.2\text{V} \leq V_{IN} \leq V_{CC}$	—	3.0	mA
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH <sup>(2)</sup>	$V_{CC} = \text{Max.}$ , $V_{IN} = 3.4\text{V}$ , Freq = 0	—	2.0	mA
$Q_{CCD}$	Supply Current per Input per MHz <sup>(3,4)</sup>	$V_{CC} = \text{Max.}$ , Outputs open and enabled One bit toggling @ 50% duty cycle Other inputs at GND or $V_{CC}$	—	0.25	mA/MHz

**Notes:**

1. For conditions shown as Min. or Max., use the appropriate values specified under DC specifications.
2. Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ).
3. For flip-flops,  $Q_{CCD}$  is measured by switching one of the data input pins so that the output changes every clock cycle. This is a measurement of device power consumption only and does not include power to drive load capacitance or tester capacitance. This parameter is guaranteed by design but not tested.
4.  $I_C$  can be computed using the above parameters as explained in the Technical Overview section.

**Table 6. DC Electrical Characteristics Over Operating Range**

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions	Min	Typ <sup>(1)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs	—	0.2	—	V
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	5	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{IN} \leq V_{CC}$	—	—	5	$\mu\text{A}$
$I_{OS}$	Short Circuit Current <sup>(2,3)</sup>	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}$	-60	—	—	mA
$V_{IC}$	Input Clamp Voltage <sup>(3)</sup>	$V_{CC} = \text{Min.}, I_{IN} = -18 \text{ mA}$	—	-0.7	-1.2	V
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}, I_{OH} = -24 \text{ mA (COM)}$	2.4	—	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}, I_{OL} = 12 \text{ mA (COM)}$	—	—	0.50	

**Notes:**

1. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^{\circ}\text{C}$ .
2. Not more than one output should be shorted and the duration is  $\leq 1$  second.
3. These parameters are guaranteed by design but not tested.

**Table 7. Switching Characteristics Over Operating Range**

Industrial:  $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ ,  
 $C_{LOAD} = 50\text{pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>	2X823A		2X2823C		Unit
		Min	Max	Min	Max	
$t_{PHL}$ $t_{PLH}$	Clock to Y Delay $\overline{OE} = \text{LOW}$		10		6.0	ns
$t_{PHL}$ $t_{PLH}$	Clock to Y Delay <sup>(2,3)</sup> $\overline{OE} = \text{LOW}$		20		12.5	ns
$t_S$	Data to CP Setup Time	4.0		3.0		ns
$t_H$	Data to CP Hold Time	2.0		1.5		ns
$t_{ENS}$	$\overline{EN}$ to CP Setup Time	4.0		3.0		ns
$t_{ENH}$	$\overline{EN}$ to CP Hold Time	2.0		0.0		ns
$t_{CLR}$	$\overline{CLR}$ to Y Delay		11		8.0	ns
$t_{REC}$	$\overline{CLR}$ to CP Setup Time	6.0		6.0		ns
$t_{PWH}$ $t_{PWL}$	Clock Pulse Width <sup>(2)</sup> HIGH or LOW	7.0		6.0		ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time $\overline{OE}$ to $Y_i$		12		7.0	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time <sup>(2,3)</sup> $\overline{OE}$ to $Y_i$		23		12.5	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time <sup>(2,4)</sup> $\overline{OE}$ to $Y_i$		7.0		6.2	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time <sup>(2)</sup> $\overline{OE}$ to $Y_i$		9.0		6.5	ns

**Notes:**

1. See Test Circuit and Waveforms.
2. This parameter is guaranteed by design but not tested.
3.  $C_{LOAD} = 300\text{pF}$
4.  $C_{LOAD} = 5\text{pF}$