SDAS090 - MARCH 1990 - REVISED JUNE 1992

- Independent Asychronous Inputs and Outputs
- 16 Words by 5 Bits
- Data Rates From 0 to 40 MHz
- Fall-Through Time . . . 14 ns Typ
- 3-State Outputs
- Package Options Include Plastic Small-Outline Packages (DW), Plastic Chip Carriers (FN), and Standard Plastic 300-mil DIPs (N)

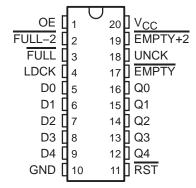
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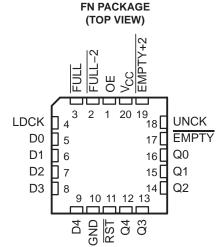
This 80-bit memory uses advanced low-power Schottky technology and features high speed and fast fall-through times. It is organized as 16 words by 5 bits.

A FIFO memory is a storage device that allows data to be written into and read from its array at independent data rates. This FIFO is designed to process data at rates from 0 to 40 MHz in a bit-parallel format, word by word.

Data is written into memory on a low-to-high transition at the load clock (LDCK) input and is read out on a low-to-high transition at the unload clock (UNCK). The memory is full when the number of words clocked in exceeds by 16 the number of words clocked out. When the memory is full, LDCK signals have no effect. When the memory is empty, UNCK signals have no effect.

DW OR N PACKAGE (TOP VIEW)





Status of the FIFO memory is monitored by the FULL, EMPTY, FULL-2, and FULL+2 output flags. The FULL output is low when the memory is full and high when it is not full. The FULL-2 output is low when the memory contains 14 data words. The EMPTY output is low when the memory is empty and high when it is not empty. The EMPTY+2 output is low when two words remain in memory.

A low level on the reset (RST) input resets the internal stack control pointers and also sets EMPTY low and sets FULL, FULL–2, and EMPTY+2 high. The Q outputs are not reset to any specific logic level. The first low-to-high transition on LDCK after either a RST pulse or from an empty condition causes EMPTY to go high and the data to appear on the Q outputs. It is important to note that the first word does not have to be unloaded. Data outputs are noninverting with respect to the data inputs and are at high impedance when the output-enable (OE) input is low. OE does not affect the output flags. Cascading is easily accomplished in the word-width direction but is not possible in the word-depth direction.

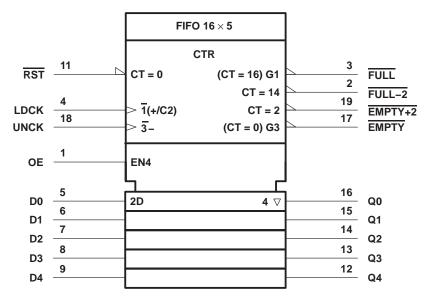
The SN74ALS229B is characterized for operation from 0°C to 70°C.



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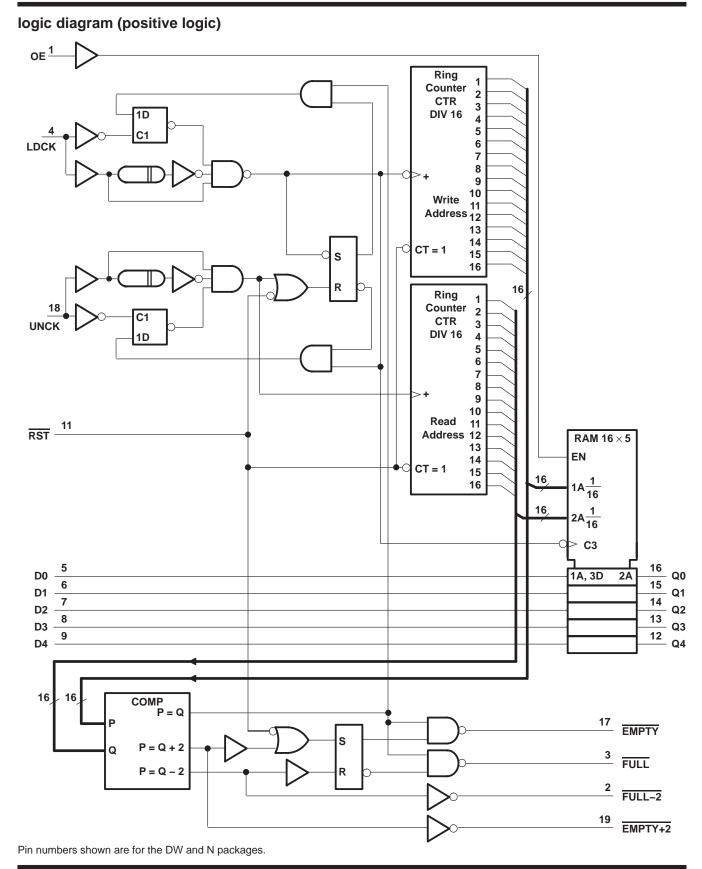


logic symbol[†]



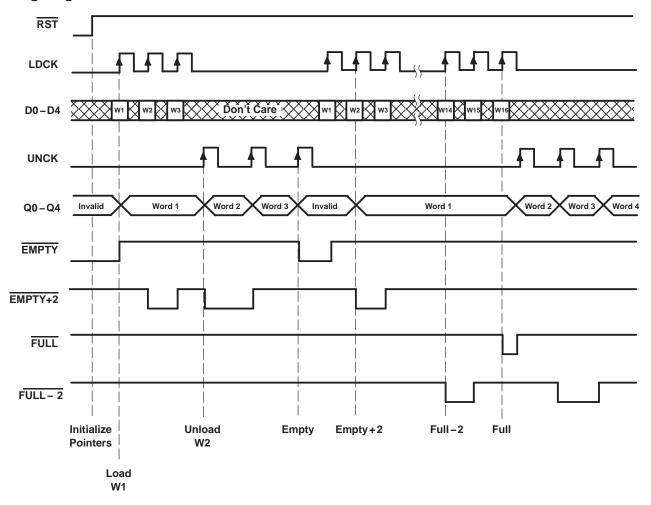
[†] This symbol is in accordance with ANSI/IEEE Standard 91-1984 and IEC Publication 617-12. The symbol is functionally accurate but does not show the details of implementation; for these, see the logic diagram. The symbol represents the memory as if it were controlled by a single counter whose content is the number of words stored at the time. Output data is invalid when the counter content (CT) is 0. Pin numbers shown are for the DW and N packages.







timing diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V _{CC}	7 V
Input voltage, V _I	7 V
Voltage applied to a disabled 3-state output	5.5 V
Operating free-air temperature range, T _A	0°C to 70°C
Storage temperature range	65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



recommended operating conditions (see Note 1)

			MIN	NOM	MAX	UNIT
Vсс	Supply voltage				5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
	High-level output current	Q outputs			-1.6	
ЮН		Status flags			-0.4	mA
		Q outputs			24	
lOL	Low-level output current	Status flags			8	mA
	Olask framosani	LDCK	0		40	MHz
f _{clock}	Clock frequency	UNCK	0		40	
		RST low	18			
t _W	Pulse duration	LDCK low	15			
		LDCK high	10			ns
		UNCK low	15			
		UNCK high	10			
t _{SU}		Data before LDCK↑	8			
	Setup time	RST (inactive) before LDCK↑	5			ns
		LDCK (inactive) before RST↑	5			
th	Hold time	Data after LDCK↑	5			ns
T _A	Operating free-air temperature		0		70	°C

NOTE 1: To ensure proper operation of this high-speed FIFO device, it is necessary to provide a clean signal to the LDCK and UNCK clock inputs. Any excessive noise or glitching on the clock inputs that violates the V_{IL}, V_{IH}, or minimum pulse duration limits can cause a false clock or improper operation of the internal read and write pointers.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Т	MIN TYPT	MAX	UNIT		
٧ıĸ		V _{CC} = 4.5 V,	I _I = -18 mA		-1.2	V	
Vон	Q outputs	V _{CC} = 4.5 V,	$I_{OL} = -2.6 \text{ mA}$	2.4 3.2			
	Status flags	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V},$	$I_{OL} = -0.4 \text{ mA}$	V _{CC} -2		٧	
	O austravita	$V_{CC} = 4.5 \text{ V},$	$I_{OL} = 12 \text{ mA}$	0.25	0.4		
.,	Q outputs	V _{CC} = 4.5 V,	I _{OL} = 24 mA	0.35	0.5	.,	
VOL	Status flags	V _{CC} = 4.5 V,	I _{OL} = 4 mA	0.25	0.4	V	
		$V_{CC} = 4.5 \text{ V},$	I _{OL} = 8 mA	0.35	0.5		
lozh		V _{CC} = 5.5 V,	V _O = 2.7 V		20	μΑ	
lozL		V _{CC} = 5.5 V,	V _O = 0.4 V		-20	μΑ	
lį		V _{CC} = 5.5 V,	V _I = 7 V		0.1	mA	
lн		V _{CC} = 5.5 V,	V _I = 2.7 V		20	μΑ	
IլL		V _{CC} = 5.5 V,	V _I = 0.4 V		-0.2	mA	
lo [‡]		$V_{CC} = 5.5 \text{ V},$	V _O = 2.25 V	-30	-112	mA	
ICC		V _{CC} = 5.5 V		85	140	mA	

[†] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.



[‡] The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, los.

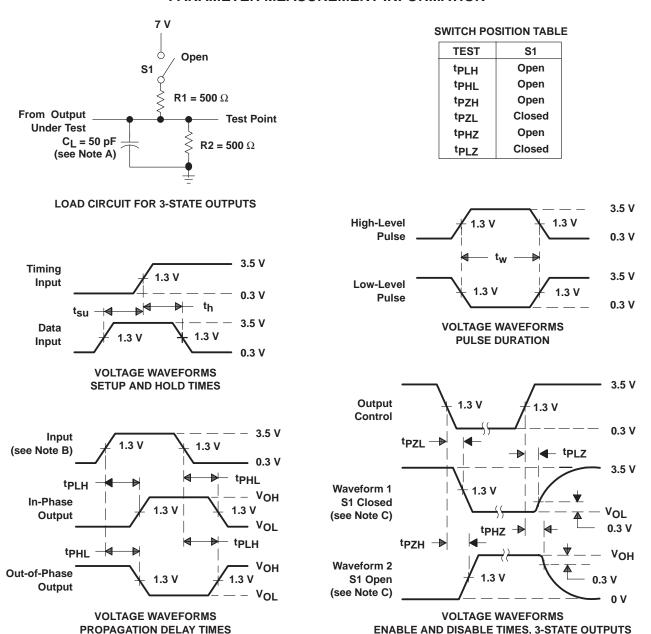
SN74ALS229B 16×5 ASYNCHRONOUS FIRST-IN, FIRST-OUT MEMORY

SDAS090 - MARCH 1990 - REVISED JUNE 1992

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$C_L = 50 \text{ pl}$ $R1 = 500 \Omega$ $R2 = 500 \Omega$	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 0°C to 70°C		
			MIN	MAX		
fmax	LDCK, UNCK		40		MHz	
	LDCK↑	A O	6	30		
^t pd	UNCK↑	Any Q	6	30	ns	
^t PLH	LDCK [↑]		5	25		
^t PHL	UNCK↑	EMPTY	6	27	ns	
^t PHL	RST↓	EMPTY	5	26	ns	
,	LDCK↑		7	33		
^t pd	UNCK↑	EMPTY+2	35	ns		
^t PLH	RST↓	EMPTY+2	9	33	ns	
	LDCK [↑]		7	33		
t _{pd}	UNCK↑	FULL-2	9	35	ns	
^t PLH	RST↓	FULL-2	9	33	ns	
^t PHL	LDCK [↑]	FULL	6	27	ns	
	UNCK↑		5	25	ns	
^t PLH	RST↓	FULL	8	31		
t _{en}	OE↑	Q	2	15	ns	
t _{dis}	OE↓	Q	1	15	ns	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_0 = 50 \ \Omega$, $t_f \leq 2 \ ns$, $t_f \leq 2 \ ns$.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74ALS229BDW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74ALS229BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS229BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74ALS229BN	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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