

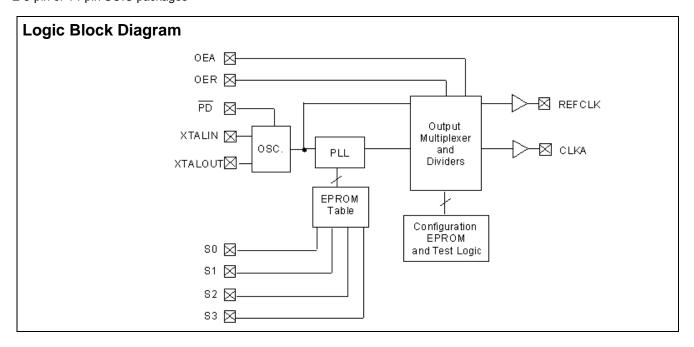
# Single-PLL General Purpose EPROM Programmable Clock Generator

#### **Features**

- Single phase locked loop (PLL) architecture
- EPROM programmability
- Factory programmable (CY2907) or field programmable (CY2907F) device options
- Up to two configurable outputs
- Low skew, low jitter, high accuracy outputs
- Power management (power down, OE)
- Frequency select option
- Configurable 5 V or 3.3 V Operation
- 8-pin or 14-pin SOIC packages

### **Benefits**

- Generates a custom frequency from an external source
- Easy customization and fast turnaround
- Programming support available for all opportunities
- Provides clocking requirements from a single device
- Meets critical industry standard timing requirements
- Supports low power applications
- Up to 16 user selectable frequencies
- Supports industry standard design platforms
- Industry standard packaging saves on board space





### **Pin Configurations**

Figure 1. 14-Pin SOIC and 8-Pin SOIC (Top View)



## **Pin Description**

Name	Pin N	umber	Description
Name	14-Pin SOIC	8-Pin SOIC	Description
S1	1	5	Frequency Select (CLKA) (Internal pull up resistor to V <sub>DD</sub> )
S2	2	NA	Frequency Select (CLKA) (Internal pull up resistor to V <sub>DD</sub> )
S3	3	NA	Frequency Select (CLKA) (Internal pull up resistor to V <sub>DD</sub> )
V <sub>SS</sub>	4	2	Ground
V <sub>SS</sub>	5	NA	Ground
PD	6	NA	Power Down (Active LOW) (Internal pull up resistor to V <sub>DD</sub> )
XTALIN <sup>[1]</sup>	7	3	Reference Crystal Input
XTALOUT <sup>[1, 2]</sup>	8	4	Reference Crystal Feedback
OER	9	NA	REFCLK Output Enable (Active HIGH) (Internal pull up resistor to V <sub>DD</sub> )
OEA	10	NA	CLKA Output Enable (Active HIGH) (Internal pull up resistor to V <sub>DD</sub> )
CLKA	11	6	Clock Output
$V_{DD}$	12	7	Voltage Supply
REFCLK	13	8	Reference Clock Output (Default, can be driven by PLL if desired)
S0	14	1	Frequency Select (CLKA) (Internal pull up resistor to V <sub>DD</sub> )

<sup>1.</sup> For best accuracy, use a parallel resonant crystal,  $C_{LOAD} \approx 17$  pF.

2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to crystal).



### **Functional Description**

The CY2907 is a general purpose clock generator designed for use in a wide variety of applications—from graphics to PC peripherals to disk drives. It generates selectable system clock frequencies from a single reference input (crystal or reference clock). The CY2907 is configured with an EPROM array, similar to the other devices in the Cypress EPROM Programmable Clock family, making it easy to customize for any application. Furthermore, the CY2907 is compatible with all industry standard 9107 and 9108 clock synthesizers.

### **Device Programming**

Two versions of the CY2907 are available - Field Programmable and Factory Programmable. Field programmable devices must be programmed before being installed in an application. They are one-time-programmable (OTP). Customers can program small quantities in-house using the Cypress CY3670 programmer. Production quantities are available through Cypress's value-added distribution partners, or by using third party programmers from BP Microsystems, Hi-Lo Systems, and others.

For high volume orders, devices can be factory programmed by Cypress. All requests must be submitted to the local Cypress Field Application Engineer (FAE) or sales representative. After the request is processed, you receive a new part number, samples, and a data sheet with the programmed values. This part number is used for additional sample requests and production orders.

### CyberClocks™ Software

CyberClocks is an easy-to-use software application that enables the user to configure any one of the EPROM Programmable Clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Note the output frequency ranges in this data sheet when specifying them in CyberClocks to make sure that you stay within the limits. After a configuration is established, you can print the configuration and save programming files in ENT and JED formats.

CyberClocks runs on PCs running the Windows™ operating system, and is available for free download on the Cypress Semiconductor website at www.cypress.com.

Within the CyberClocks application, the CY2907 is found in the CyClocks<sup>™</sup> section. Note that the standalone CyberClocks software should not be confused with the CyberClocks Online software, which is a web-based application that is used to configure other programmable clock devices.

### **Cypress CY3670 Programming Kit**

Cypress's CY3670 is a portable programmer that connects to a PC serial port and enables users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. An adapter is also required and is ordered separately. The CY3097 is the adapter for the CY2907F8. For the CY2907F14, order adapter CY3098.

### **Maximum Ratings**

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Supply Voltage	0.5 to +7.0 V
Input Voltage	0.5 V to V <sub>DD</sub> +0.5 V
Storage Temperature (Non-Condens	ing) –65 °C to +150 °C
Max Soldering Temperature (10 sec)	
Junction Temperature	+150 °C
Static Discharge Voltage(per MIL-STD-883, Method 3015)	>2000 V

# Operating Conditions<sup>[1]</sup>

Parameter	Description	Min	Max	Unit
$V_{DD}$	Supply Voltage, 5 V Operation	4.5	5.5	V
	Supply Voltage, 3.3 V Operation	3.0	3.6	V
T <sub>A</sub>	Commercial Operating Temperature, Ambient	0	70	°C
C <sub>L</sub>	Max. Capacitive Load		15	pF
f <sub>REF</sub>	External Reference Crystal		25.0	MHz
	External Reference Clock <sup>[2, 3]</sup>	1.0	30.0	MHz

- 1. Electrical parameters are guaranteed with these operating conditions.
- 2. Guaranteed by design, not 100% tested in production.
- 3. Load = max. typical configuration, f<sub>REF</sub> = 14.318 MHz. Specific configurations may vary. A close approximation of I<sub>DD</sub> can be derived by the following formula: I<sub>DD</sub> (mA) = V<sub>DD</sub> \* (6.25 + (0.055\*F<sub>REF</sub>) + (0.0017\*C<sub>LOAD</sub>\*(F<sub>CLKA</sub> + REFCLK))). C<sub>LOAD</sub> is specified in pF and F is specified in MHz.

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# Electrical Characteristics at 5.0 V Commercial $V_{DD}$ = 4.5 V to 5.5 V, $T_A$ = 0 °C to +70 °C

Parameter	Description		Test Conditions			Max	Unit
V <sub>IH</sub>	High-level Input Voltage	Except Crystal In	puts		2.0		V
V <sub>IL</sub>	Low-level Input Voltage	Except Crystal In	puts			0.8	V
V <sub>OH</sub> <sup>[1]</sup>	High-level Output Voltage	$V_{DD} = V_{DD}$ Min.	$I_{OH} = -30 \text{ mA}$	CLKA	2.4		V
V <sub>OL</sub> <sup>[1]</sup>	Low-level Output Voltage	$V_{DD} = V_{DD}$ Min.	I <sub>OL</sub> = 10 mA	CLKA		0.4	V
I <sub>OH</sub> <sup>[1]</sup>	Output High Current $V_{OH} = 2.0V$				-35	mA	
I <sub>OL</sub> <sup>[1]</sup>	Output Low Current	$V_{OL} = 0.8V$	V <sub>OL</sub> = 0.8V		22		mA
I <sub>IH</sub>	Input High Current	$V_{IH} = V_{DD}$		-2	2	μА	
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0V	$V_{IL} = 0V$			20	μА
I <sub>DD</sub> <sup>[2]</sup>	Power Supply Current	PD HIGH, CLKA	PD HIGH, CLKA = 50 MHz			42	mA
I <sub>DD</sub>	Power Supply Current	PD LOW, Logic Inputs LOW			100	μА	
I <sub>DD</sub>	Power Supply Current	PD LOW, Logic Inputs HIGH			40	μА	
R <sub>PU</sub> <sup>[1]</sup>	Pull Up Resistor	$V_{IN} = V_{DD} - 1.0 \ V_{IN} = V_{DD} - 1.0 \ V_{D$	/			700	kΩ

<sup>1.</sup> Guaranteed by design, not 100% tested in production.

# Electrical Characteristics at 3.3 V Commercial $V_{DD}$ = 3.0 V to 3.6 V, $T_A$ = 0 °C to +70 °C

Parameter	Description	Test Conditions	Min	Max	Unit
V <sub>IH</sub>	High-level Input Voltage	Except Crystal Inputs	0.7*V <sub>DD</sub>		V
V <sub>IL</sub>	Low-level Input Voltage	Except Crystal Inputs		0.2*V <sub>DD</sub>	V
V <sub>OH</sub> <sup>[1]</sup>	High-level Output Voltage	CLKA, I <sub>OH</sub> = -5 mA	0.85*V <sub>DD</sub>		V
V <sub>OL</sub> <sup>[1]</sup>	Low-level Output Voltage	CLKA, I <sub>OL</sub> = 6 mA		0.1*V <sub>DD</sub>	V
I <sub>OH</sub> <sup>[1]</sup>	Output High Current	$V_{OH} = 0.7^*V_{DD}$		-10	mA
I <sub>OL</sub> <sup>[1]</sup>	Output Low Current	$V_{OL} = 0.2 V_{DD}$	15		mA
I <sub>IH</sub>	Input High Current	$V_{IH} = V_{DD}$	-2	2	μА
I <sub>IL</sub>	Input Low Current	V <sub>IL</sub> = 0 V		10	μА
I <sub>DD</sub> <sup>[2]</sup>	Power Supply Current	PD HIGH, CLKA = 50 MHz		40	mA
I <sub>DD</sub>	Power Supply Current	PD LOW, Logic Inputs LOW		40	μА
I <sub>DD</sub>	Power Supply Current	PD LOW, Logic Inputs HIGH		12	μА
R <sub>PU</sub> <sup>[1]</sup>	Pull Up Resistor	$V_{IN} = V_{DD} - 0.5 \text{ V}$		900	kΩ

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Coad = max. typical configuration, f<sub>REF</sub> = 14.318 MHz. Specific configurations may vary. A close approximation of I<sub>DD</sub> can be derived by the following formula: I<sub>DD</sub> (mA) = V<sub>DD</sub> \* (6.25 + (0.055\*F<sub>REF</sub>) + (0.0017\*C<sub>LOAD</sub>\*(F<sub>CLKA</sub> + REFCLK))). C<sub>LOAD</sub> is specified in pF and F is specified in MHz.

Guaranteed by design, not 100% tested in production.
 Load = max. typical configuration, f<sub>REF</sub> = 14.318 MHz. Specific configurations may vary. A close approximation of I<sub>DD</sub> can be derived by the following formula: I<sub>DD</sub> (mA) = V<sub>DD</sub> \* (6.25 + (0.055\*F<sub>REF</sub>) + (0.0017\*C<sub>LOAD</sub>\*(F<sub>CLKA</sub> + REFCLK))). C<sub>LOAD</sub> is specified in pF and F is specified in MHz.



# Switching Characteristics at 5.0 V Commercial $^{[1]}$

Parameter	Output <sup>[2]</sup>	Description	Test Conditions	Min	Max	Unit
t <sub>R</sub>	CLKA	Output Rise Time 0.8 V to 2.0 V	15 pF Load		1.40	ns
t <sub>F</sub>	CLKA	Output Fall Time 2.0 V to 0.8 V	15 pF Load		1.00	ns
t <sub>R</sub>	CLKA	Output Rise Time 20% to 80%	15 pF Load		3.5	ns
t <sub>F</sub>	CLKA	Output Fall Time 80% to 20%	15 pF Load		2.5	ns
t <sub>D</sub>	CLKA	Duty Cycle	15 pF Load at 1.4 V	45.0	55.0	%
F <sub>I</sub>	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F <sub>I</sub>	XTALIN	Input Frequency	External Input Clock <sup>[3]</sup>	1	30	MHz
F <sub>O</sub>	CLKA	Output Frequency	CY2907, 15 pF Load	0.5	130.0	MHz
			CY2907F, 15 pF Load	0.5	100.0	MHz
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	20 MHz to 130 MHz		150	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	14 MHz to 20 MHz		200	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	20 MHz to 130 MHz	-250	+ 250	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	14 MHz to 20 MHz	<b>-</b> 500	+ 500	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t <sub>PU</sub>		Power Up Time			18	ms
t <sub>FT</sub>	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

Guaranteed by design, not 100% tested in production.

# Switching Characteristics at 3.3 V Commercial<sup>[1]</sup>

Parameter	Output <sup>[2]</sup>	Description	Test Conditions	Min	Max	Unit
t <sub>R</sub>	CLKA	Output Rise Time 20% to 80%	15 pF Load		3.5	ns
t <sub>F</sub>	CLKA	Output Fall Time 80% to 20%	15 pF Load		2.5	ns
t <sub>D</sub>	CLKA	Duty Cycle	15 pF Load at 1.4 V	40.0	53.0	%
F <sub>I</sub>	XTALIN	Input Frequency	Crystal Oscillator	10	25	MHz
F <sub>I</sub>	XTALIN	Input Frequency	External Input Clock <sup>[3]</sup>	1	30	MHz
F <sub>O</sub>	CLKA	Output Frequency	CY2907, 15 pF Load	0.5	100.0	MHz
			CY2907F, 15 pF Load	0.5	80.0	MHz
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	25 MHz to 100 MHz		150	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	14 MHz to 25 MHz		200	ps
t <sub>JIS</sub>	CLKA	Jitter (One Sigma)	Less than 14 MHz		1	%
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	25 MHz to 120 MHz	-250	+250	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	14 MHz to 25 MHz	-500	+500	ps
t <sub>JAB</sub>	CLKA	Jitter (Absolute)	Less than 14 MHz		3	%
t <sub>PU</sub>		Power Up Time			18	ms
t <sub>FT</sub>	CLKA	Transition Time	8 MHz to 66.6 MHz		13	ms

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REFCLK output can also be configured to be driven by the PLL. In that case these characteristics are also valid.
 Refer to the application note *Crystal Oscillator Topics* when using an external reference clock as an input frequency source.

Guaranteed by design, not 100% tested in production.
 REFCLK output can also be configured to be driven by the PLL. In that case these characteristics are also valid.

<sup>3.</sup> Refer to the application note Crystal Oscillator Topics when using an external reference clock as an input frequency source.



# **Switching Waveforms**

Figure 2. Frequency Select Change (Transition Time)

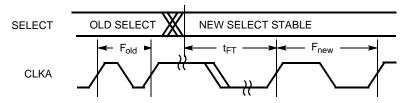


Figure 3. Duty Cycle Timing

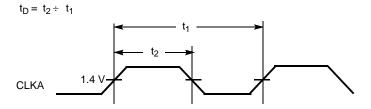
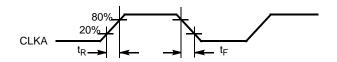
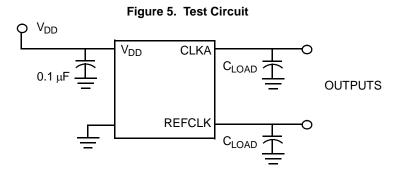


Figure 4. All Outputs Rise/Fall Time



### **Test Circuit**



Note: All capacitors should be placed as close to each pin as possible.



# **Ordering Information**

Ordering Code	Package Type	Operating Range			
CY2907SL-262 <sup>[1]</sup>	8-pin SOIC	3.3 V, Commercial, Factory Programmed			
CY2907SL-262T <sup>[1]</sup>	8-pin SOIC - Tape and Reel	3.3 V, Commercial, Factory Programmed			
CY2907SL-367T <sup>[1]</sup>	8-pin SOIC - Tape and Reel	3.3 V, Commercial, Factory Programmed			
Pb-free					
CY2907FX8 <sup>[1]</sup>	8-pin SOIC	5.0 V/3.3 V, Commercial, Field Programmable			
CY2907FX8T <sup>[1]</sup>	8-pin SOIC - Tape and Reel	5.0 V/3.3 V, Commercial, Field Programmable			
CY2907FX14 <sup>[1]</sup>	14-pin SOIC	5.0 V/3.3 V, Commercial, Field Programmable			
CY2907FX14T <sup>[1]</sup>	14-pin SOIC - Tape and Reel	5.0 V/3.3 V, Commercial, Field Programmable			
Programmer	Programmer				
CY3670	Cypress FTG Programmer				
CY3097	Socket Adapter for CY3670 for programming CY2907FX8				
CY3098	Socket Adapter for CY3670 for programm	ing CY2907FX14			

<sup>1.</sup> Not for new designs. New designs should use a device other than the CY2907.

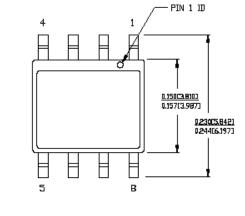
## **Package Characteristics**

Package	θ <sub>JA</sub> (C/W)	θ <sub>JC</sub> (C/W)	Transistor Count
8-pin SOIC	170	35	5436
14-pin SOIC	140	31	5436



### **Package Diagrams**

Figure 6. 8-Pin (150-Mil) SOIC



- DIMENSIONS IN INCHESEMM) MIN. MAX.
- 2. PIN 1 II IS OPTIONAL, ROUNI ON SINGLE LEAIFRAME RECTANGULAR ON MATRIX LEADFRAME
- 3. REFERENCE JEDEC MS-012
- 4. PACKAGE WEIGHT 0.07gms

PART #				
208.15	STANDARD PKG.			
SZ08.15	LEAD FREE PKG.			

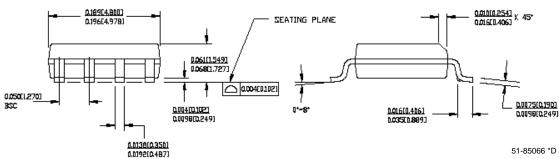
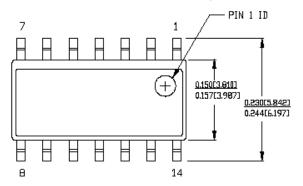
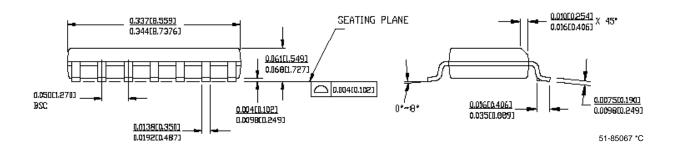


Figure 7. 14-Pin (150-Mil) SOIC



DIMENSIONS IN INCHESIMM) MIN. MAX.
REFERENCE JEDEC MS-012

PART #				
Z14.15	STANDARD PKG.			
SZ14.15	LEAD FREE PKG.			



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### **Document History Page**

	Document Title: CY2907 Single-PLL General Purpose EPROM Programmable Clock Generator Document Number: 38-07137			
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	110246	SZV	12/18/01	Change from Spec number: 38-00505 to 38-07137
*A	1088524	KVM/ KKVTMP	See ECN	Added Pb-free for CY2907F8 and CY2907F14 field programmable devices Updated and added to text on page 2 Applied new template
*B	2715646	KVM/AESA	06/10/09	Removed obsolete part numbers from the ordering information table: CY2907SC-xxx, CY2907SC-xxxT, CY2907SI-xxxT, CY2907F8T, CY2907F8I, CY2907F8IT, CY2907F14T, CY2907F14I and CY2907F14IT Added note: "Not for new designs" Removed industrial temperature references: page 1 features list, T <sub>A</sub> spec, DC and AC electrical tables Removed Selector Guide table from page 1
*C	2948496	KVM	06/09/10	Updated package diagrams and ordering information table.

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