EMI9406

L-C LCD and Camera EMI Array with ESD Protection

ON Semiconductor®

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Functional Description

The EMI9406 is an inductor−based (L−C) EMI filter array with ESD protection, which integrates six filters in a uDFN package with 0.40 mm pitch. Each EMI filter channel of the EMI9406 is implemented with the component value of 1.8 pF 35 nH−4.7 pF−35 nH−6 pF. The cut−off frequency at −3 dB attenuation is 300 MHz and can be used in applications where the data rates are as high as 160 Mbps, while providing greater than −35 dB attenuation over the 800 MHz to 2.7GHz frequency range. The parts include ESD diodes on every I/O pin and provide a high level of protection against electrostatic discharge (ESD). The ESD protection diodes connected to the external filter ports are designed and characterized to safely dissipate ESD strikes of ±14 kV, which is beyond the maximum requirement of the IEC61000−4−2 international standard.

This device is particularly well suited for wireless handsets, mobile LCD modules and PDAs because of its small package format and easy−to−use pin assignments. In particular, the EMI9406 is ideal for EMI filtering and protecting data and control lines for the LCD display and camera interface in mobile handsets.

The EMI9404 is housed in space saving, low profile, 0.40 mm pitch UDFN packages in a RoHS compliant, Pb−Free format.

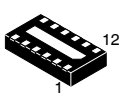
Features

- Six Channels of EMI Filtering with Integrated ESD Protection
- Pi−Style EMI Filters in a Capacitor−Inductor−Capacitor (C−L−C) Network
- ±14 kV ESD Protection (IEC 61000−4−2 Level 4, contact discharge) at External Pin
- Greater than −35 dB Attenuation (typical) at 1 GHz
- UDFN Pb−Free Package with 0.40 mm Lead Pitch: 6−ch. = 12−Lead UDFN
- UDFN Pb−Free Package with 0.40 mm Lead Pitch: 12−lead: 2.50 mm x 1.35 mm
- Increased Robustness Against Vertical Impacts During Manufacturing Process
- These Devices are Pb−Free and are RoHS Compliant

Applications

- LCD and Camera Data Lines in Mobile Handsets
- I/O Port Protection for Mobile Handsets, Notebook Computers, PDAs, etc.
- EMI Filtering for Data Ports in Cell Phones, PDAs or Notebook Computer
- Wireless Handsets
- Handheld PCs/PDAs
- LCD and Camera Modules

MARKING DIAGRAMS

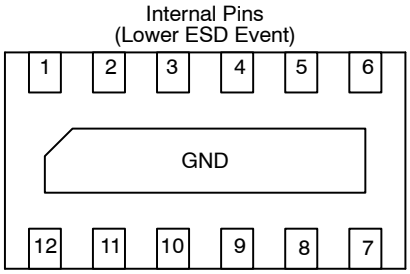


UDFN12
CASE 517BD

L6 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PINOUTS



(Bottom View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

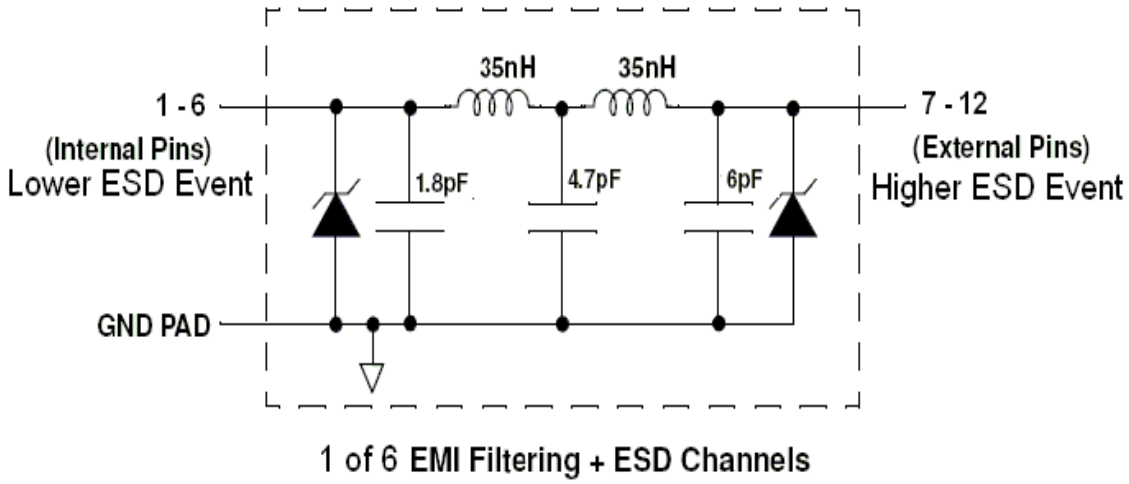


Figure 1. Electrical Schematic

Table 1. PIN DESCRIPTIONS

Pin #	Name	Description
1	FILTER1	Filter + ESD Channel 1 (Internal)
2	FILTER2	Filter + ESD Channel 2 (Internal)
3	FILTER3	Filter + ESD Channel 3 (Internal)
4	FILTER4	Filter + ESD Channel 4 (Internal)
5	FILTER5	Filter + ESD Channel 5 (Internal)
6	FILTER6	Filter + ESD Channel 6 (Internal)
7	FILTER6	Filter + ESD Channel 6 (External)
8	FILTER5	Filter + ESD Channel 5 (External)
9	FILTER4	Filter + ESD Channel 4 (External)
10	FILTER3	Filter + ESD Channel 3 (External)
11	FILTER2	Filter + ESD Channel 2 (External)
12	FILTER1	Filter + ESD Channel 1 (External)
GND PAD	GND	Device Ground

SPECIFICATIONS

MAXIMUM RATINGS

Parameter	Value	Unit
Storage Temperature Range	–65 to +150	°C
Current per Inductor	15	mA
DC Package Power Rating	500	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

STANDARD OPERATING CONDITIONS

Parameter	Rating	Unit
Operating Temperature Range	–40 to +85	°C

ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L_{TOT}	Total Channel Inductance			70		nH
R_{TOT}	Total Channel DC Resistance			45		Ω
C_{TOT_0V}	Total Channel Capacitance, 0 V bias	0 V dc; 1 MHz, 30 mV_{rms}		17.5	24	pF
$C_{TOT\_2.5V}$	Total Channel Capacitance, 2.5 V bias	2.5 V dc; 1 MHz, 30 mV_{rms}		11.5		pF
V_{ST}	Stand−off Voltage	I = 10 μA	5.5			V
I_{LEAK}	Diode Leakage Current	V_{IN} = +3.3 V		0.1	0.5	μA
V_{SIG}	Signal Clamp Voltage Positive Clamp Negative Clamp	I_{LOAD} = 10 mA I_{LOAD} = −10 mA	5.6 −1.5	6.8 −0.8	9.0 −0.4	V
V_{ESD}	In−system ESD Withstand Voltage a) Contact discharge per IEC 61000−4−2 standard, Level 4 **(External Pins)** b) Contact discharge per IEC 61000−4−2 standard, Level 4 **(Internal Pins)** c) Air discharge per IEC61000−4−2 standard, Level 4 **(External Pins)**	Notes 2 and 3	±14 ±2 ±16			kV
V_C	Clamping Voltage TLP (Note 4) See Figures 4 through 7	I_{PP} = 8 A I_{PP} = 16 A I_{PP} = −8 A I_{PP} = −16 A		13.7 20 −4.4 −7.6		V
f_C	Cut−off frequency Z_{SOURCE} = 50 Ω, Z_{LOAD} = 50 Ω			345		MHz

1. T_A = 25°C unless otherwise specified.
2. ESD applied to input and output pins with respect to GND, one at a time.
3. Unused pins are left open.
4. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

PERFORMANCE INFORMATION

TYPICAL FILTER PERFORMANCE

(T_A = 25°C, DC Bias = 0 V, 50 Ω Environment)

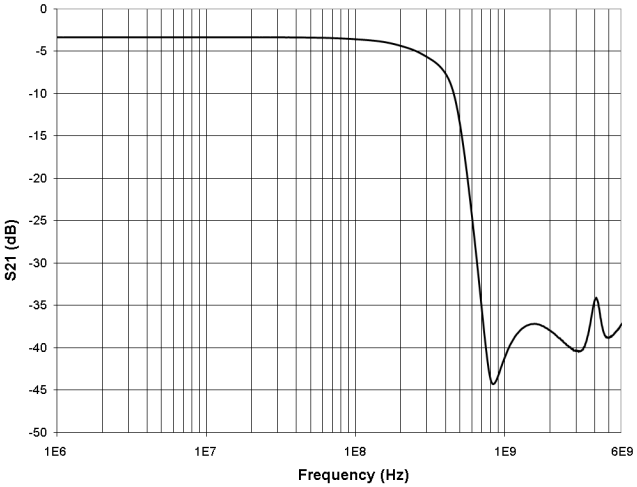


Figure 2. Typical Filter Insertion Loss

TYPICAL DIODE CAPACITANCE VS. INPUT VOLTAGE

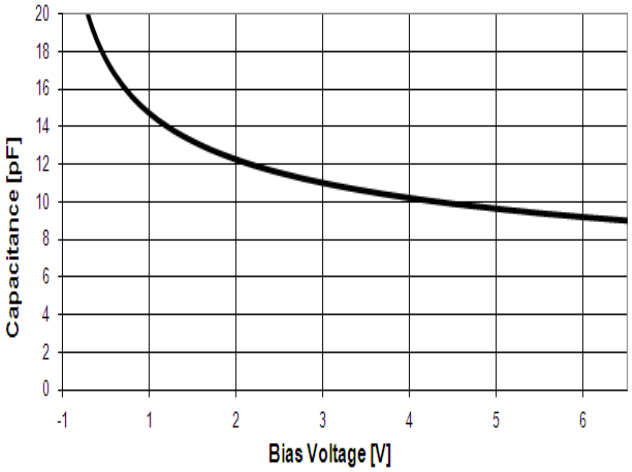


Figure 3. Filter Capacitance vs. Input Voltage (Normalized to Capacitance at 0 VDC and 25°C)

ORDERING INFORMATION

Device	Pins	Marking	Package	Shipping†
EMI9406MUTAG	12	96	UDFN12 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

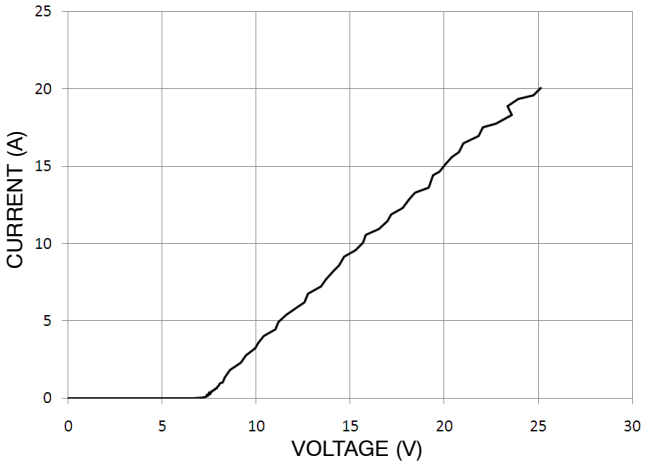


Figure 4. Positive TLP I–V Curve

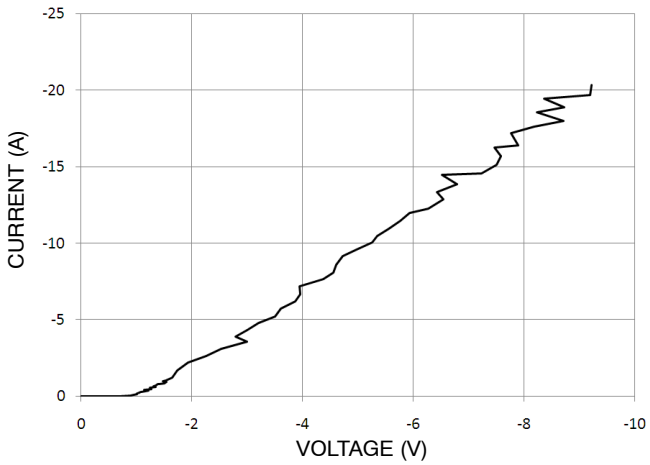


Figure 5. Negative TLP I–V Curve

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I–V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 6. TLP I–V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 7 where an 8 kV IEC 61000–4–2 current waveform into a short is compared with TLP current pulses at 8 A and 16 A, also into a short. A TLP I–V curve shows the voltage at which the device turns on, as well as how well the device clamps voltage over a range of current levels. Typical TLP I–V curves for the EMI9404 are shown in Figures 4 and 5 for positive and negative stress respectively. Application note AND9007/D gives more detail on TLP datasheet parameters, while application note AND9006/D provides a more complete explanation of the use of TLP for understanding protection product characteristics.

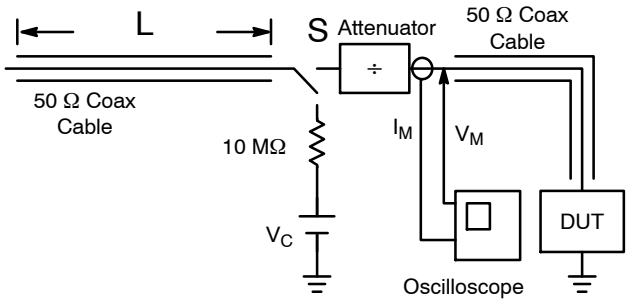


Figure 6. Simplified Schematic of a Typical TLP System

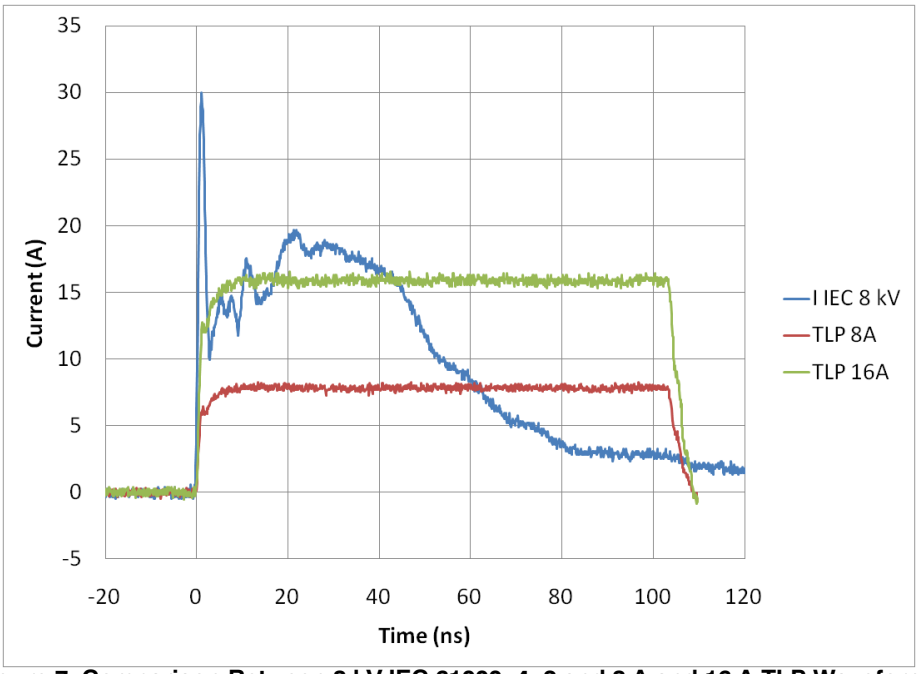


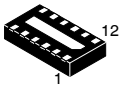
Figure 7. Comparison Between 8 kV IEC 61000–4–2 and 8 A and 16 A TLP Waveforms

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

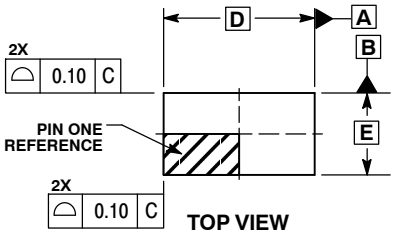
ON Semiconductor®

UDFN12, 2.5x1.35, 0.4P
CASE 517BD−01
ISSUE O

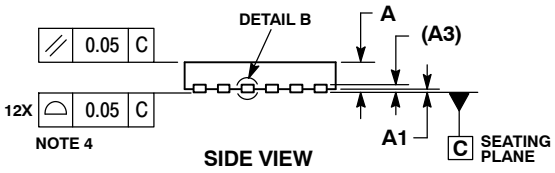
DATE 18 NOV 2009



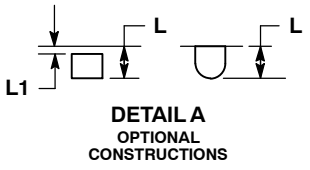
SCALE 4:1



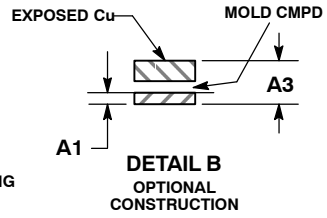
TOP VIEW



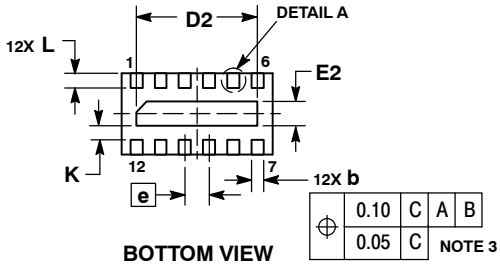
SIDE VIEW



DETAIL A
OPTIONAL CONSTRUCTIONS



DETAIL B
OPTIONAL CONSTRUCTION

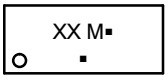


BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 mm FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	2.50 BSC	
D2	1.90	2.10
E	1.35 BSC	
E2	0.30	0.50
e	0.40 BSC	
K	0.15	−−−
L	0.20	0.30
L1	−−−	0.05

GENERIC MARKING DIAGRAM*

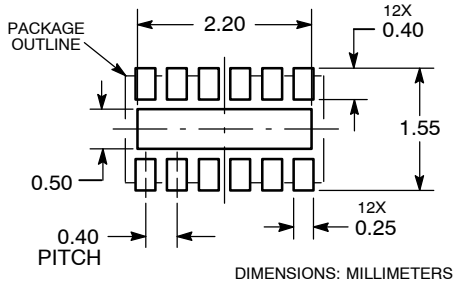


XX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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STATUS:	ON SEMICONDUCTOR STANDARD		
NEW STANDARD:			
DESCRIPTION:	UDFN12, 2.5X1.35, 0.4P		PAGE 1 OF 2

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