1.1 Scope.

This specification covers the detail requirements for a monolithic dual 8-bit CMOS multiplying digital-to-analog converter with on-chip latches for each DAC to allow easy microprocessor interface.

1.2 Part Number.

The complete part number per Tables 1 and 2 of this specification is as follows:

Device	Part Number[1]
–1	AD7528S(X)/883B
–2	AD7528T(X)/883B
–3	AD7528U(X)/883B

NOTE
[1]See paragraph 1.2.3 for package identifier.

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	Package	Description
Q	Q-20	20-Pin Cerdip
E	E-20A	20-Contact LCC

1.3 Absolute Maximum Ratings. (T_A = 25°C unless otherwise noted)

V_{DD} to AGND	0V, +17V
V_{DD} to DGND	0V, +17V
AGND to DGND	−0.3V, V_{DD} +0.3V
DGND to AGND	V_{DD}
Digital Input Voltage to DGND	−0.3V to +15V
V_{PIN2}, V_{PIN20} to AGND	−0.3V to +15V
V_{REFA}, V_{REFB} to AGND	±25V
V_{RFBA}, V_{RFBB} to DGND	±25V
Power Dissipation	
Up to +75°C	450mW
Derates above +75°C	6mW/°C
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 10sec)	+300°C

1.5 Thermal Characteristics.

Thermal Resistance θ_{JC} = 35°C/W for Q-20 and E-20A
θ_{JA} = 120°C/W for Q-20 and E-20A

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Table 1.

Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1] V_{DD} = +15V	Units
Resolution	RES	–1, 2, 3	8					Bits
Relative Accuracy	RA	–1	1	1	1			± LSB max
		–2	1/2	1	1/2	1/2		
		–3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	–1, 2, 3	1	1	1		All Grades Guaranteed Monotonic to 8 Bits Over Operating Temperature Range	± LSB max
Gain Error[2]	A_E	–1	5	4	5			± LSB max
		–2	3	4	3	2		
		–3	1	4	1	1		
Gain Tempco	dA_E/dT	–1, 2, 3	35					± ppm/°C max
Power Supply Rejection	PSRR	–1, 2, 3	0.02	0.01	0.02		ΔV_{DD} = ± 5%	± %/% max
Output Leakage Current Pin 2	I_{OL}	–1, 2, 3	200	50	200		DAC Latches Loaded with 0000 0000.	± nA max
Pin 20	I_{OL}	–1, 2, 3	200	50	200		DAC Latches Loaded with 0000 0000.	± nA max
Output Current Settling Time	t_{SL}	–1, 2, 3	350				To ± 1/2LSB; R_{OUTA}/R_{OUTB} = 100Ω, C_{OUTA}/C_{OUTB} = 13pF; $\overline{WR} = \overline{CS}$ = 0V; DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V.	ns max
Feedthrough Error[3] V_{REFA} to OUTA	FTE	–1, 2, 3	55				V_{REFA}/V_{REFB} = ± 10V, 100kHz Sinewave; DAC Latches Loaded with 0000 0000.	– dB max
V_{REFB} to OUTB	FTE	–1, 2, 3	55					
Channel-to-Channel Isolation V_{REFA} to OUTB	V_{CT}	–1, 2, 3	60				V_{REFA} = ± 10V, 100kHz Sinewave; V_{REFB} = 0V.	– dB max
V_{REFB} to OUTA		–1, 2, 3	60				V_{REFB} = ± 10V, 100kHz Sinewave; V_{REFA} = 0V.	– dB max
Reference Input Resistance V_{REFA}, V_{REFB}	R_I	–1, 2, 3	8					kΩ min
			15					kΩ max
Reference Input Resistance Match	RM_{IN}	–1, 2, 3	1	1	1			± % max
Digital Input High Voltage	V_{IH}	–1, 2, 3	13.5	13.5	13.5			V min
Digital Input Low Voltage	V_{IL}	–1, 2, 3	1.5	1.5	1.5			V max
Digital Input Leakage Current	I_{IN}	–1, 2, 3	10	1	10		V_{IN} = 0V or V_{DD}	± μA max
Digital Input Capacitance DB0–DB7	C_I	–1, 2, 3	10					pF max
$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/DACB			15					
Output Capacitance Pin 2	C_O	–1, 2, 3	50				DAC Latches Loaded with 0000 0000.	pF max
Pin 20	C_O	–1, 2, 3	50					
Pin 2	C_O	–1, 2, 3	120				DAC Latches Loaded with 1111 1111.	pF max
Pin 20	C_O	–1, 2, 3	120					
Supply Current from V_{DD}	I_{DD}	–1, 2, 3	2				All Digital Inputs = V_{IL} or V_{IH}	mA max
	I_{DD}	–1, 2, 3	500	100	500		All Digital Inputs = 0V or V_{DD}	μA max
Chip Select to Write Setup Time[4]	t_{CS}	–1, 2, 3	180					ns min
Chip Select to Write Hold Time[4]	t_{CH}	–1, 2, 3	10					ns min
DAC Select to Write Setup Time[4]	t_{AS}	–1, 2, 3	180					ns min
DAC Select to Write Hold Time[4]	t_{AH}	–1, 2, 3	10					ns min
Data Valid to Write Setup Time[4]	t_{DS}	–1, 2, 3	180					ns min
Data Valid to Write Hold Time[4]	t_{DH}	–1, 2, 3	10					ns min
Write Pulse Width[4]	t_{WR}	–1, 2, 3	180					ns min

NOTES

[1] $V_{OUTA} = V_{OUTB}$ = 0V; V_{REF} = + 10V unless otherwise stated.

[2] Measured using internal R_{FB} and includes effect of leakage current and gain TC.

[3] Feedthrough error can be reduced by connecting the lid on the package to ground.

[4] Timing per Figure 1.

Table 2.

Test	Symbol	Device	Design Limit T_{min}–T_{max}	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition[1] V_{DD} = +5V	Units
Resolution	RES	–1, 2, 3	8					Bits
Relative Accuracy	RA	–1	1	1	1			± LSB max
		–2	1/2	1	1/2	1/2		
		–3	1/2	1	1/2	1/2		
Differential Nonlinearity	DNL	–1, 2, 3	1	1	1		All Grades Guaranteed Monotonic to 8 Bits Over Operating Temperature Range	± LSB max
Gain Error[2]	A_E	–1	6	4	6			± LSB max
		–2	4	4	4	2		
		–3	3	4	3	1		
Gain Tempco	dA_E/dT	–1, 2, 3	70					± ppm/°C max
Power Supply Rejection	PSRR	–1, 2, 3	0.04	0.02	0.04		ΔV_{DD} = ± 5%	± %/% max
Output Leakage Current Pin 2	I_{OL}	–1, 2, 3	400	50	400		DAC Latches Loaded with 0000 0000.	± nA max
Pin 20	I_{OL}	–1, 2, 3	400	50	400		DAC Latches Loaded with 0000 0000.	± nA max
Output Current Settling Time	t_{SL}	–1, 2, 3	600				To ± 1/2LSB; R_{OUTA}/R_{OUTB} = 100Ω, C_{OUTA}/C_{OUTB} = 13pF; $\overline{WR} = \overline{CS}$ = 0V; DB0–DB7 = 0V to V_{DD} or V_{DD} to 0V.	ns max
Feedthrough Error[3] V_{REFA} to OUTA	FTE	–1, 2, 3	55				V_{REFA}/V_{REFB} = ± 10V, 100kHz Sinewave; DAC Latches Loaded with 0000 0000.	– dB max
V_{REFB} to OUTB	FTE	–1, 2, 3	55					
Channel-to-Channel Isolation V_{REFA} to OUTB	V_{CT}	–1, 2, 3	60				V_{REFA} = ± 10V, 100kHz Sinewave; V_{REFB} = 0V.	– dB max
V_{REFB} to OUTA		–1, 2, 3	60				V_{REFB} = ± 10V, 100kHz Sinewave; V_{REFA} = 0V.	– dB max
Reference Input Resistance V_{REFA}, V_{REFB}	R_I	–1, 2, 3	8	8	8			kΩ min
			15	15	15			kΩ max
Reference Input Resistance Match	RM_{IN}	–1, 2, 3	1					± % max
Digital Input High Voltage	V_{IH}	–1, 2, 3	2.4	2.4	2.4			V min
Digital Input Low Voltage	V_{IL}	–1, 2, 3	0.8	0.8	0.8			V max
Digital Input Leakage Current	I_{IN}	–1, 2, 3	10				V_{IN} = 0V or V_{DD}	± μA max
Digital Input Capacitance DB0–DB7	C_I	–1, 2, 3	10					pF max
$\overline{WR}$, $\overline{CS}$, $\overline{DACA}$/$\overline{DACB}$			15					
Output Capacitance Pin 2	C_O	–1, 2, 3	50				DAC Latches Loaded with 0000 0000.	pF max
Pin 20	C_O	–1, 2, 3	50					
Pin 2	C_O	–1, 2, 3	120				DAC Latches Loaded with 1111 1111.	pF max
Pin 20	C_O	–1, 2, 3	120					
Supply Current from V_{DD}	I_{DD}	–1, 2, 3	2	2	2		All Digital Inputs = V_{IL} or V_{IH}	mA max
	I_{DD}	–1, 2, 3	500				All Digital Inputs = 0V or V_{DD}	μA max
Chip Select to Write Setup Time[4]	t_{CS}	–1, 2, 3	250					ns min
Chip Select to Write Hold Time[4]	t_{CH}	–1, 2, 3	20					ns min
DAC Select to Write Setup Time[4]	t_{AS}	–1, 2, 3	250					ns min
DAC Select to Write Hold Time[4]	t_{AH}	–1, 2, 3	20					ns min
Data Valid to Write Setup Time[4]	t_{DS}	–1, 2, 3	220					ns min
Data Valid to Write Hold Time[4]	t_{DH}	–1, 2, 3	10					ns min
Write Pulse Width[4]	t_{WR}	–1, 2, 3	220					ns min

NOTES
[1] $V_{OUTA} = V_{OUTB}$ = 0V; V_{REF} = +10V unless otherwise stated.
[2] Measured using internal R_{FB} and includes effect of leakage current and gain TC.
[3] Feedthrough error can be reduced by connecting the lid on the package to ground.
[4] Timing per Figure 1.

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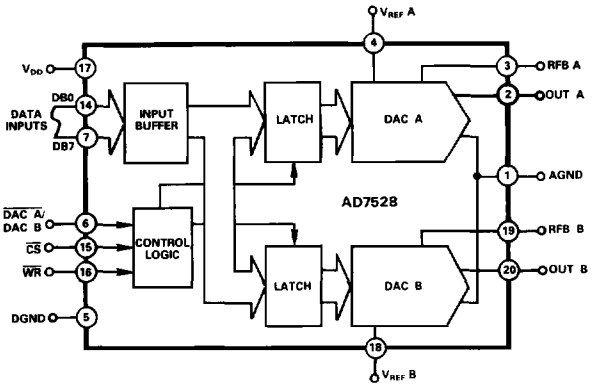
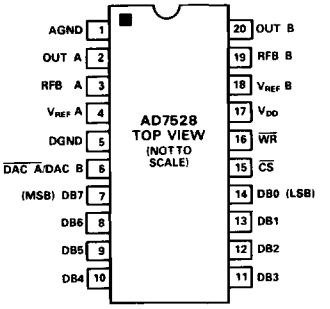
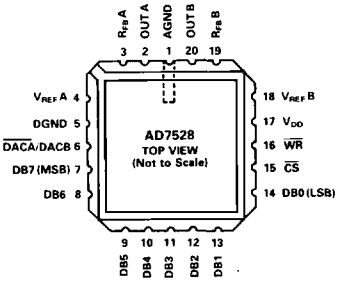
DIGITAL-TO-ANALOG CONVERTERS

3.2.1 Functional Block Diagram and Terminal Assignments.





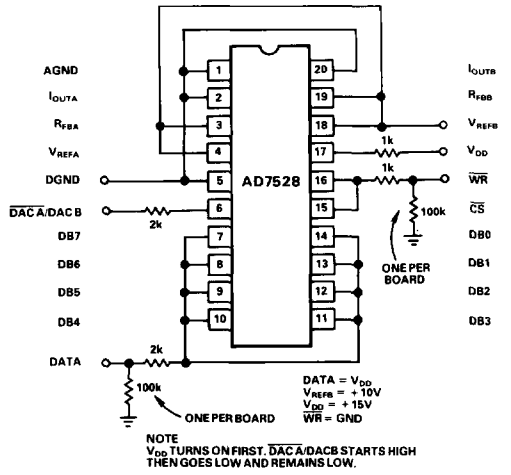


3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).

4.2.1 Life Test/Burn-In Circuit.

Steady state life test is per MIL-STD-883 Method 1005. Burn-in is per MIL-STD-883 Method 1015 test condition (B).



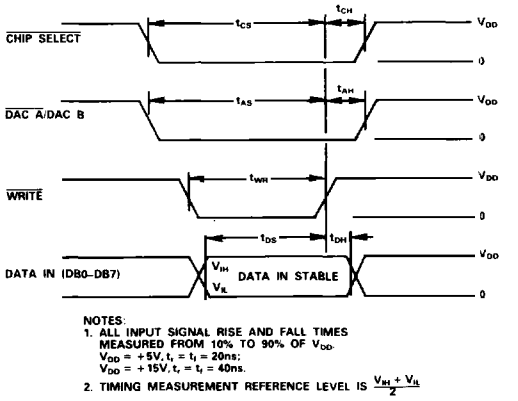


Figure 1. Write Cycle Timing Diagram

Table 3. Mode Selection Table

DAC A/ DAC B	CS	WR	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State H = High State X = Don't Care