

BTA201-800ER

3Q Hi-Com Triac
15 October 2012

Product data sheet

1. Product profile

1.1 General description

Planar passivated high commutation three quadrant triac in a SOT54 (TO-92) plastic package. This "series ER" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers. It has reverse pinning to that of the standard triac in this package.

1.2 Features and benefits

- 3Q technology for improved noise immunity
- Direct triggering from low power drivers and logic ICs
- High commutation capability with sensitive gate
- High immunity to false turn-on by dV/dt
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Reverse pinning version (ER)
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only

1.3 Applications

- General purpose motor control
- Small loads in washing machines
- Solenoid drivers

1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{\text{j(init)}} = 25\text{ }^{\circ}\text{C}$; $t_{\text{p}} = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	12.5	A
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{lead}} \leq 54\text{ }^{\circ}\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	1	A



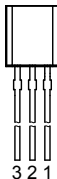
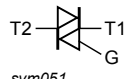
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _J = 25 °C; Fig. 7	1	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _J = 25 °C; Fig. 7	1	-	10	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _J = 25 °C; Fig. 7	1	-	10	mA

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>TO-92 (SOT54)</p>	 <p>sym051</p>
2	G	gate		
3	T2	main terminal 2		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BTA201-800ER	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _{lead} ≤ 54 °C; Fig. 1 ; Fig. 2 ; Fig. 3	-	1	A
I _{TSM}	non-repetitive peak on-state current	full sine wave; T _{J(init)} = 25 °C; t _p = 16.8 ms	-	13.7	A
		full sine wave; T _{J(init)} = 25 °C; t _p = 20 ms; Fig. 4 ; Fig. 5	-	12.5	A
I ² t	I ² t for fusing	t _p = 10 ms; SIN	-	0.78	A ² s

Symbol	Parameter	Conditions	Min	Max	Unit
di_T/dt	rate of rise of on-state current	I_T 1.5 A; I_G 0.2 A; $di_G/dt = 0.2$ A/ μ s	-	100	A/ μ s
I_{GM}	peak gate current		-	2	A
P_{GM}	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_j	junction temperature		-40	125	$^{\circ}$ C

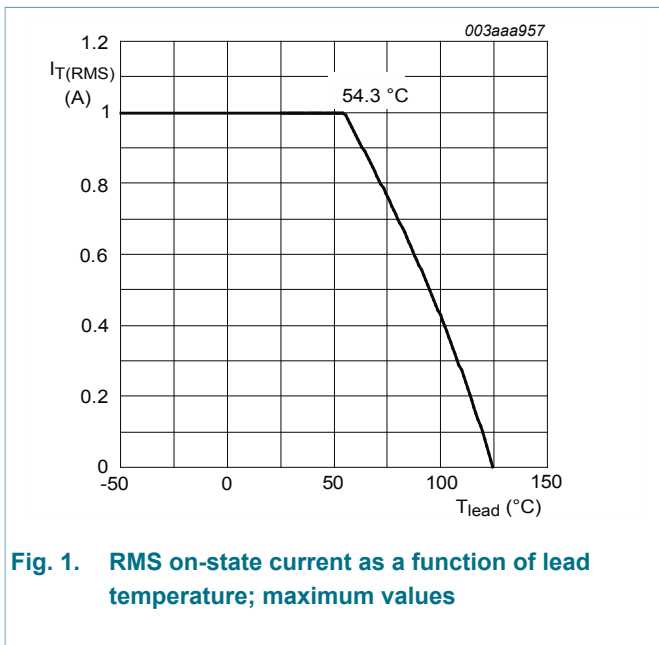


Fig. 1. RMS on-state current as a function of lead temperature; maximum values

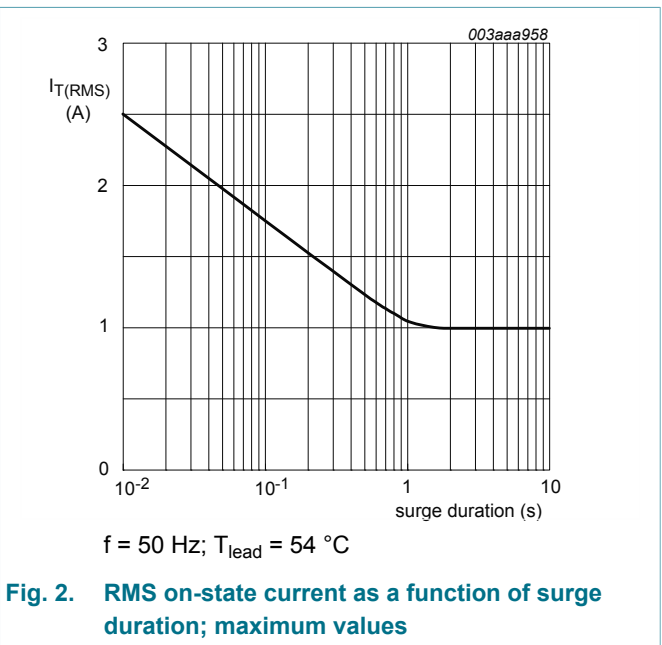


Fig. 2. RMS on-state current as a function of surge duration; maximum values

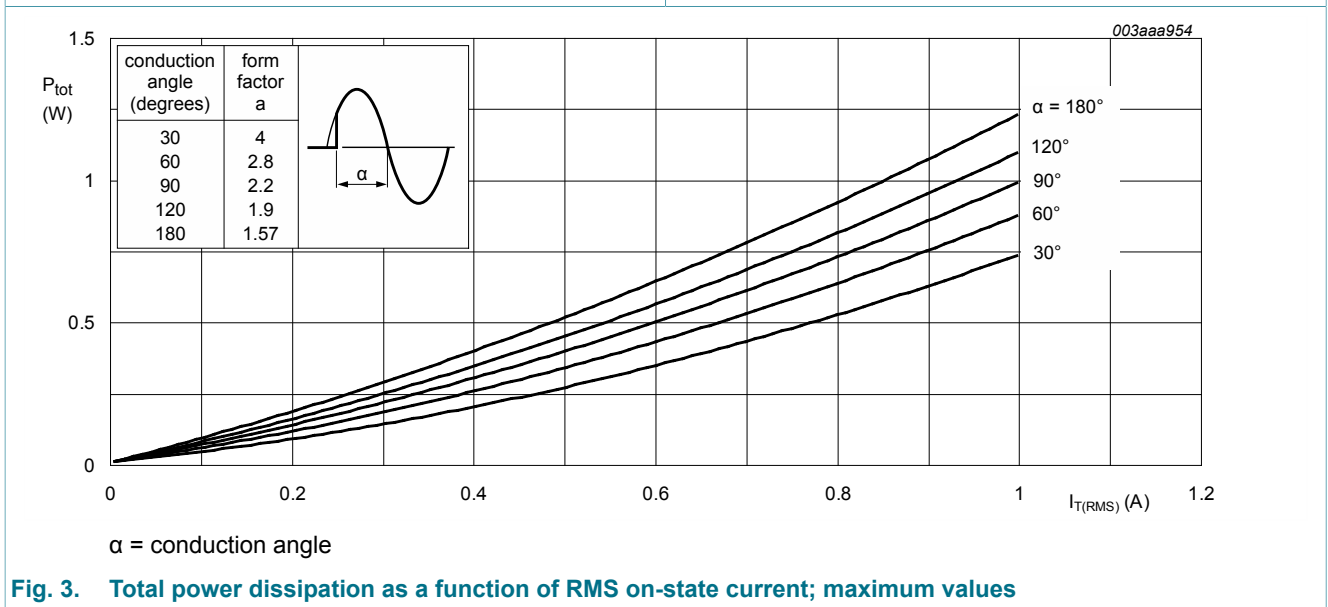


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

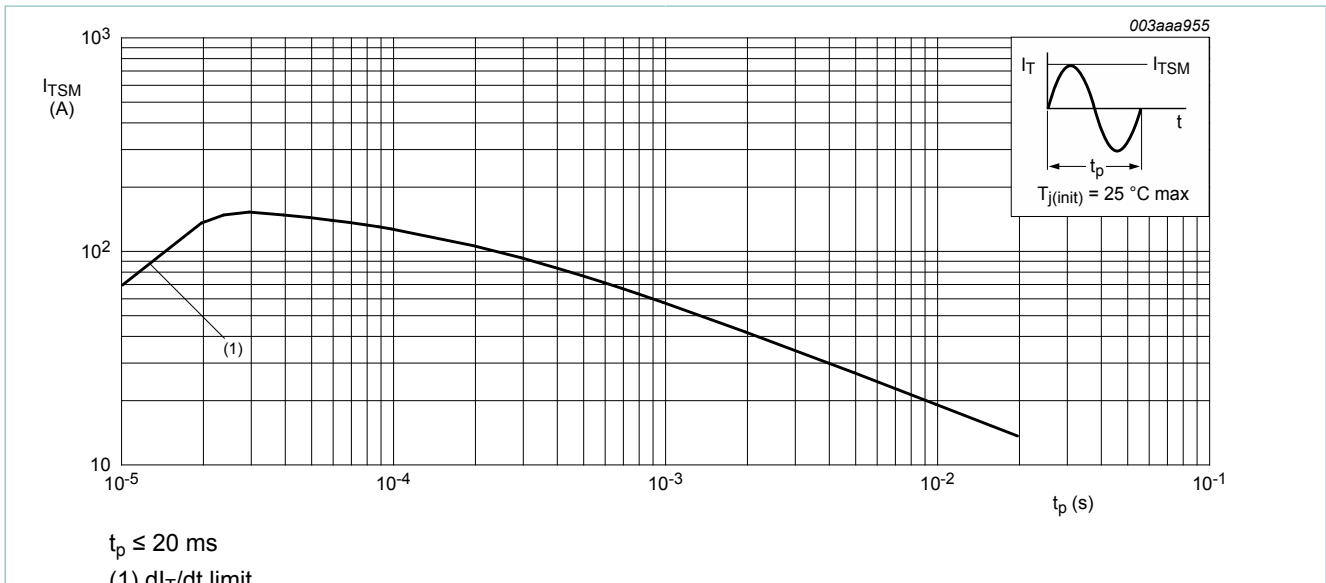


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

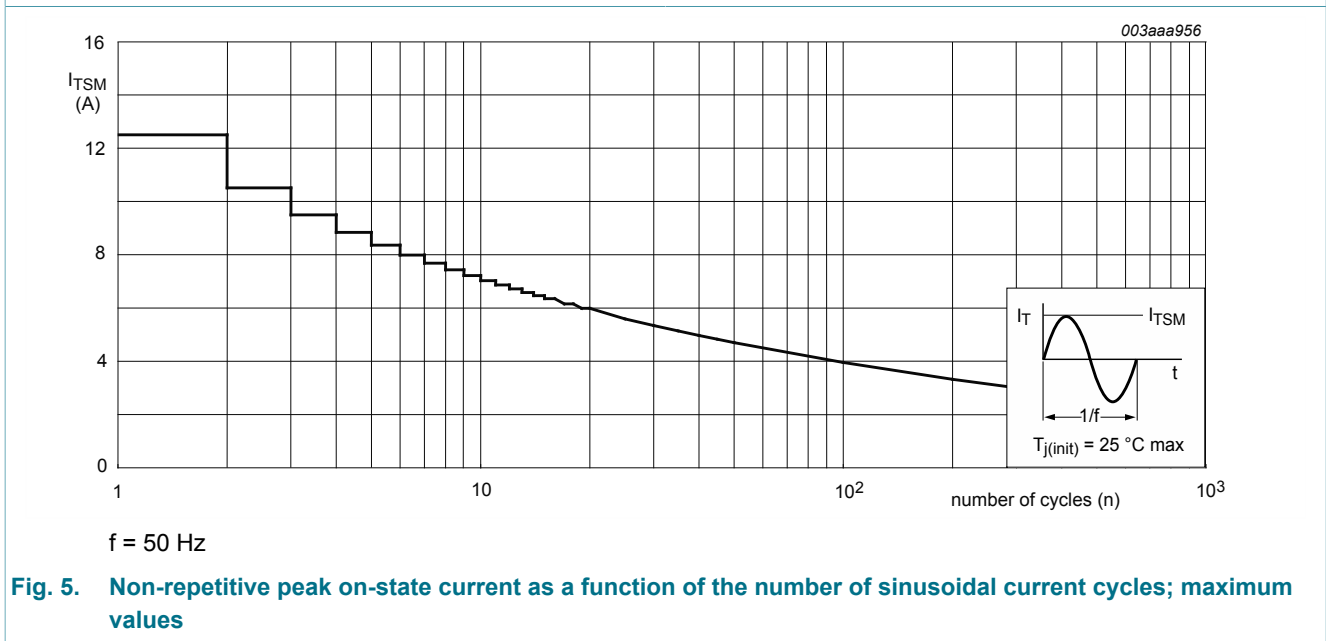
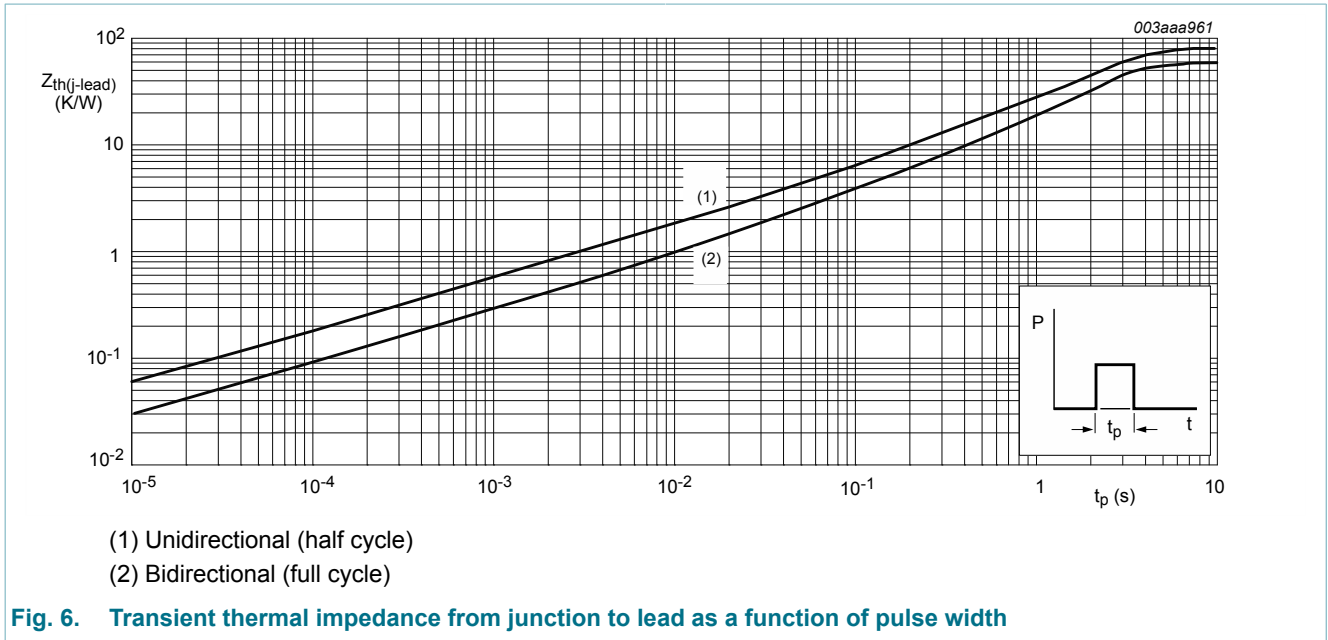


Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle; Fig. 6	-	-	60	K/W
		half cycle; Fig. 6	-	-	80	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient		-	150	-	K/W

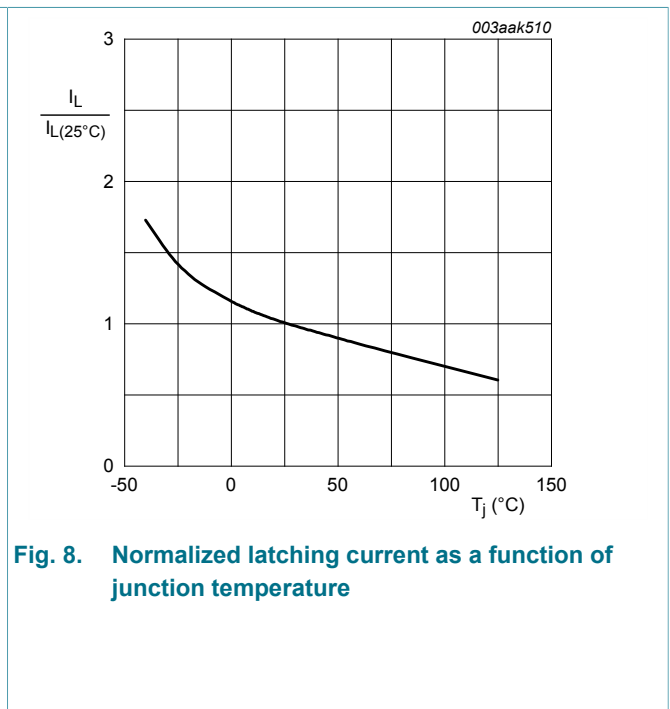
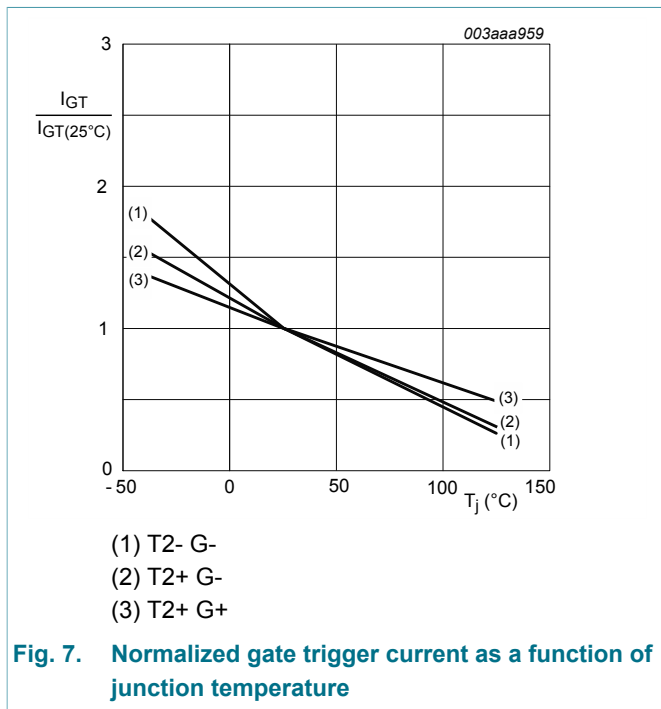


6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G+;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 7	1	-	10	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 7	1	-	10	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 7	1	-	10	mA
I_L	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2+ G+;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	12	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2+ G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	20	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2- G-;$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	12	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 9	-	-	12	mA
V_T	on-state voltage	$I_T = 1.4\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 10	-	1.2	1.5	V
V_{GT}	gate trigger voltage	$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125\text{ }^\circ\text{C};$ Fig. 11	0.2	0.3	-	V
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 11	-	0.7	1.5	V
I_D	off-state current	$V_D = 800\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	600	-	-	V/ μs
di_{com}/dt	rate of change of commutating current	$V_D = 400 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$; $I_{T(RMS)} = 1 \text{ A}$; $dV_{com}/dt = 20 \text{ V/s}$; (snubberless condition); gate open circuit	2.5	-	-	A/ms
		$V_D = 400 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$; $I_{T(RMS)} = 1 \text{ A}$; $dV_{com}/dt = 10 \text{ V}/\mu\text{s}$; gate open circuit	3.5	-	-	A/ms



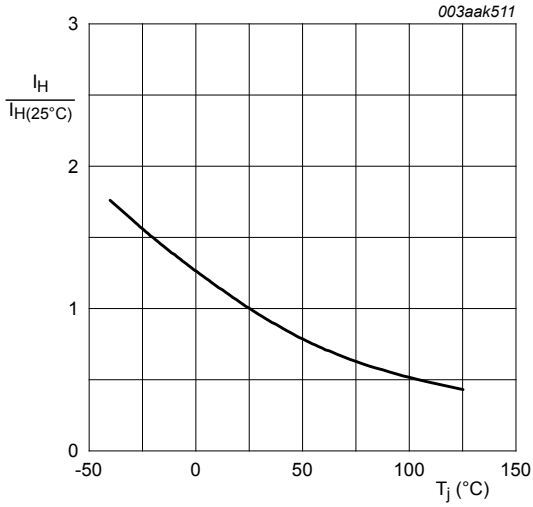
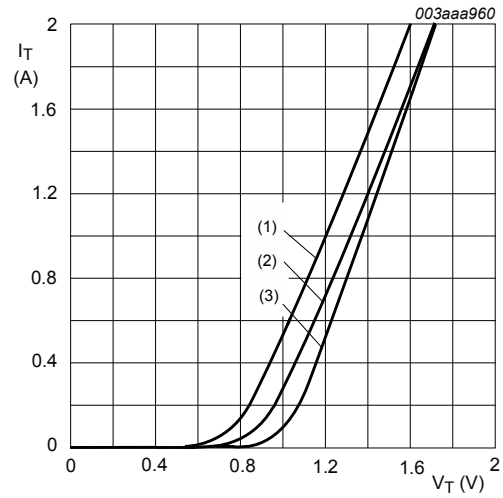


Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 1.02 \text{ V}; R_s = 0.358 \Omega$

- (1) $T_j = 125 \text{ }^\circ\text{C}$; typical values
- (2) $T_j = 125 \text{ }^\circ\text{C}$; maximum values
- (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

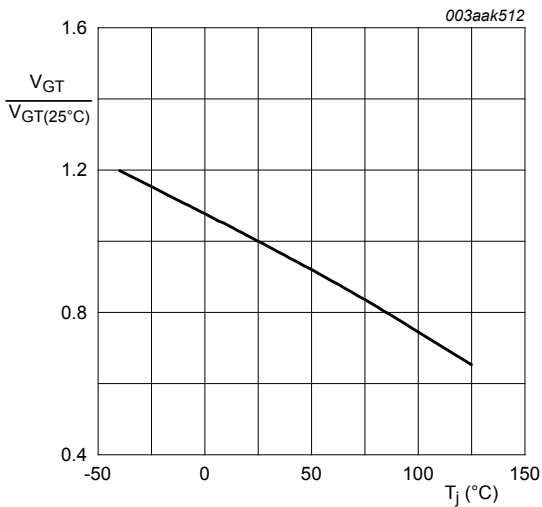


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

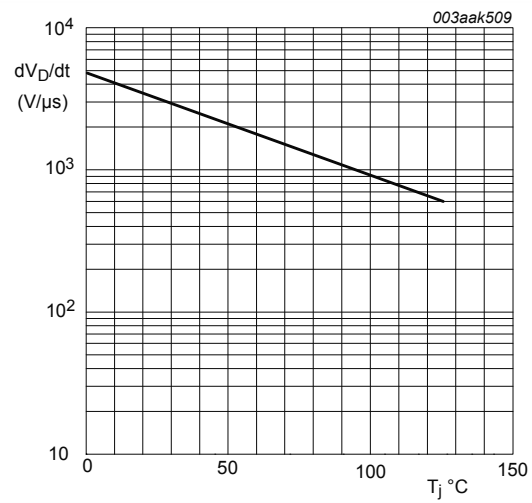


Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values

7. Package outline

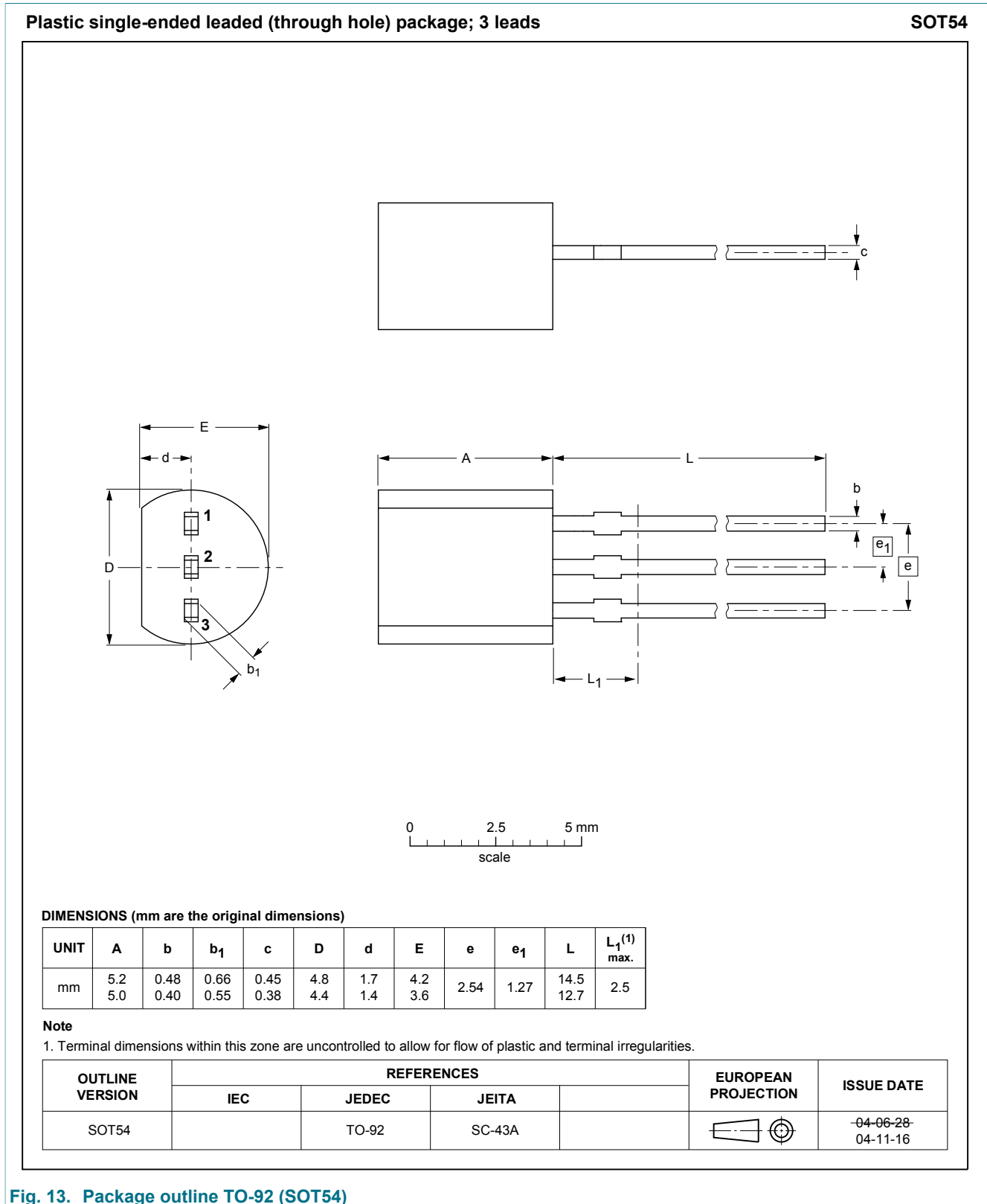


Fig. 13. Package outline TO-92 (SOT54)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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9. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
1.4	Quick reference data	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	4
6	Characteristics	5
7	Package outline	8
8	Legal information	9
8.1	Data sheet status	9
8.2	Definitions	9
8.3	Disclaimers	9
8.4	Trademarks	10

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