REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	Add device type 03. Add case outline Y. Change supply voltage range, changes to table I. Editorial changes throughout. Change drawing CAGE number to 67268.	20 Aug 87	

REV	A																													
PAGE	28																													
REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF PAGES	PAGES	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27		

Defense Electronics Supply Center Dayton, Ohio Original date of drawing: 20 May 1986 AMSC N/A	PREPARED BY: Greg A. Pitz CHECKED BY: APPROVED BY:	**MILITARY DRAWING** This drawing is available for use by all Departments and Agencies of the Department of Defense TITLE: MICROPROCESSOR, 16-BIT, N-CHANNEL, MONOLITHIC SILICON MICROCIRCUIT
	SIZE: A CODE IDENT. NO.: 67268 REV: A	DWG NO.: 5962-85148 PAGE 1 OF 28

5962-E534

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-85148	01	X	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	M80286-8	8 MHz	16-bit microprocessor
02	M80286-6	6 MHz	16-bit microprocessor
03	M80286-10	10 MHz	16-bit microprocessor

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
X	P-AC 68-terminal (1.160" by 1.160") pin grid array
Y	68-terminal ceramic quad package (see figure 3)

1.3 Absolute maximum ratings.

Supply voltage range with respect to ground (V_{CC})	-1.0 to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) (per device type)	3.3 W dc
Lead temperature (soldering, 5 seconds)	+300°C
Junction temperature (T_J)	+200°C
Thermal resistance, junction-to-case (θ_{JC})	+9.5°C/W

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	4.75 V dc minimum to 5.25 V dc maximum
Minimum high level input voltage (V_{IH}):	
Logic inputs	2.0 V dc to V_{CC+} .5 V dc
Clock input	3.8 V dc to V_{CC+} .5 V dc
Maximum low level input voltage (V_{IL}):	
Logic inputs	-0.5 V dc to 0.8 V dc
Clock input	-0.5 V dc to 0.6 V dc
Minimum high level output voltage	2.4 V dc
Maximum low level output voltage	0.45 V dc
Frequency of operation:	
01	8 MHz
02	6 MHz
03	10 MHz
Case operating temperature range	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outlines. The case outlines shall be in accordance with 1.2.2 and figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C < T_C < +125°C$ unless otherwise specified V_{CC} = 5.0 V ±5%	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		All	1, 2, 3	-0.5	0.8	V
Input high voltage	V_{IH}		All	1, 2, 3	2.0	V_{CC}+ 0.5	V
CLK input low voltage	V_{ILC}		All	1, 2, 3	-0.5	0.6	V
CLK input high voltage	V_{IHC}		All	1, 2, 3	3.8	V_{CC}+ 0.5	V
Output low voltage	V_{OL}	I_{OL} = 2.0 mA	All	1, 2, 3		0.45	V
Output high voltage	V_{OH}	I_{OH} = -400 µA	All	1, 2, 3	2.4		V
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ V_{CC}	All	1, 2, 3		±10	µA
Input sustaining current on $\overline{BUSY}$ and $\overline{ERROR}$ pins	I_{IL}	V_{IN} = 0 V	All	1, 2, 3	30	500	µA
Output leakage current	I_{LO1}	0.45 V ≤ V_{OUT} ≤ V_{CC}	All	1, 2, 3		±20	µA
Output leakage current 1/	I_{LO2}	0 V ≤ V_{OUT} ≤ 0.45 V	All	1, 2, 3		±1	mA
Supply current 2/	I_{CC}		All	1, 2, 3		600	mA
CLK input capacitance	C_{CLK}	F_c = 1 MHz See 4.3.1c	All	4		20	pF
Other input capacitance	C_{IN}	F_c = 1 MHz See 4.3.1c	All	4		10	pF
Input/Output capacitance	C_O	F_c = 1 MHz See 4.3.1c	All	4		20	pF

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	3/ Waveform reference	Conditions $-55°C < T_C < +125°C$ unless otherwise specified V_{CC} = 5.0 V ±5%	Device type	Group A subgroups	Limits Min	Limits Max	Unit
System clock period	1		01	9, 10, 11	1/ 62	250	ns
			02		83	250	
			03		50	250	
System clock low time	2	@ 1.0 V	01	9, 10, 11	1/ 15	225	ns
			02		20	225	
			03		12	234	
System clock high time	3	@ 3.6 V	01	9, 10, 11	1/ 25	1/ 235	ns
			02		1/ 25	230	
			03		1/ 16	238	
1/ System clock rise time		1.0 V to 3.6 V	01, 02	9, 10, 11		10	ns
			03			8	
1/ System clock fall time		3.6 V to 1.0 V	01, 02	9, 10, 11		10	ns
			03			8	
Asynchronous input setup time 4/	4		01, 03	9, 10, 11	20		ns
			02		30		
Asynchronous input hold time 5/	5		01, 03	9, 10, 11	20		ns
			02		30		
RESET setup time	6		01	9, 10, 11	28		ns
			02		33		
			03		23		
RESET hold time	7		All	9, 10, 11	5		ns
Read data setup time	8		01	9, 10, 11	10		ns
			02		20		
			03		8		

See footnotes at end of table.

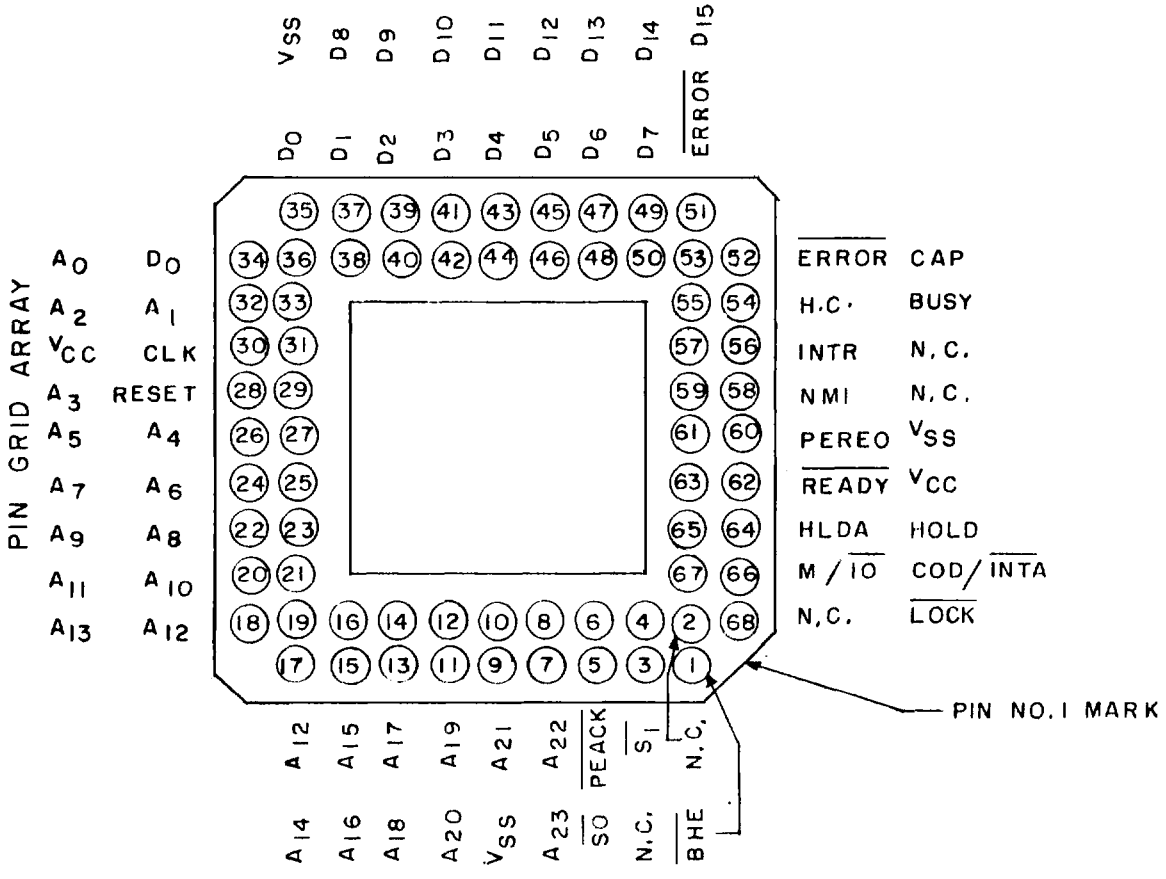
TABLE I. Electrical performance characteristics - Continued.

Test	3/ Waveform reference	Conditions $-55°C < T_C < +125°C$ unless otherwise specified V_{CC} = 5.0 V ±5%	Device type	Group A subgroups	Limits Min	Limits Max	Unit
Read data hold time	9		All	9, 10, 11	8		ns
$\overline{\text{Ready}}$ setup time	10		01	9, 10, 11	38		ns
			02		50		
			03		26		
$\overline{\text{Ready}}$ hold time	11		01, 03	9, 10, 11	25		ns
			02		35		
Status/$\overline{\text{PEACK}}$ valid delay	12	5/, 6/	01	9, 10, 11	1	40	ns
			02		1	55	
			03		1	22	
Address valid delay	13	5/, 6/	01	9, 10, 11	1	60	ns
			02		1	80	
			03		1	47	
Write data valid delay	14	5/, 6/	01	9, 10, 11	1/ 0	50	ns
			02		1/ 0	65	
			03		0	40	
Address/status/data float delay	15	5/, 7/	01	9, 10, 11	0	50	ns
			02		0	80	
			03		0	47	
HLDA valid delay	16	5/, 6/	01	9, 10, 11	0	50	ns
			02		0	80	
			03		0	47	

1/ Guaranteed if not tested.
2/ Low temperature is worst case.
3/ See figure 4.
4/ Asynchronous inputs are INTR, NMI, HOLD, PEREQ, $\overline{\text{ERROR}}$, and $\overline{\text{BUSY}}$. This specification is given only for testing purposes to assure recognition at a specific CLK edge.
5/ Delay from 0.8 V on the CLK to 0.8 V or 2.0 V or float on the output as appropriate for valid or floating condition.
6/ Output load: C_L = 100 pF.
7/ Float condition occurs when output current is less than I_{LO} in magnitude.

Case X

Component pad view -- As viewed from underside of component when mounted on the board.

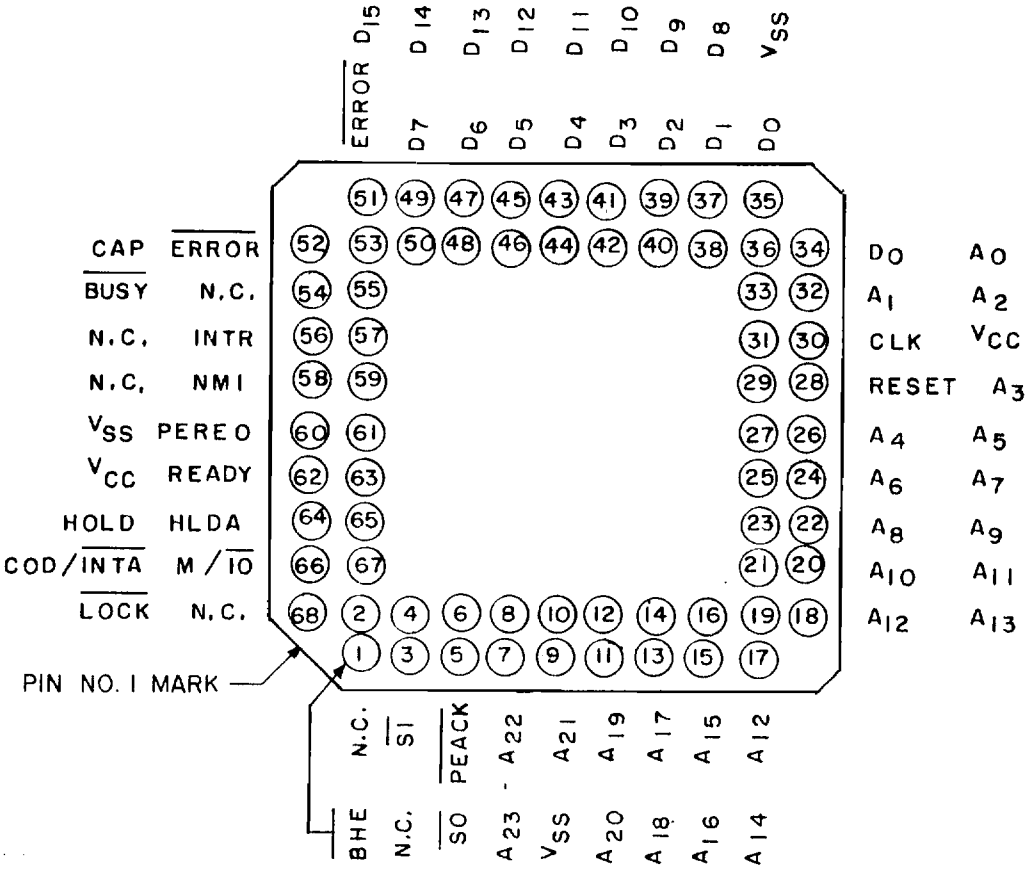


NOTE: N.C. signals must not be connected.

FIGURE 1. Terminal connections.

Case X

P.C. Board View -- As viewed
from the component side of
the P.C. board.



NOTE: N.C. signals must not be connected.

FIGURE 1. Terminal connections - Continued.

Case Y

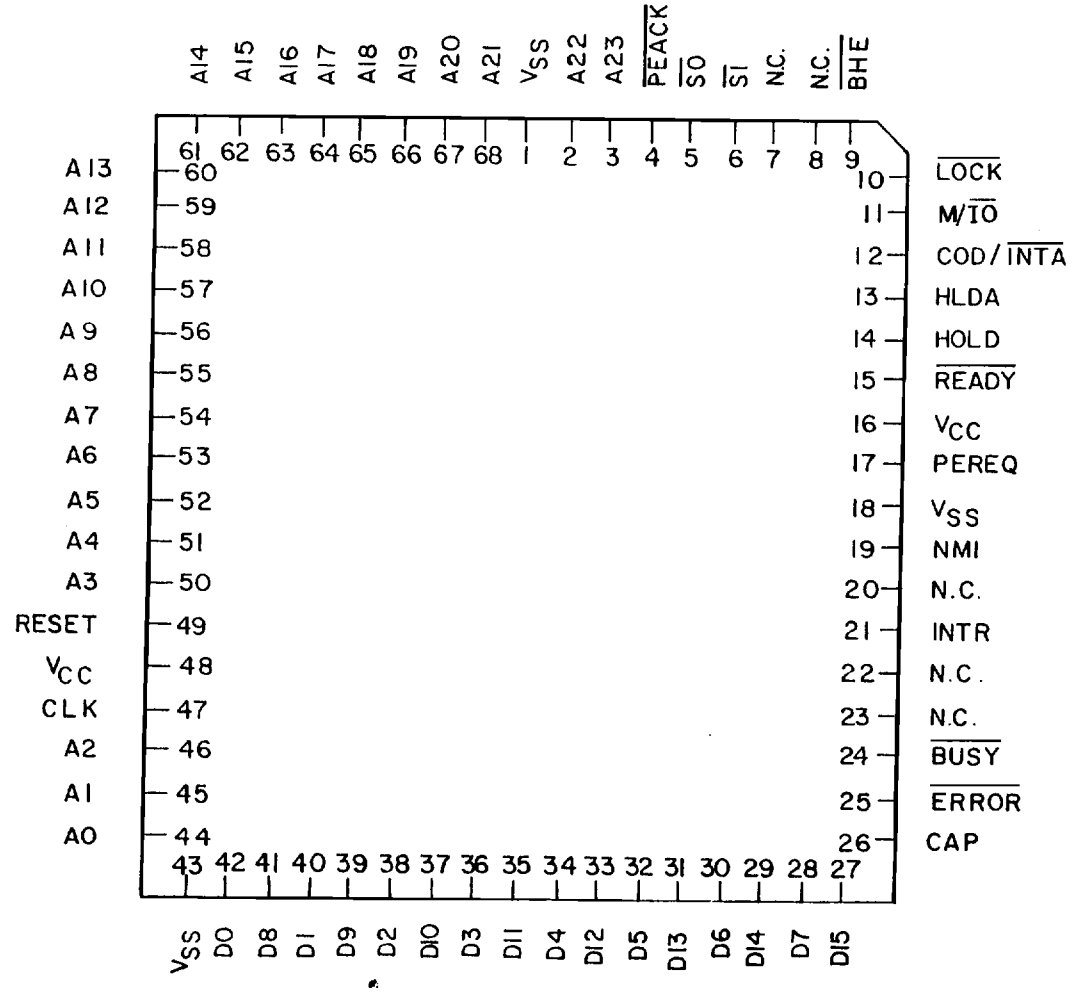


FIGURE 1. Terminal connections - Continued.

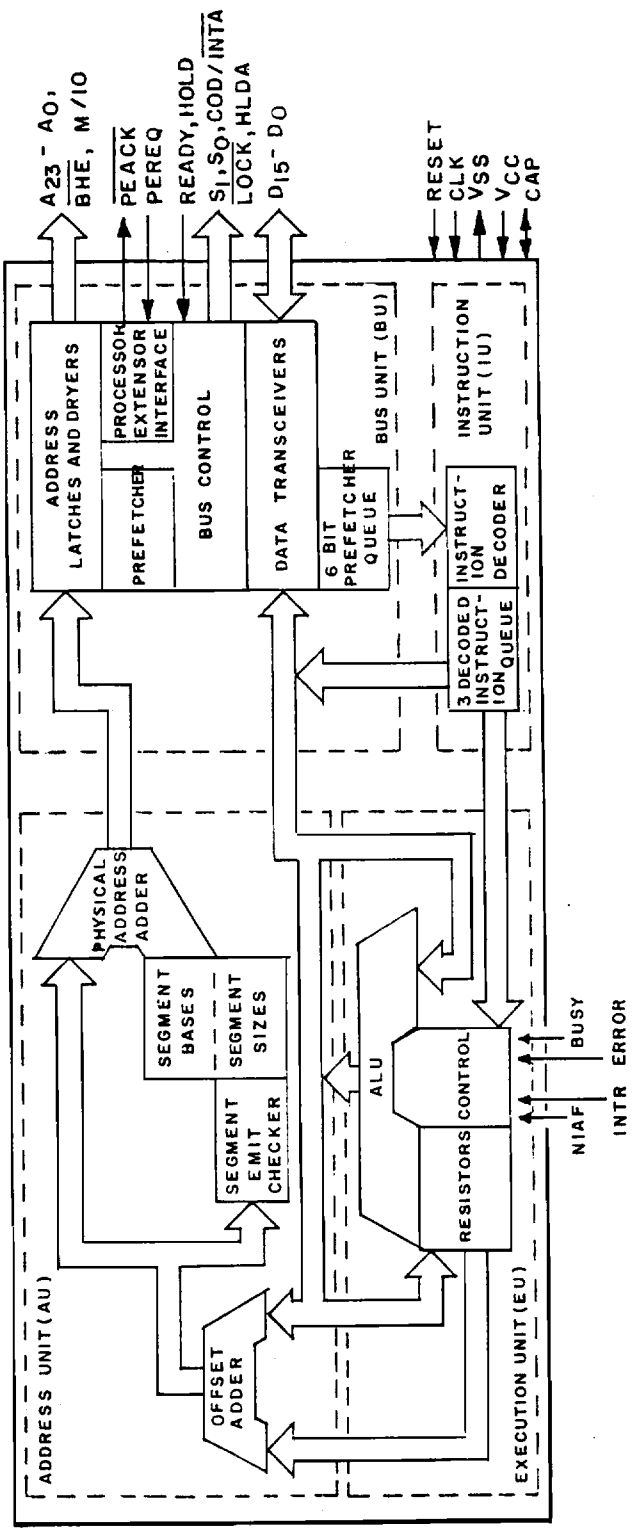


FIGURE 2. Internal block diagram.

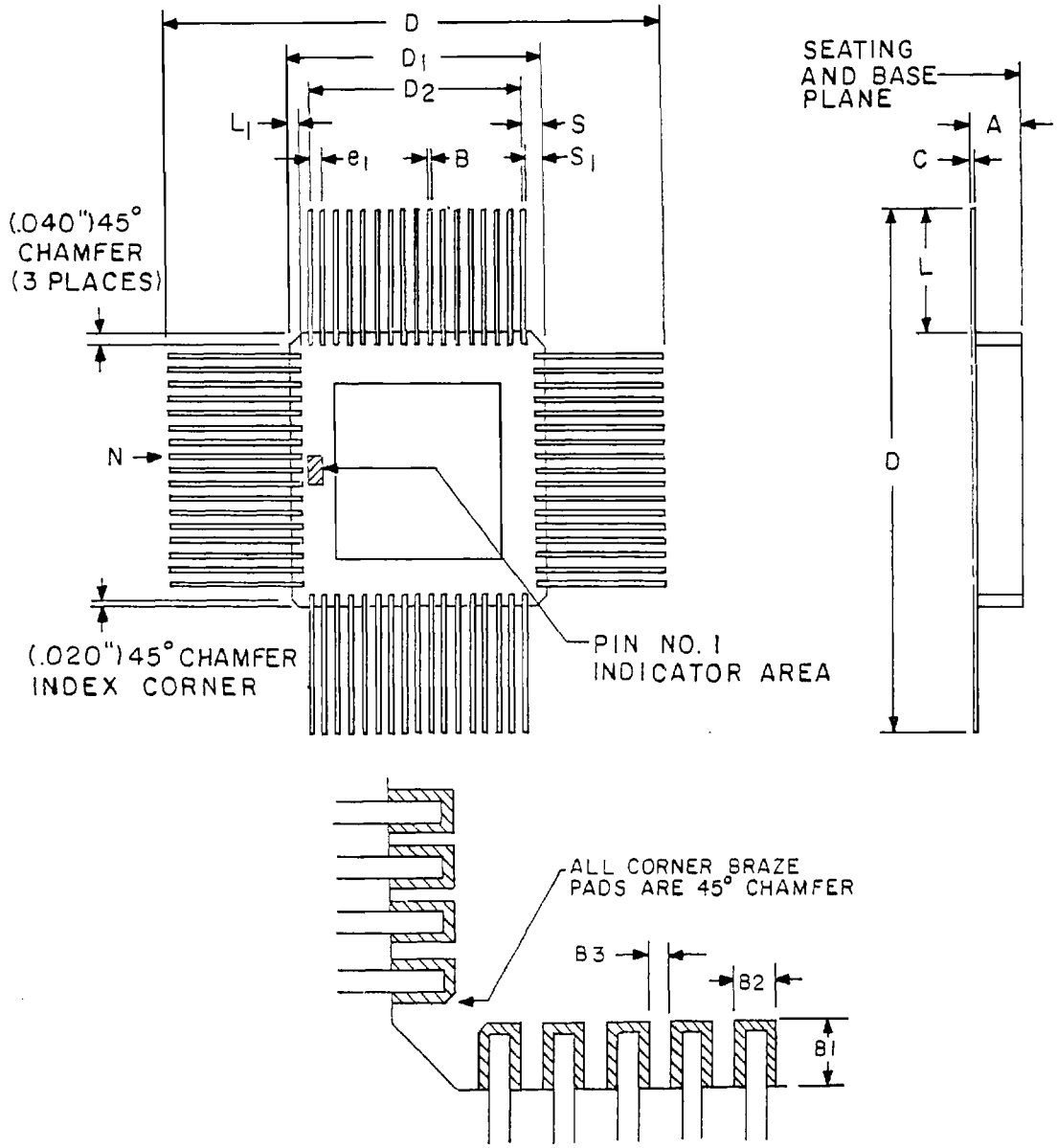


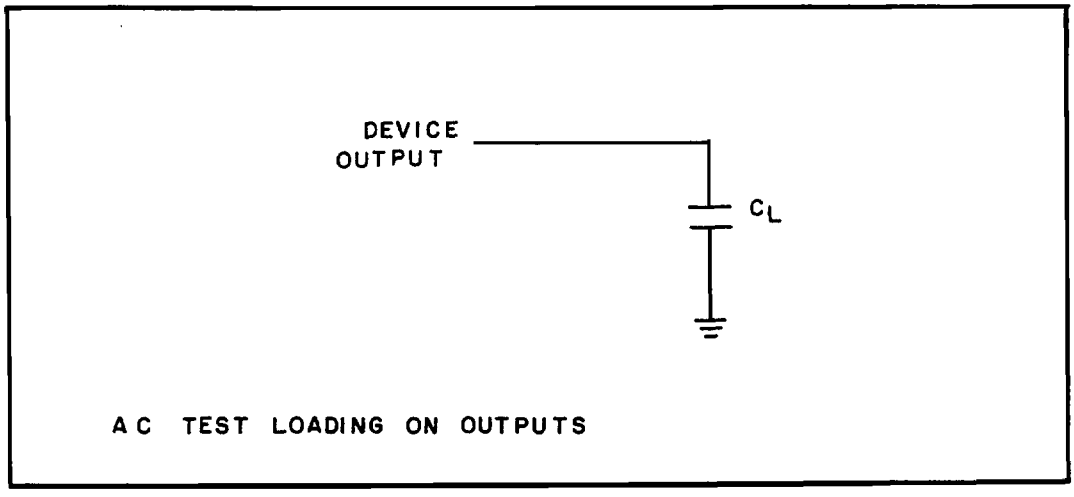
FIGURE 3. Case outline Y.

MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO	SIZE A	CODE IDENT. NO. 67268	DWG NO. 5962-85148
		REV A	PAGE 11

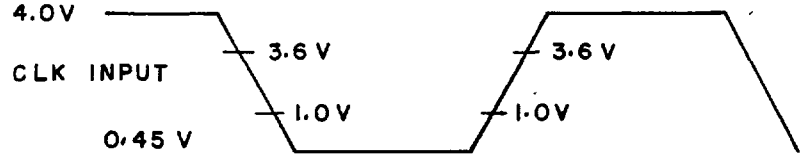
DESC FORM 193A
FEB 86

Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	0.080	0.106	2.03	2.69
B	0.016	0.020	0.41	0.51
B_1	0.040	0.060	1.02	1.52
B_2	0.030	0.040	0.76	1.02
B_3	0.005	0.020	0.13	0.51
C	0.008	0.012	0.20	0.31
D	1.640	1.870	41.66	47.50
D_1	0.935	0.970	23.75	24.64
D_2	0.800 BSC		20.32 BSC	
e_1	0.050 BSC		1.27 BSC	
L	0.375	0.450	9.53	11.43
L_1	0.040	0.060	1.02	1.52
N	68		68	
S	0.066	0.087	1.68	2.21
S_1	0.050		1.27	

FIGURE 3. Case outline Y - Continued.



A C TEST LOADING ON OUTPUTS



A C DRIVE AND MEASUREMENT POINTS - CLK INPUT

FIGURE 4. Waveforms.

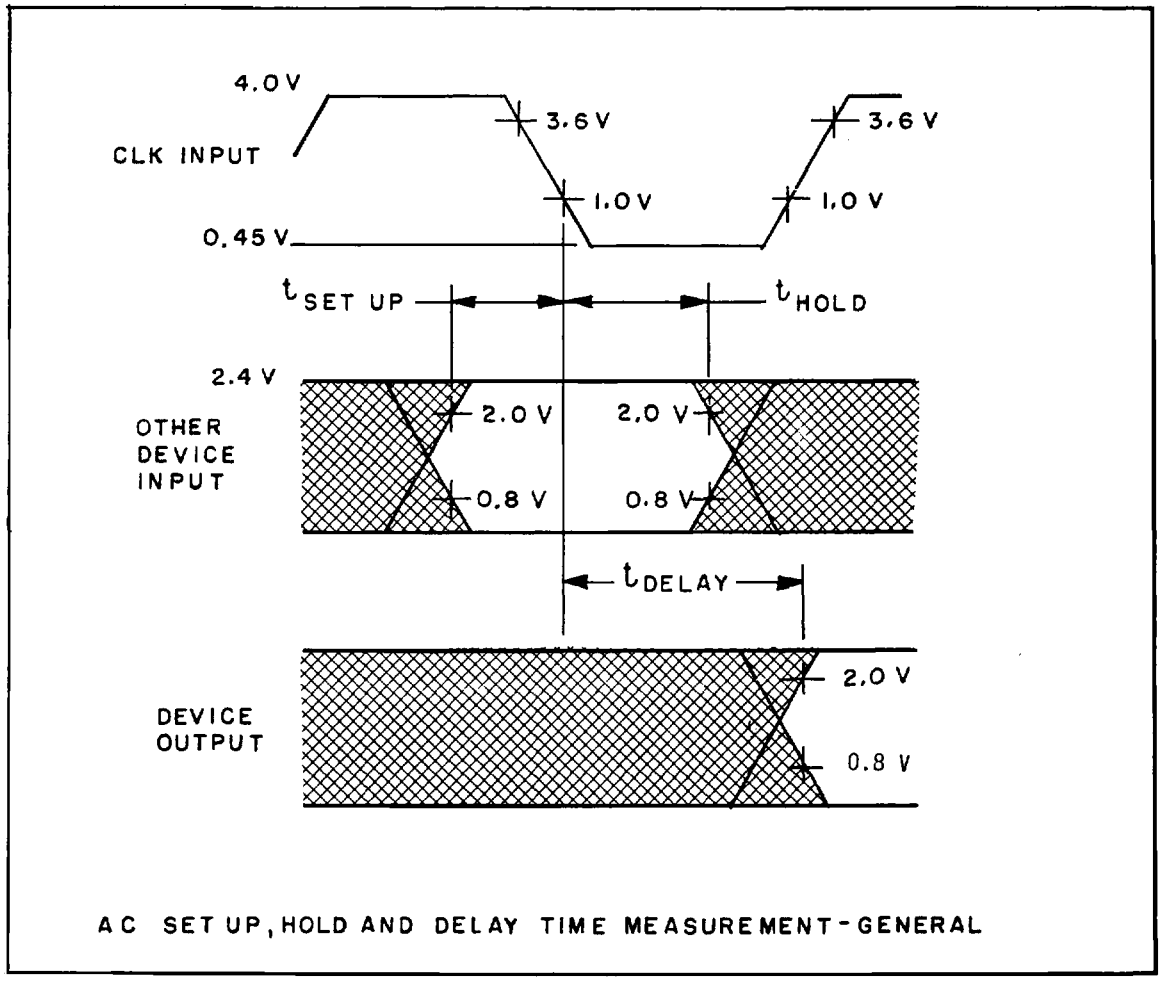


FIGURE 4. Waveforms - Continued.

Major cycle timing

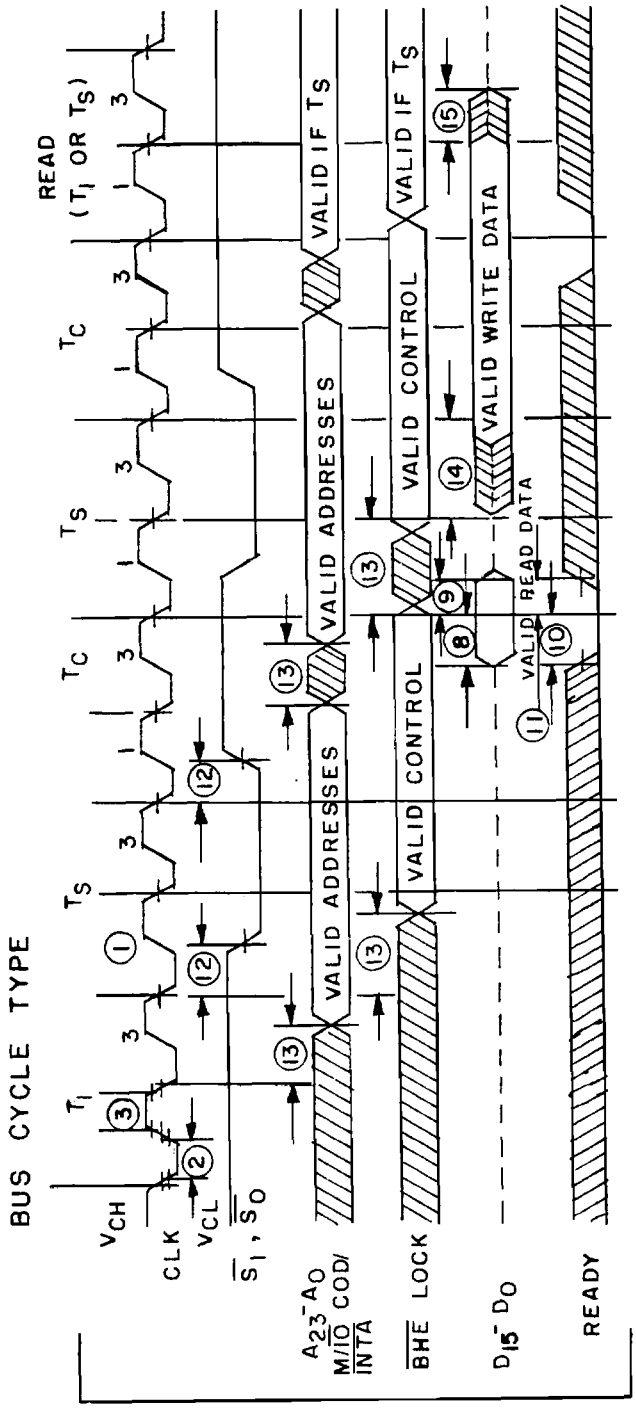
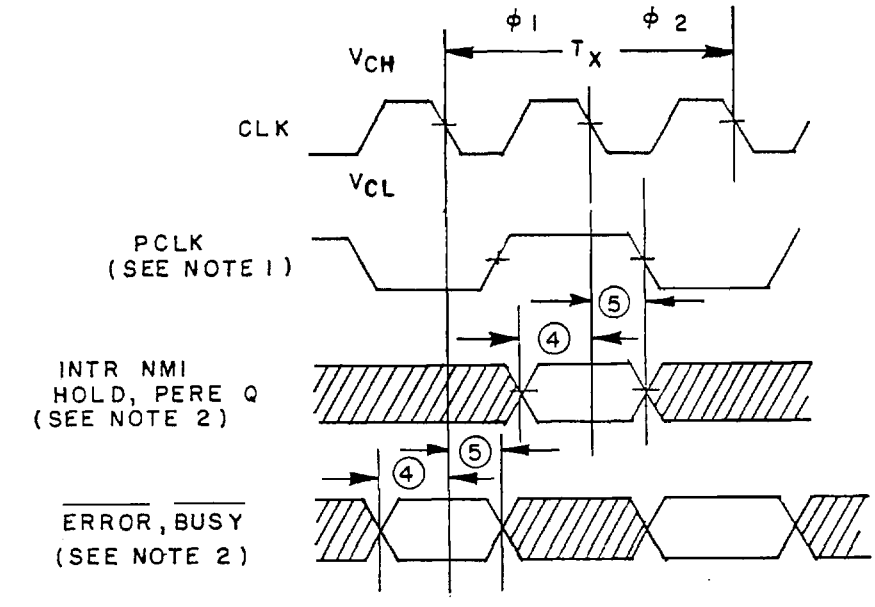


FIGURE 4. Waveforms - Continued.

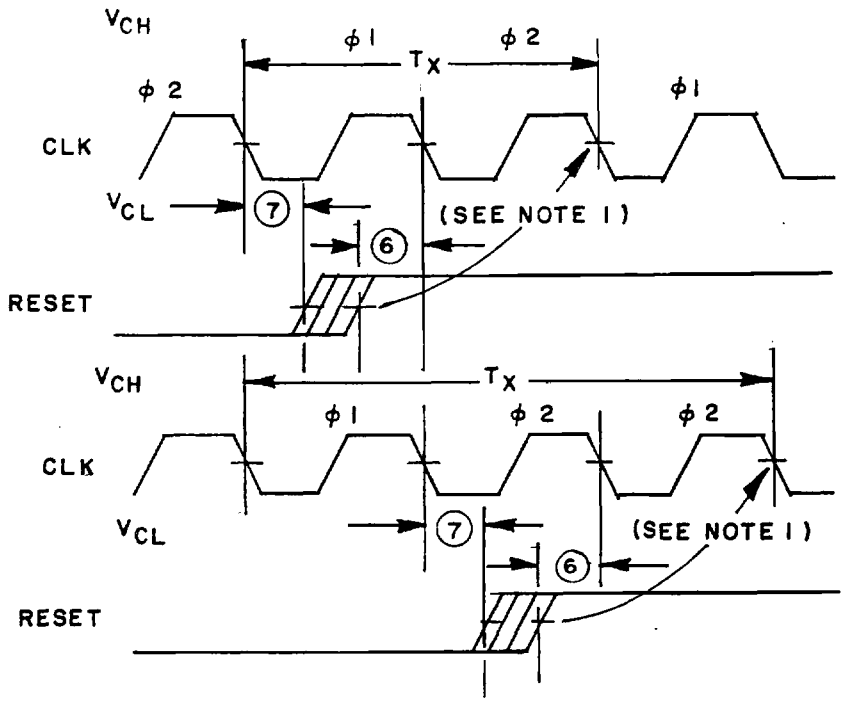
Asynchronous input signal timing



NOTES:
1. PCLK indicates which processor cycle phase will occur on the next CLK. PCLK may not indicate the correct phase until the first bus cycle is performed.
2. These inputs are asynchronous. The setup and hold times shown assure recognition for testing purposes.

FIGURE 4. Waveforms - Continued.

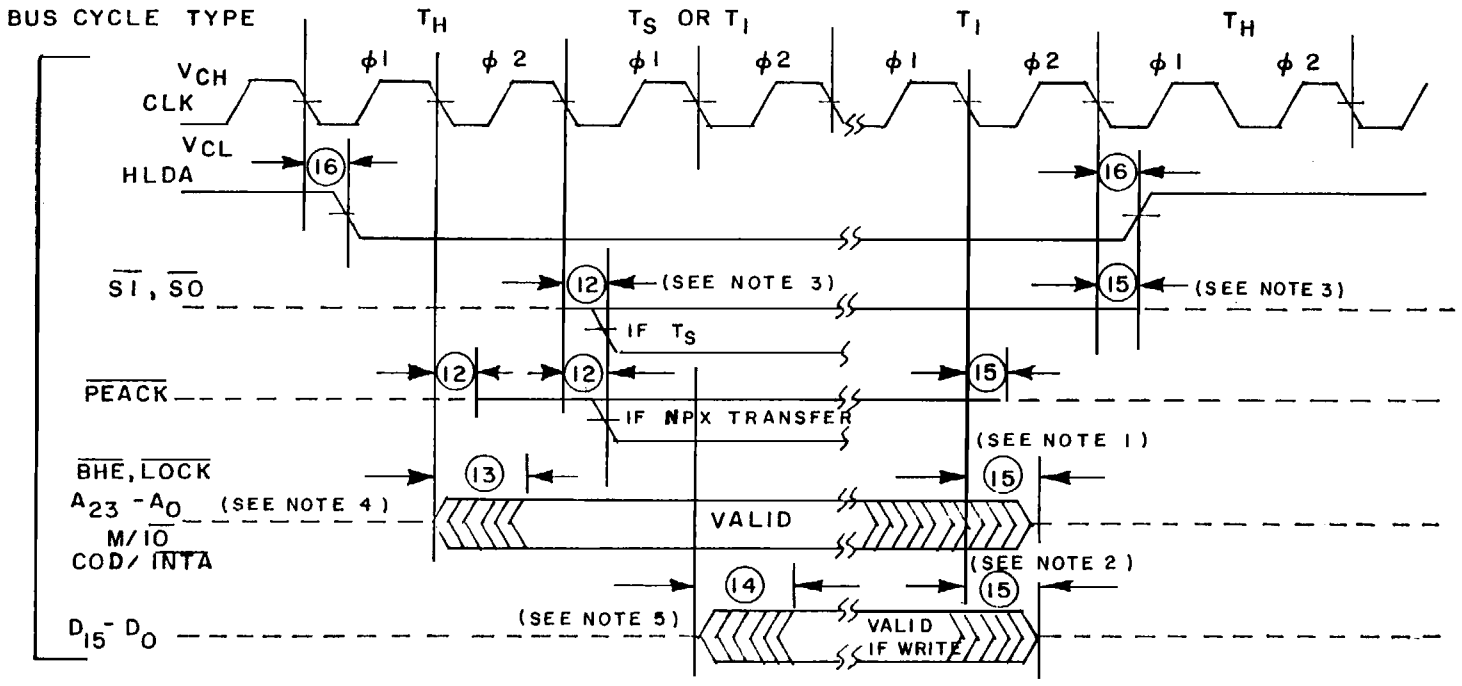
Reset input timing and subsequent processor cycle phase



NOTE: When RESET meets the setup time shown, the next CLK will start or repeat $\phi 2$ of a processor cycle.

FIGURE 4. Waveforms - Continued.

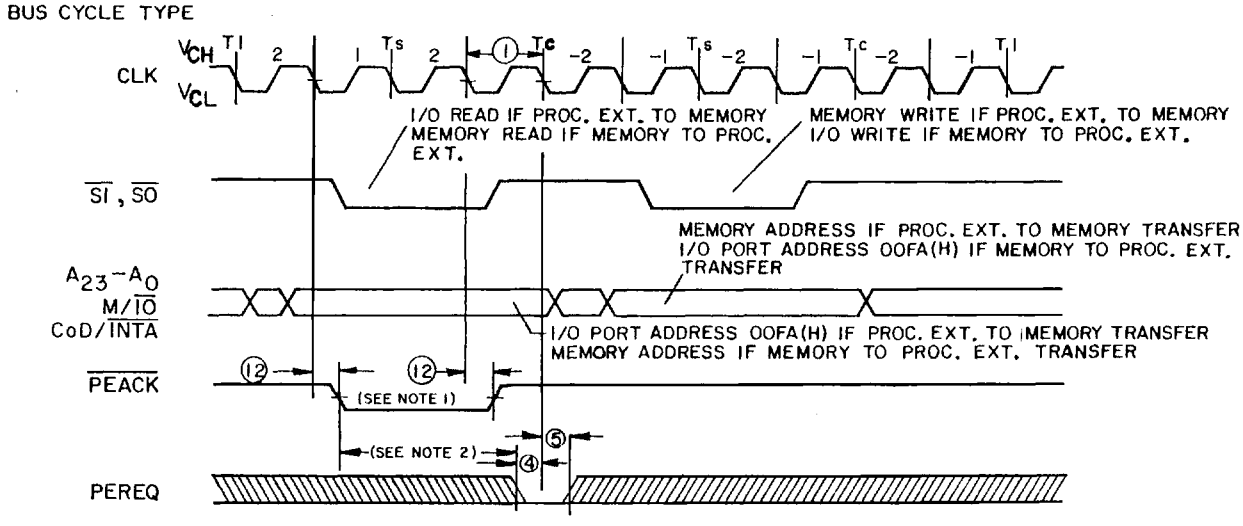
Exiting and entering hold



NOTES:
1. These signals may not be driven by the device during the time shown. The worst case in terms of latest float time is shown.
2. The data bus will be driven as shown if the last cycle before T_1 in the diagram was a write T_C.
3. The M80286 floats its status pins during T_H. External 20 kΩ resistors keep these signals high.
4. $\overline{BHE}$ and $\overline{LOCK}$ are driven at this time but will not become valid until T_S.
5. The data bus will remain in three-state OFF if a read cycle is performed.

FIGURE 4. Waveforms - Continued.

PEREQ/$\overline{\text{PEACK}}$ timing for one transfer only.



Assuming word-aligned memory operand, if odd aligned, 80286 transfers to/from memory byte-at-a-time with two memory cycles.

NOTES:
1. $\overline{\text{PEACK}}$ always goes active during the first bus operation of a processor extension data operand and transfer sequence. The first bus operation will be either a memory read at operand address or I/O read at port address 00FA(H).
2. To prevent a second processor extension data operand transfer, the worst case maximum time (shown above) is: $3 \times ① - 11_{MAX} - ④_{MIN}$. The actual configuration dependent, maximum time is: $3 \times ① - 11_{MAX} - ④_{MIN} + A \times 2 \times ①$. A is the number of extra T_C states added to either the first or second bus operation of the processor extension data operand transfer sequence.

FIGURE 4. Waveforms - Continued.

Pin state during reset

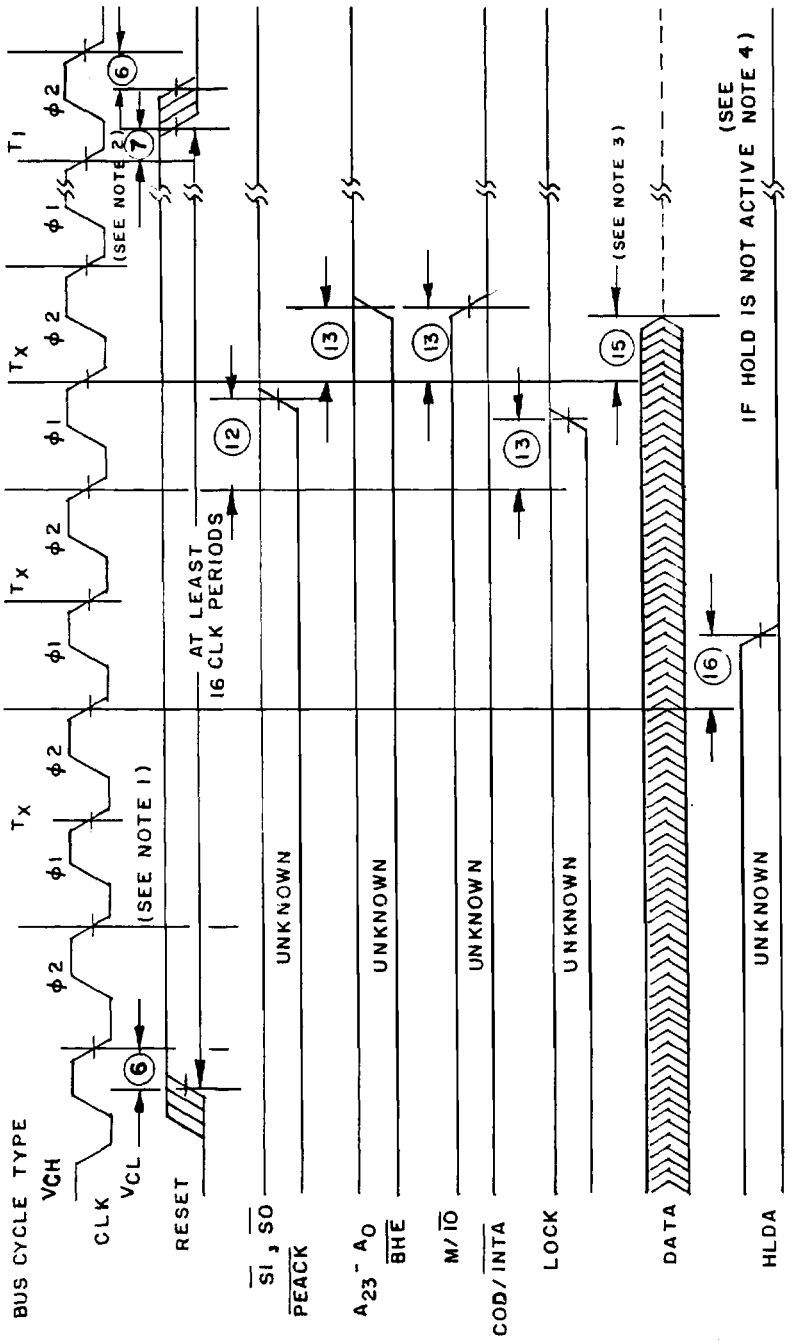


FIGURE 4. Waveforms - Continued.

Pin state during reset

NOTES:
1. Setup time for RESET↑ may be violated with the consideration that ϕ1 of the processor clock may begin one system CLK period later.
2. Setup and hold times for RESET↓ must be met for proper operation, but RESET↓ may occur during ϕ1 or ϕ2.
3. The data bus is only guaranteed to be in three-state OFF at the time shown.
4. HOLD is acknowledged during RESET, causing HLDA to go active and the appropriate pins to float. If HOLD remains active while RESET goes inactive, the device remains in HOLD state and will not perform any bus accesses until HOLD is de-activated.

FIGURE 4. Waveforms - Continued.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

d. Subgroups 7 and 8 shall consist of verifying the instruction set.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 8(125°C), 10
Additional electrical subgroups for group C periodic inspections	---

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/535--B--.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Symbols, definitions, and functional descriptions. The symbols, definitions, and functional description for these devices shall be as follows:

Symbol	Type	Name and function
PEREQ $\overline{\text{PEACK}}$	I O	Processor extension operand request and acknowledge extend the memory management and protection capabilities of the device to processor extensions. The PEREQ input requests the device to perform a data operand transfer for a processor extension. The $\overline{\text{PEACK}}$ output signals the processor extension when the requested operand is being transferred. PEREQ is active HIGH and floats to 3-state OFF during bus hold acknowledge. $\overline{\text{PEACK}}$ may be asynchronous to the system clock. $\overline{\text{PEACK}}$ is active LOW.
$\overline{\text{BUSY}}$ $\overline{\text{ERROR}}$	I I	Processor extension busy and error indicate the operating condition of a processor extension to the device. An active $\overline{\text{BUSY}}$ input stops device program execution on WAIT and some ESC instructions until $\overline{\text{BUSY}}$ becomes inactive (HIGH). The device may be interrupted while waiting for $\overline{\text{BUSY}}$ to become inactive. An active $\overline{\text{ERROR}}$ input causes the device to perform a processor extension interrupt when executing WAIT or some ESC instructions. These inputs are active LOW and may be asynchronous to the system clock.
RESET	I	System reset clears the internal logic of the device and is active HIGH. The device may be reinitialized at any time with a LOW to HIGH transition on RESET which remains active for more than 16 system clock cycles. During RESET active, the output pins of the device enter the state shown below:

Device pin state during reset

Pin value	Pin names
1 (HIGH)	$\overline{S_0}$,$\overline{S_1}$, $\overline{\text{PEACK}}$, A23-A0, $\overline{\text{BHE}}$, $\overline{\text{LOCK}}$
0 (LOW)	M/$\overline{\text{IO}}$, COD/$\overline{\text{INTA}}$, HLDA
3-state OFF	D_{15} - D_0

Operation of the device begins after a HIGH to LOW transition on RESET. The HIGH to LOW transition of RESET must be synchronous to the system clock. Approximately 50 system clock cycles are required by the device for internal initializations before the first bus cycle to fetch code from the power-on execution address is performed.
A LOW to HIGH transition of RESET synchronous to the system clock will end a processor cycle at the second HIGH to LOW transition of the system clock. The LOW to HIGH transition of RESET may be asynchronous to the system clock; however, in this case it cannot be predetermined which phase of the processor clock will occur during the next system clock period. Synchronous LOW to HIGH transitions of RESET are required only for systems where the processor clock must be phase synchronous to another clock.

Symbol	Type	Name and function
V_{SS}	I	System ground: 0 volts.
V_{CC}	I	System power: +5 volt power supply
CAP	I	Substrate filter capacitor: a 0.047 µF ±20% 12 V capacitor must be connected between this pin and ground. This capacitor filters the output of the internal substrate bias generator. A maximum dc leakage current of 1 µA is allowed through the capacitor. For correct operation of the device, the substrate bias generator must charge this capacitor to its operating voltage. The capacitor chargeup time is 5 milliseconds (maximum) after V_{CC} and CLK reach their specified ac and dc parameters. RESET may be applied to prevent spurious activity by the CPU during this time. After this time, the device processor clock can be synchronized to another clock by pulsing RESET LOW synchronous to the system clock.
$\overline{S_1}$, $\overline{S_0}$	O	Bus cycle status indicates initiation of a bus cycle and, along with M/IO and COD/INTA, defines the type of bus cycle. The bus is in a T_s state whenever one or both are LOW, $\overline{S_1}$ and $\overline{S_0}$ are active LOW and float to 3-state OFF during bus hold acknowledge.

Bus cycle status definition

COD/$\overline{INTA}$	M/$\overline{IO}$	$\overline{S_1}$	$\overline{S_0}$	Bus cycle initiated
0(LOW)	0	0	0	Interrupt acknowledge
0	0	0	1	Reserved
0	0	1	0	Reserved
0	0	1	1	None; not a status cycle
0	1	0	0	IF A1 = 1 then halt; else shutdown
0	1	0	1	Memory data read
0	1	1	0	Memory data write
0	1	1	1	None; not a status cycle
1 (HIGH)	0	0	0	Reserved
1	0	0	1	I/O read
1	0	1	0	I/O write
1	0	1	1	None; not a status cycle
1	1	0	0	Reserved
1	1	0	1	Memory instruction read
1	1	1	0	Reserved
1	1	1	1	None; not a status cycle

Symbol	Type	Name and function
M/$\overline{IO}$	O	Memory I/O select distinguishes memory access from I/O access. If HIGH during T_s, a memory cycle or a halt/shutdown cycle is in progress. If LOW, an I/O cycle or an interrupt acknowledge cycle is in progress. M/$\overline{IO}$ floats to 3-state OFF during bus hold acknowledge.

Symbol	Type	Name and function
COD/$\overline{\text{INTA}}$	O	Code/interrupt acknowledge distinguishes instruction fetch cycles from memory data read cycles. Also distinguishes interrupt acknowledge cycles from I/O cycles. COD/$\overline{\text{INTA}}$ floats to 3-state OFF during bus hold acknowledge. Its timing is the same as M/$\overline{\text{IO}}$.
$\overline{\text{LOCK}}$	O	Bus lock indicates that other system bus masters are not to gain control of the system bus following the current bus cycle. The $\overline{\text{LOCK}}$ signal may be activated explicitly by the "LOCK" instruction prefix or automatically by device hardware during memory XCHG instructions, interrupt acknowledge, or descriptor table access. $\overline{\text{LOCK}}$ is active LOW and floats to 3-state OFF during bus hold acknowledge.
$\overline{\text{READY}}$	I	Bus ready terminates a bus cycle. Bus cycles are extended without limit until terminated by $\overline{\text{READY}}$ LOW, $\overline{\text{READY}}$ is an active LOW synchronous input requiring setup and hold times relative to the system clock be met for correct operation. $\overline{\text{READY}}$ is ignored during bus hold acknowledge.
HOLD HLDA	I O	Bus hold request and hold acknowledge control ownership of the device local bus. The HOLD input allows another local bus master to request control of the local bus. When control is granted, the device will float its bus drives to 3-state OFF and then activate HLDA, thus entering the bus hold acknowledge condition. The local bus will remain granted to the requesting master until HOLD becomes inactive which results in the device deactivating HLDA and regaining control of the local bus. This terminates the bus hold acknowledge condition. HOLD may be synchronous to the system clock. These signals are active HIGH.
INTR	I	Interrupt request requests the device to suspend its current program execution and service a pending external request. Interrupt requests are masked whenever the interrupt enable bit in the flag word is cleared. When the device responds to an interrupt request, it performs two interrupt acknowledge bus cycles to read an 8-bit interrupt vector that identifies the source of the interrupt. To assure program interruption, INTR must remain active until the first interrupt acknowledge cycle is completed. INTR is sampled at the beginning of each processor cycle and must be active HIGH at least two processor cycles before the current instruction ends in order to interrupt before the next instruction. INTR is level sensitive, active HIGH, and may be asynchronous to the system clock.

Symbol	Type	Name and function
NMI	I	Non-maskable interrupt request interrupts the device with an internally supplied vector value of 2. No interrupt acknowledge cycles are performed. The interrupt enable bit in the device flag word does not affect this input. The NMI input is active HIGH, may be asynchronous to the system clock, and is edge triggered after internal synchronization. For proper recognition, the input must have been previously LOW for at least four system clock cycles and remain HIGH for at least four system clock cycles.
CLK	I	System clock provides the fundamental timing for multi-tasking systems. It is divided by two inside the device to generate the processor clock. The internal divided-by-two circuitry can be synchronized to an external clock generator by a LOW to HIGH transition on the RESET input.
D_{15} - D_0	I/O	Data bus inputs data during memory, I/O, and interrupt acknowledge read cycles; outputs data during memory and I/O write cycles. The data bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.
A_{23} - A_0	O	Address bus outputs physical memory and I/O port addresses. A0 is LOW when data is to be transferred on pins D_7-D_0. A_{23}-A_{16} are LOW during I/O transfers. The address bus is active HIGH and floats to 3-state OFF during bus hold acknowledge.
$\overline{BHE}$	O	Bus high enable indicates transfer or data on the upper byte of the data bus, D_{15}-D_8. Eight-bit oriented devices assigned to the upper byte of the data bus would normally use $\overline{BHE}$ to condition chip select functions. $\overline{BHE}$ is active LOW and floats to 3-state OFF during bus hold acknowledge.

$\overline{BHE}$ and A0 encodings

$\overline{BHE}$ value	A0 value	Function
0	0	Word transfer
0	1	Byte transfer on upper half of data bus (D_{15}-D_8)
1	0	Byte transfer on lower half of data bus (D_7-D_0)
1	1	Reserved

6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8514801XX	34649	MG80286-8/B	M38510/53502BXX
5962-8514801YX	34649	MQ80286-8/B	M38510/53502BYX
5962-8514802XX	34649	MG80286-6/B	M38510/53501BXX
5962-8514802YX	34649	MQ80286-6/B	M38510/53501BYX
5962-8514803XX	34649	MG80286-10/B	---
5962-8514803YX	34649	MQ80286-10/B	---

1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 5000 W. Williams Field Road Chandler, AZ 85224

☆ U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-073/60057