CY7C166

16 K × 4 Static RAM

Features

- High speed
  - 15 ns
- Output enable ($\overline{OE}$) feature
- CMOS for optimum speed/power
- Low active power
  - 633 mW
- Low standby power
  - 110 mW
- TTL-compatible inputs and outputs
- Automatic power-down when deselected

Functional Description

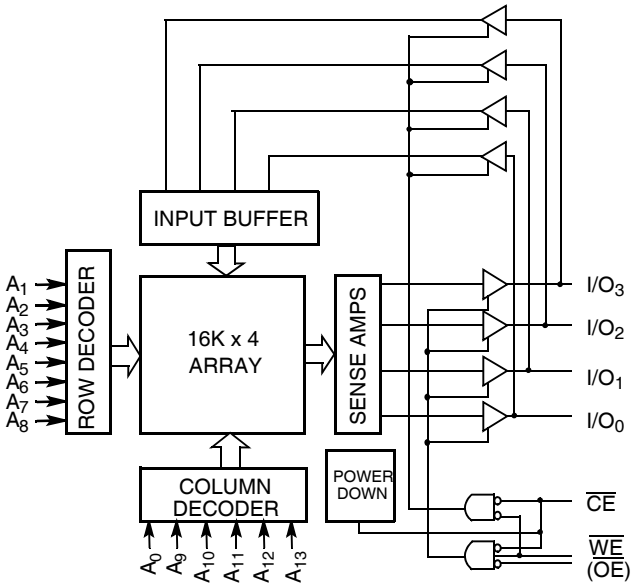
The CY7C166 is a high-performance CMOS static RAMs organized as 16,384 by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$) and tri-state drivers. The CY7C166 has an active LOW Output Enable ($\overline{OE}$) feature. This device has an automatic power-down feature, reducing the power consumption by 65% when deselected.

Writing to the device is accomplished when the Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs are both LOW (and the Output Enable ($\overline{OE}$) is LOW). Data on the four input/output pins (I/O_0 through I/O_3) is written into the memory location specified on the address pins (A_0 through A_{13}).

Reading the device is accomplished by taking Chip Enable ($\overline{CE}$) LOW (and $\overline{OE}$ LOW), while Write Enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data I/O pins.

The I/O pins stay in a high-impedance state when Chip Enable ($\overline{CE}$) is HIGH (or Output Enable ($\overline{OE}$) is HIGH). A die coat is used to insure alpha immunity.

Logic Block Diagram



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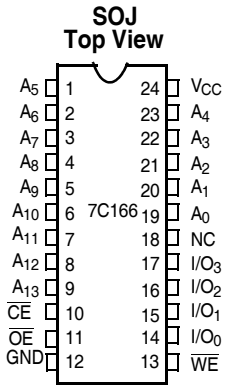
Pin Configuration



Selection Guide

Description	CY7C166-15
Maximum Access Time (ns)	15
Maximum Operating Current (mA)	115
Maximum CMOS Standby Current (mA)	20

Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.5 V to +7.0 V

DC voltage applied to outputs in high Z State[1] .....–0.5 V to +7.0 V

DC input voltage[1].....–0.5 V to +7.0 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, method 3015)

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	5 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	–15		Unit
			Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = Min, I_{OH} = –4.0 mA	2.4	–	V
V_{OL}	Output LOW voltage	V_{CC} = Min, I_{OL} = 8.0 mA	–	0.4	V
V_{IH}	Input HIGH voltage		2.2	V_{CC}	V
V_{IL}	Input LOW voltage[1]		–0.5	0.8	V
I_{IX}	Input leakage current	GND ≤ V_I ≤ V_{CC}	–5	+5	µA
I_{OZ}	Output leakage current	GND ≤ V_O ≤ V_{CC}, output disabled	–5	+5	µA
I_{CC}	V_{CC} operating supply current	V_{CC} = Max, I_{OUT} = 0 mA	–	115	mA
I_{SB1}	Automatic $\overline{CE}$ power-down current[2]	Max V_{CC}, $\overline{CE}$ ≥ V_{IH}, Min Duty Cycle = 100%	–	40	mA
I_{SB2}	Automatic $\overline{CE}$ power-down current[2]	Max V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3 V, V_{IN} ≥ V_{CC} – 0.3 V or V_{IN} ≤ 0.3 V	–	20	mA

Capacitance[3]

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = 5.0 V	10	pF
C_{OUT}	Output capacitance		10	pF

Notes
1. Minimum voltage is equal to –3.0 V for pulse durations less than 30 ns.
2. A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed values given.
3. Tested initially and after any design or process changes that may affect these parameters.

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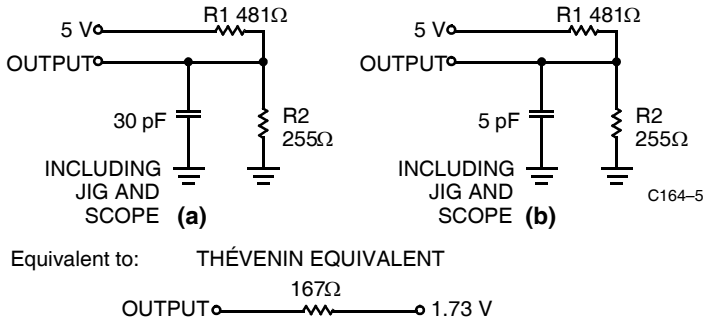
AC Test Loads and Waveforms



Switching Characteristics

Over the Operating Range[4]

Parameter	Description	CY7C166-15		Unit
		Min	Max	
READ CYCLE				
t_{RC}	Read cycle time	15	–	ns
t_{AA}	Address to data valid	–	15	ns
t_{OHA}	Output hold from address change	3	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	15	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	10	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z	3	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z	–	8	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z[5]	3	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z[5, 6]	–	8	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	15	ns
WRITE CYCLE[7]				
t_{WC}	Write cycle time	15	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	12	–	ns
t_{AW}	Address set-up to write end	12	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address set-up to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	12	–	ns
t_{SD}	Data set-up to write end	10	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z[5]	5	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z[5, 6]	–	7	ns

Notes

4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} for any given device. These parameters are guaranteed by design and not 100% tested.
6. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) in AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
7. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

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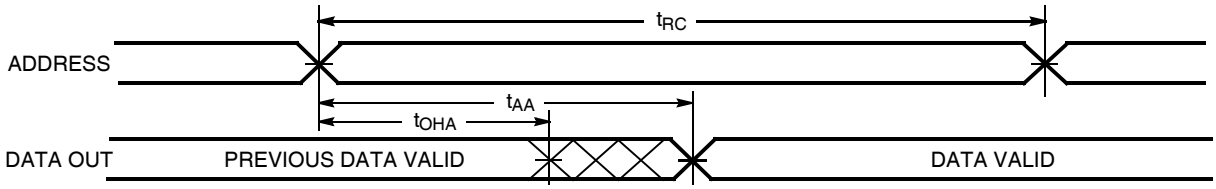
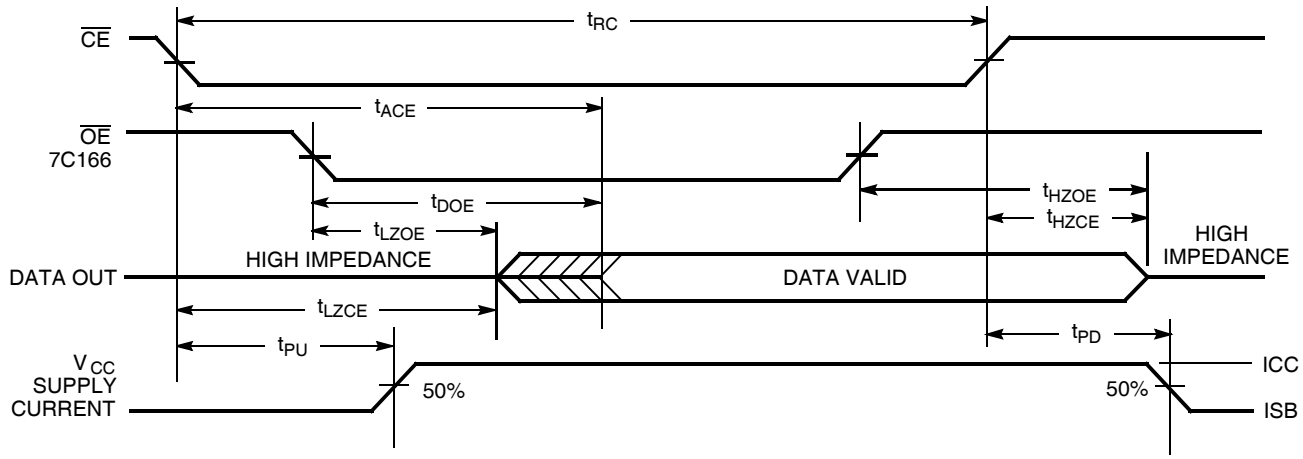
Switching Waveforms

Read Cycle No. 1[8, 9]



Read Cycle No. 2[8, 10]



Notes
8. $\overline{WE}$ is HIGH for read cycle.
9. Device is continuously selected, $\overline{CE} = V_{IL}$. (CY7C166: $\overline{OE} = V_{IL}$ also).
10. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

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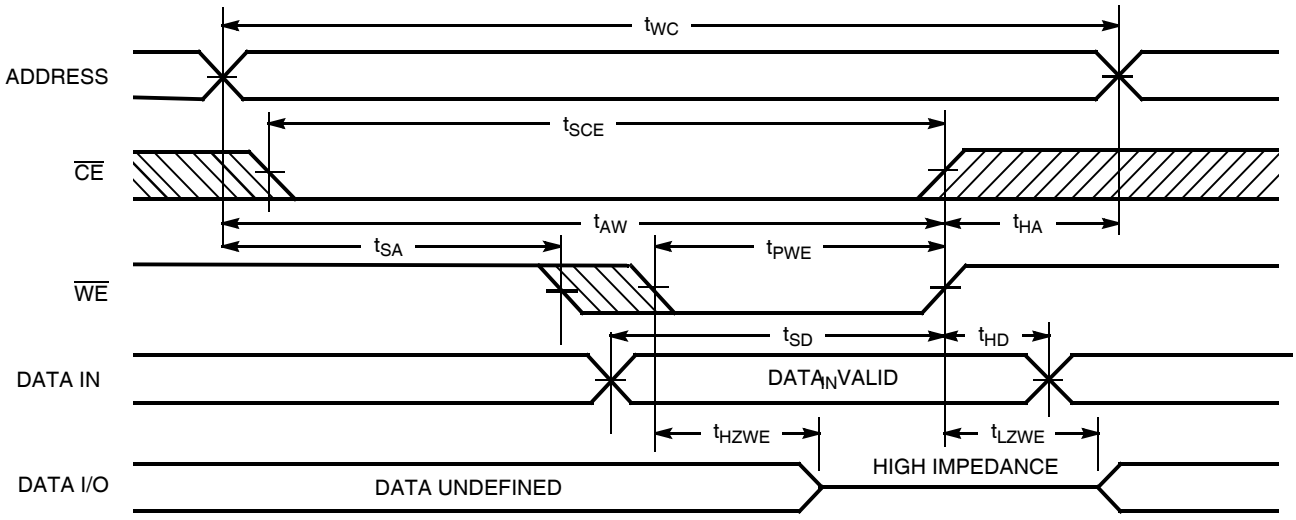
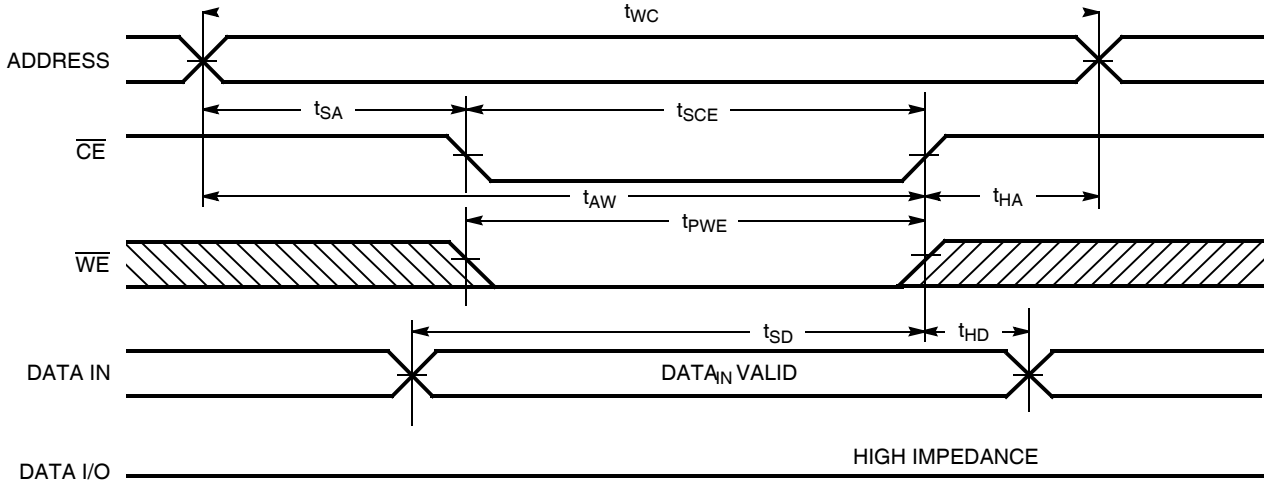
Switching Waveforms (continued)

Write Cycle No. 1($\overline{WE}$ Controlled)[11,12]



Write Cycle No. 2($\overline{CE}$ Controlled)[11,12,13]

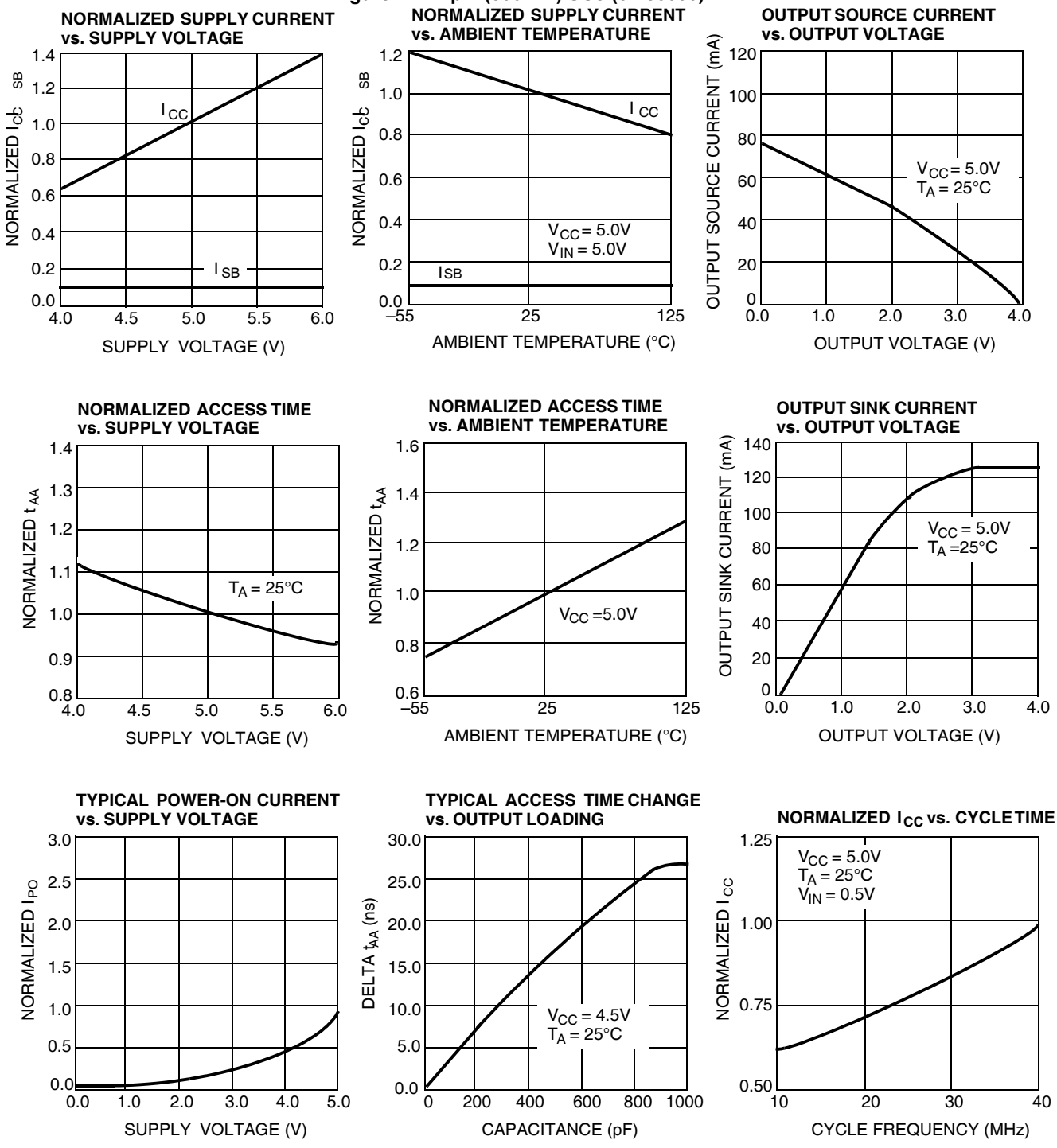


Notes

11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. CY7C166 only: Data I/O will be high-impedance if $\overline{OE} = V_{IH}$.
13. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.

Typical DC and AC Characteristics

Figure 1. 24-pin (300-mil) SOJ (51-85030)



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CY7C166 Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Input/Output	Mode	Power
H	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	L	Data out	Read	Active (I_{CC})
L	L	H	Data in	Write	Active (I_{CC})
L	H	H	High Z	Select/output disabled	Active (I_{CC})

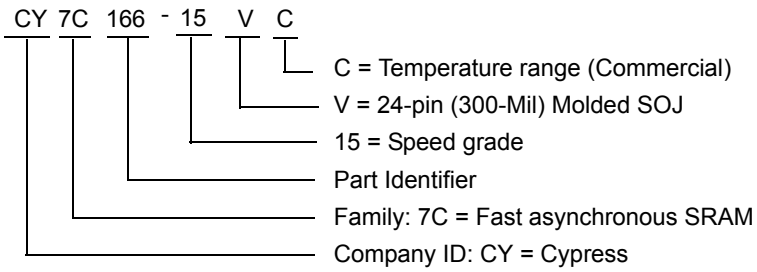
Address Designators

Address Name	Address Function	CY7C166 Pin Number
A5	X3	1
A6	X4	2
A7	X5	3
A8	X6	4
A9	X7	5
A10	Y5	6
A11	Y4	7
A12	Y0	8
A13	Y1	9
A0	Y2	19
A1	Y3	20
A2	X0	21
A3	X1	22
A4	X2	23

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C166-15VC	51-85030	24-pin (300-Mil) Molded SOJ	Commercial

Ordering Code Definitions



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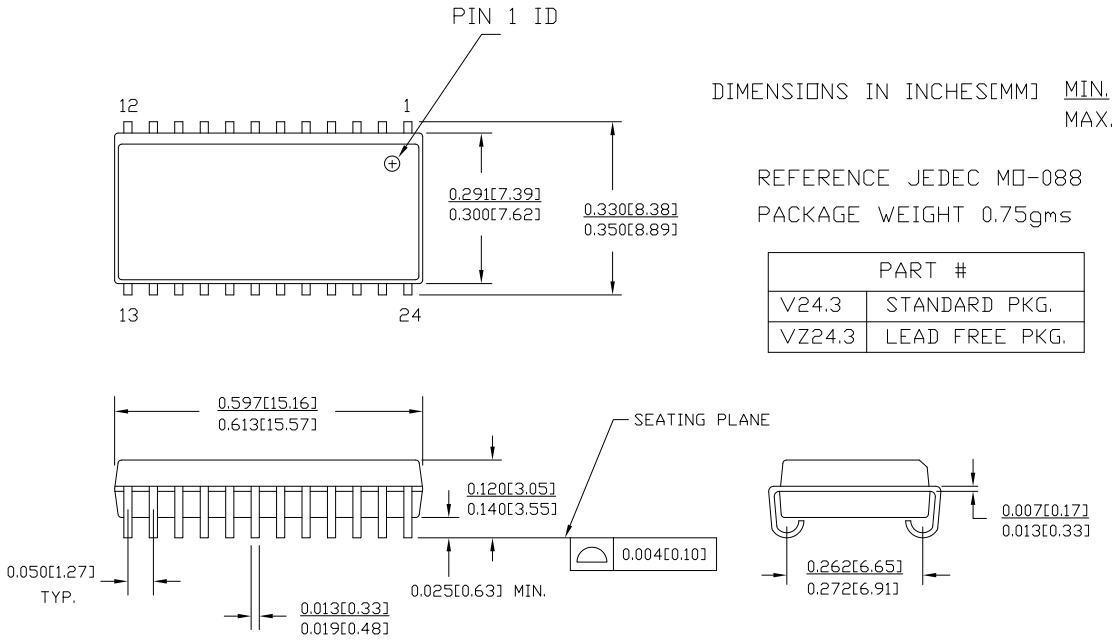
Package Diagram

Figure 1. 24-pin (300-mil) SOJ, 51-85030



51-85030 *C

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
CE	chip enable
DIP	dual inline package
I/O	input/output
OE	output enable
SRAM	static random access memory
SOJ	small outline J-lead
TTL	transistor-transistor logic
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
ns	nano seconds
V	Volts
µA	micro Amperes
mA	milli Amperes
mV	milli Volts
mW	milli Watts
pF	pico Farad
°C	degree Celcius
W	Watts
%	percent

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Document History Page

Document Title: CY7C166 16 K × 4 Static RAM Document Number: 38-05025				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	106811	09/10/01	SZV	Change from Spec number: 38-00032 to 38-05025
*A	486744	See ECN	NXR	Removed 20 ns and 35 ns speed bin from Product offering Removed 24-pin (300-Mil) Molded DIP package Changed the description of I_{IX} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I_{OS} parameter from DC Electrical Characteristics table Updated the ordering information table
*B	2894113	03/17/2010	VKN	Added Table of Contents Removed CY7C164 part from the data sheet Removed 25 ns speed bin Removed 22-pin (300-Mil) PDIP package Updated ordering Information Table Updated Package Diagram (Figure 1) Added Sales, Solutions, and Legal Information
*C	3096933	11/29/2010	PRAS	Added Ordering Code Definitions. Added Acronyms and Units of Measure. Minor edits.

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