Rochester Electronics®

PART NUMBER

74178PC-ROCV

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

• ISO-9001

• AS9120 certification

• Qualified Manufacturers List (QML) MIL-PRF-38535
    • Class Q Military
    • Class V Space Level

Qualified Suppliers List of Distributors (QSLD)
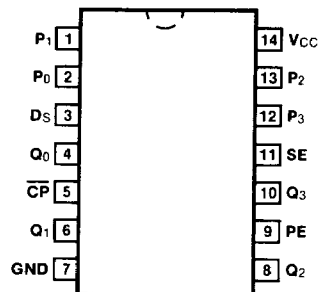   • Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

54/74178 *010680*

4-BIT SHIFT REGISTER

Connection Diagram Pinout A:

| Pin	Signal		Pin	Signal
1	P_1		14	V_{CC}
2	P_0		13	P_2
3	D_S		12	P_3
4	Q_0		11	SE
5	$\overline{CP}$		10	Q_3
6	Q_1		9	PE
7	GND		8	Q_2

DESCRIPTION — The '178 features synchronous parallel or serial entry and parallel outputs. The flip-flops are fully edge-triggered, with state changes initiated by a HIGH-to-LOW transition of the clock. Parallel Enable and Serial Enable inputs are used to select Load, Shift and Hold modes of operation. The '178 is the 14-pin version of the '179. For detail specifications, please refer to the '179 data sheet.

LOGIC SYMBOL

V_{CC} = Pin 14
GND = Pin 7

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74178PC		9A
Ceramic DIP (D)	A	74178DC	54178DM	6A
Flatpak (F)	A	74178FC	54178FM	3I
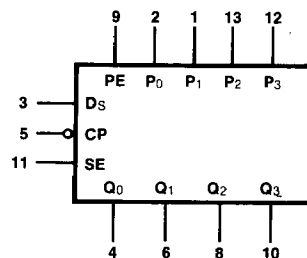
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

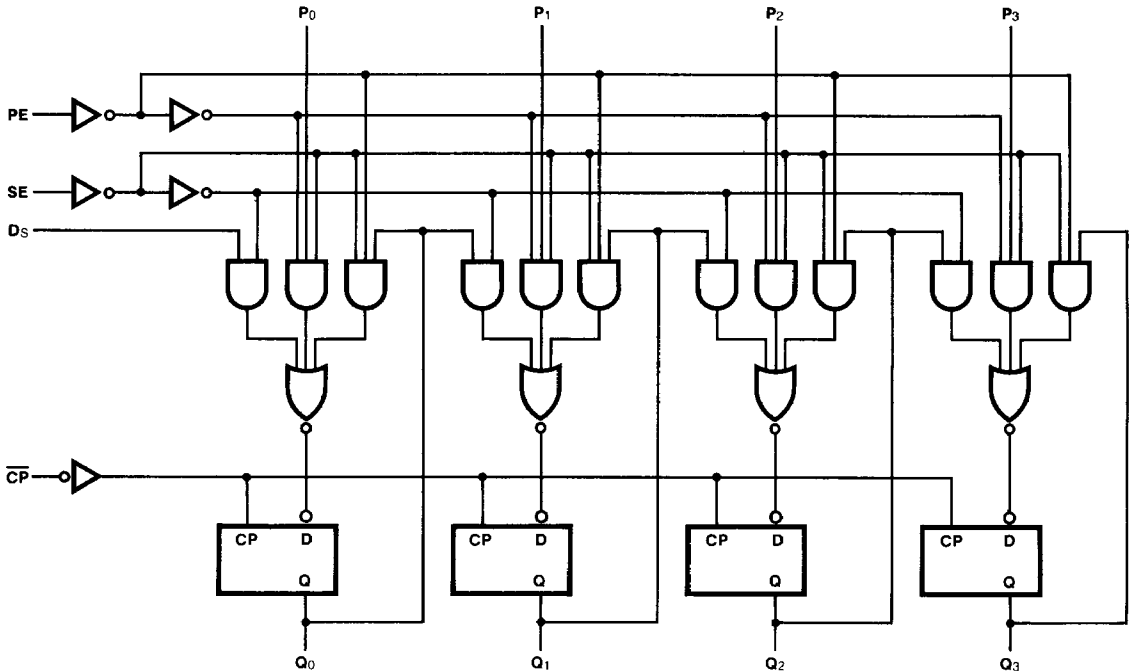| PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
PE	Parallel Enable Input	1.0/1.0
$P_0 - P_3$	Parallel Data Inputs	1.0/1.0
D_S	Serial Data Input	1.0/1.0
$\overline{SE}$	Shift Enable Input	1.0/1.0
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	1.0/1.0
$Q_0 - Q_3$	Flip-flop Outputs	20/10

FUNCTIONAL DESCRIPTION — The '178 contains four D-type edge-triggered flip-flops and sufficient interstage logic to perform parallel load, shift right or hold operations. All state changes are initiated by a HIGH-to-LOW transition of the clock. A HIGH signal on the Shift Enable (SE) input prevents parallel loading and permits a right shift each time the clock makes a negative transition. When the SE input is LOW, the signal applied to the Parallel Enable (PE) input determines whether the circuit is in a parallel load or a hold mode, as shown in the Mode Select Table. The SE, PE, D_S and P_n inputs can change when the clock is in either state, provided only that the recommended setup and hold times are observed.

MODE SELECT TABLE

SE	PE	$\overline{CP}$	RESPONSE
H	X	⌐L	Right Shift. $D_S \rightarrow Q_0$; $Q_0 \rightarrow Q_1$, etc.
L	H	⌐L	Parallel load $P_n \rightarrow Q_n$.
L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial.

LOGIC DIAGRAM