NEC

MOS INTEGRATED CIRCUIT

μPD8670

7400 PIXELS CCD LINEAR IMAGE SENSOR

The μPD8670 is a high sensitive and high-speed CCD (Charge Coupled Device) linear image sensor which changes optical images to electrical signal.

The μPD8670 is a 2-output type CCD sensor with 2 rows of high-speed charge transfer register, which transfers the photo signal electrons of 7400 pixels separately in odd and even pixels. And it has reset feed-through level clamp circuits and voltage amplifiers. Therefore, it is suitable for 600 dpi/A3 high-speed digital copiers, multi-function products and so on.

FEATURES

- Valid photocell : 7400 pixels
- Photocell pitch : 4.7 μm
- Photocell size : $4.7 \times 4.7\ \mu m^2$
- Resolution : 24 dot/mm (600 dpi) A3 (297×420 mm) size (shorter side)
- Data rate : 44 MHz MAX. (22 MHz/1 output)
- Output type : 2 outputs in-phase operation, and out of phase also supported
- High sensitivity : 17.0 V/lx•s TYP. (Light source: Daylight color fluorescent lamp)
- Peak response wavelength : 550 nm (green)
- Low image lag : 1 % MAX.
- Drive clock level : CMOS output under +5 V operation
- Power supply : +12 V
- On-chip circuits : Reset feed-through level clamp circuits
  Voltage amplifiers

ORDERING INFORMATION

Part Number	Package
μPD8670CY	CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

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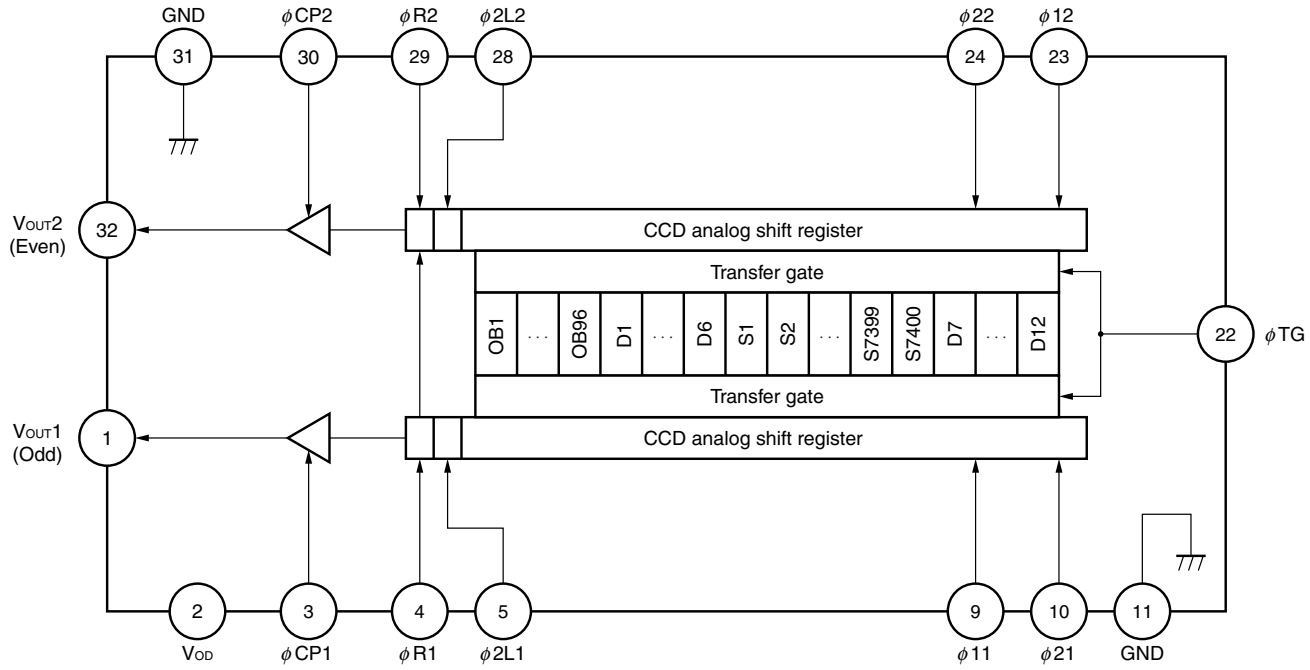
DIFFERENCE BETWEEN μPD8670CY and μPD3747D

Part	Item	μPD8670CY	μPD3747D	Referential Page
Features	Output type	2 outputs out of phase or in phase	2 outputs in phase only	1
	Sensitivity (Daylight color fluorescent lamp)	TYP. 17 V/lx•s	TYP. 19 V/lx•s	
Ordering information	Package	32-pin plastic DIP	22-pin ceramic DIP (CERDIP)	
Pin configuration	Input clock	φCP1, φCP2 separated, φR1, φR2 separated, φ2L1, φ2L2 separated (Output: in/out of phase)	φCP common, φR common, φ2L common (Output: in phase)	4
Block diagram				3
Application circuit example				21
	Equivalent circuit Tr.	2SA1206, 2SC1842	2SA1005, 2SC945	
Absolute maximum ratings	Operating ambient temperature	0 to +60°C	–25 to +55°C	5
	Storage temperature	–40 to +70°C	–40 to +100°C	
Recommended operating condition	Each clock amplitude	Addition of specifications (from 4.5 V to 5.8 V)	–	
Electrical characteristics	ADS, DSNU, DR1, DR2	Change of specifications	–	6
	R_F	TYP. 17 V/lx•s	TYP. 19 V/lx•s	
	RFTN	Addition of PRFTN, RFTN1, RFTN2	Only RFTN	
	t_d	TYP. 13 ns Addition of min. max.	TYP. 14 ns	
	σbit, σline, σshot	Addition of condition (t6)	–	
Input pin capacitance	Capacitance	Change of specification Addition of note	–	7
Timing chart	Operation	Addition of out-of-phase timing chart	–	8, 9
	t6	MIN. 5 ns	MIN. 0 ns	12, 14
	t10	MIN. 0 ns	MIN. t3	
	t13, t16, t17	MAX. 10000 ns	–	14
Close point	–	Cange of specifications	–	15
Definitions	V_{OS}, RFTN	Additional item	–	19
Recommended soldering condition	Partial heating method	350°C or blow, 3 seconds or less	300°C or blow, 3 seconds or less	24
Package drawing	Package	32-pin plastic DIP	22-pin ceramic DIP (CERDIP)	23
	Cap	Plastic cap 0.7t	Glass cap 0.7t	
	From CCD to bottom of package	2.45 ± 0.3 mm	2.38 ± 0.3 mm	
	From CCD to top of cap	(2.0) mm	(1.95) mm	

Remark T_A = +25°C, V_{OD} = 12 V

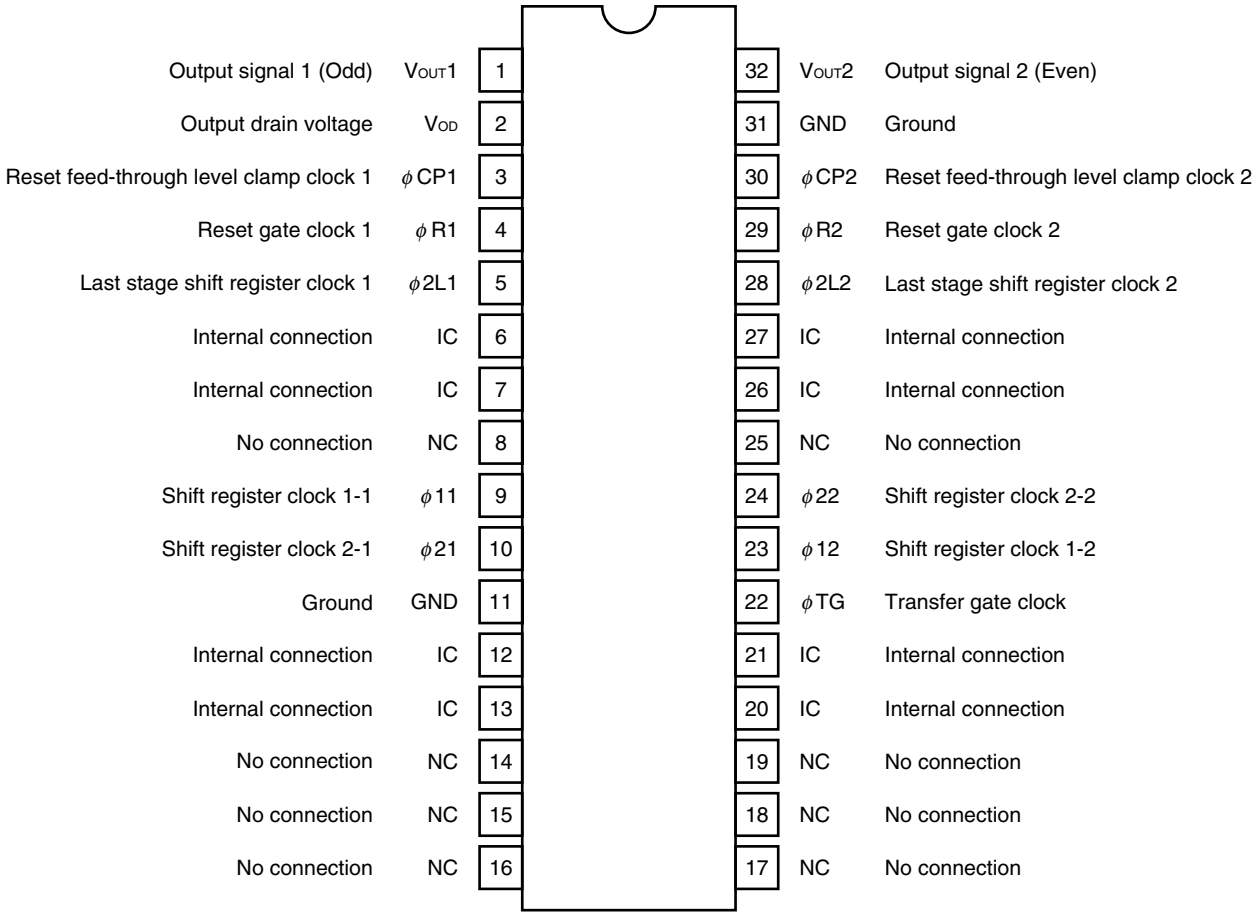
BLOCK DIAGRAM



PIN CONFIGURATION (Top View)

CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

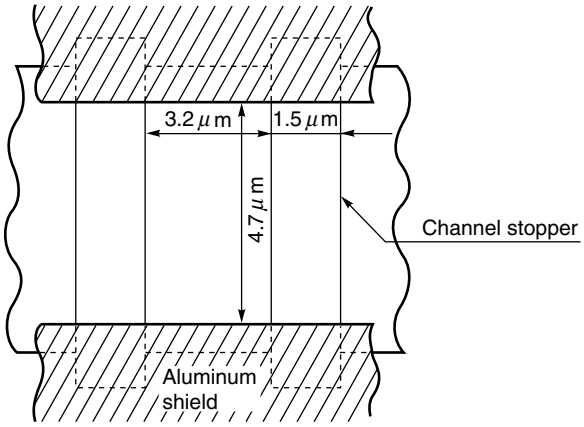
• μPD8670CY



Cautions 1. Leave pins 6, 7, 12, 13, 20, 21, 26 and 27 (IC) unconnected.

2. Connect the No connection pins (NC) to GND.

PHOTOCELL STRUCTURE DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T_A = +25°C)

Parameter	Symbol	Ratings	Unit
Output drain voltage	V_{OD}	−0.3 to +14.0	V
Shift register clock voltage	$V_{\phi 1}$, $V_{\phi 2}$	−0.3 to +8.0	V
Last stage shift register clock voltage	$V_{\phi 2L}$	−0.3 to +8.0	V
Reset gate clock voltage	$V_{\phi R}$	−0.3 to +8.0	V
Transfer gate clock voltage	$V_{\phi TG}$	−0.3 to +8.0	V
Reset feed-through level clamp clock voltage	$V_{\phi CP}$	−0.3 to +8.0	V
Operating ambient temperature[Note]	T_A	0 to +60	°C
Storage temperature	T_{stg}	−40 to +70	°C

Note Use at the condition without dew condensation.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

RECOMMENDED OPERATING CONDITIONS (T_A = +25°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output drain voltage	V_{OD}		11.4	12.0	12.6	V
Shift register clock high level	$V_{\phi 1H}$, $V_{\phi 2H}$		4.5	5.0	5.5	V
Shift register clock low level	$V_{\phi 1L}$, $V_{\phi 2L}$		−0.3	0	+0.5	V
Last stage shift register clock high level	$V_{\phi 2LH}$		4.5	5.0	5.5	V
Last stage shift register clock low level	$V_{\phi 2LL}$		−0.3	0	+0.5	V
Reset gate clock high level	$V_{\phi RH}$		4.5	5.0	5.5	V
Reset gate clock low level	$V_{\phi RL}$		−0.3	0	+0.5	V
Reset feed-through level clamp clock high level	$V_{\phi CPH}$		4.5	5.0	5.5	V
Reset feed-through level clamp clock low level	$V_{\phi CPL}$		−0.3	0	+0.5	V
Transfer gate clock high level	$V_{\phi TGH}$		4.5	5.0	5.5	V
Transfer gate clock low level	$V_{\phi TGL}$		−0.3	0	+0.5	V
Shift register clock amplitude	$V_{\phi 1\_pp}$,	f < 10 MHz/ch	4.0	5.0	5.8	V
	$V_{\phi 2\_pp}$	f ≥ 10 MHz/ch	4.5	5.0	5.8	V
Last stage shift register clock amplitude	$V_{\phi 2L\_pp}$		4.5	5.0	5.8	V
Reset gate clock amplitude	$V_{\phi R\_pp}$		4.5	5.0	5.8	V
Reset feed-through level clamp clock amplitude	$V_{\phi CP\_pp}$		4.5	5.0	5.8	V
Transfer gate clock amplitude	$V_{\phi TG\_pp}$		4.5	5.0	5.8	V
Data rate	$2f_{\phi R}$		1	2	44	MHz

ELECTRICAL CHARACTERISTICS

(T_A = +25°C, V_{OD} = 12 V, $f_{\phi R}$ = 1 MHz, data rate = 2 MHz, storage time = 10 ms, input signal clock = 5 V_{p-p}, light source : 3200 K halogen lamp + C-500S (infrared cut filter, t = 1 mm) + HA-50 (heat absorbing filter, t = 3 mm))

Parameter	Symbol	Test Conditions		MIN.	TYP.	MAX.	Unit
Saturation voltage	V_{sat}			1.5	2.0	–	V
Saturation exposure	SE	Daylight color fluorescent lamp		–	0.10	–	lx•s
Photo response non-uniformity	PRNU	V_{OUT} = 500 mV		–	5.0	10.0	%
Average dark signal	ADS	Light shielding		–	1.0	6.0	mV
Dark signal non-uniformity	DSNU	Light shielding		–	16.0	28.0	mV
Power consumption	P_W			–	350	600	mW
Output impedance	Z_O			–	0.2	0.3	kΩ
Response	R_F	Daylight color fluorescent lamp		13.6	17.0	20.4	V/lx•s
Image lag	IL	V_{OUT} = 500 mV		–	0.5	1.0	%
Offset level Note 1	V_{OS}			3.7	4.7	5.7	V
Output fall delay time Note 2	t_d	V_{OUT} = 500 mV		11.0	13.0	14.0	ns
Total transfer efficiency	TTE	V_{OUT} = 1 V, data rate = 44 MHz		94	98	–	%
Register imbalance	RI	V_{OUT} = 500 mV		0	1.0	4.0	%
Response peak				–	550	–	nm
Dynamic range	DR1	V_{sat}/DSNU		–	125	–	times
	DR2	V_{sat}/σbit, t6 ≥ 20 ns		–	1000	–	times
Reset feed-through noise Note 1	PRFTN	Light shielding, t4 = 5 ns		–	1.0	–	V
	RFTN1			–0.3	+0.3	+0.9	V
	RFTN2			–0.3	+0.3	+0.9	V
Random noise	σbit	Light shielding, bit clamp mode	t6 = 5 ns	–	2.6	–	mV
			t6 ≥ 20 ns	–	2.0	–	mV
	σline	Light shielding, line clamp mode	t6 ≥ 5 ns	–	8.0	–	mV
Shot noise	σshot	V_{OUT} = 500 mV, bit clamp mode	t6 ≥ 5 ns	–	10.0	–	mV

Notes 1. Refer to 13 and 14 of **DEFINITION OF CHARACTERISTIC ITEMS**.

2. When the fall time of ϕ2L (t2') is the TYP. value (refer to **TIMING CHART 5, 6**). Note that V_{OUT}1 and V_{OUT}2 are the outputs of the two steps of emitter-follower shown in **APPLICATION CIRCUIT EXAMPLE**.

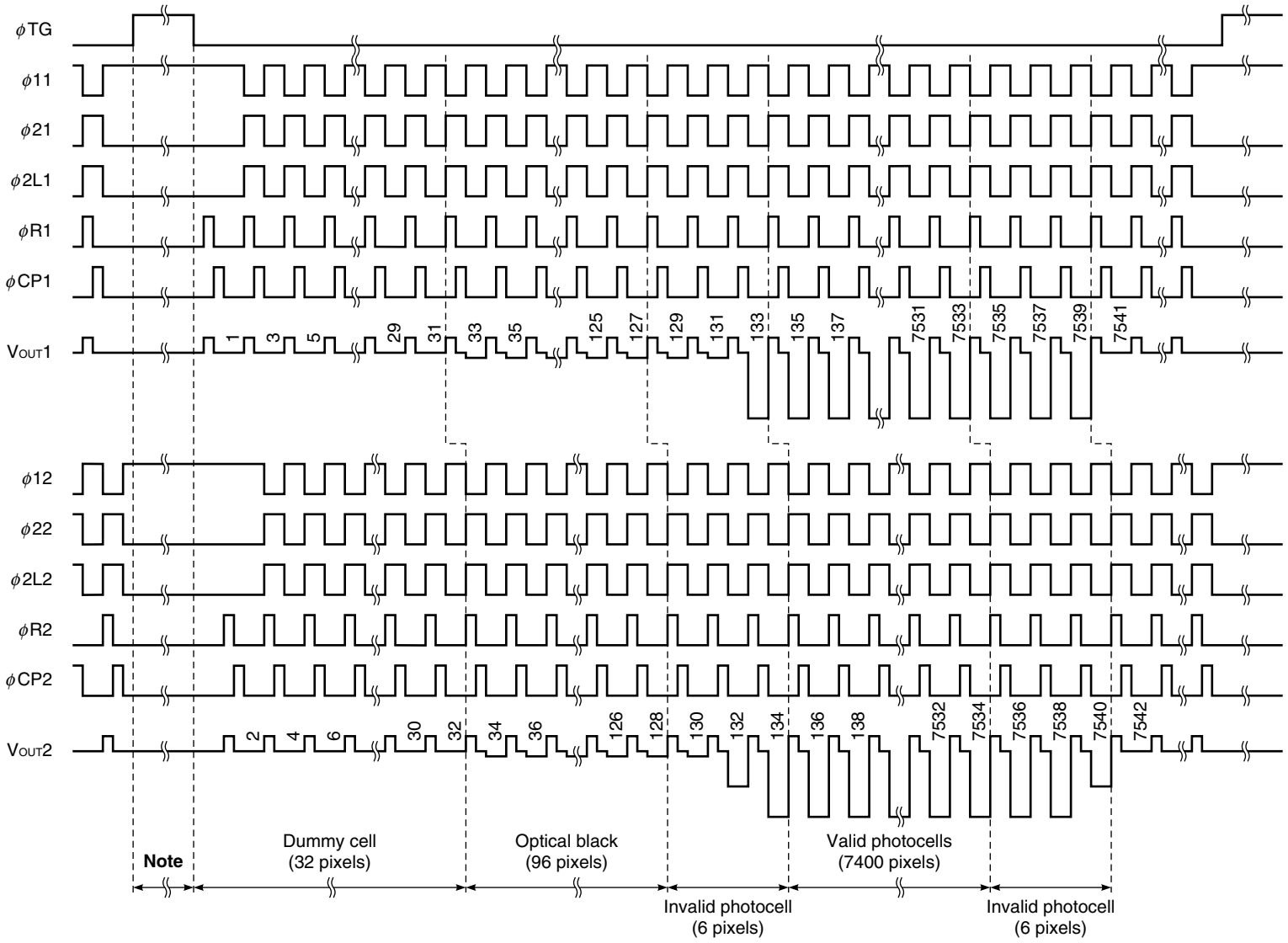
INPUT PIN CAPACITANCE (T_A = +25°C, V_{OD} = 12 V)

Parameter	Symbol	Pin name	Pin No.	MIN.	TYP.	MAX.	Unit
Shift register clock pin capacitance 1	$C_{\phi 1}$ Note	ϕ11	9	225	250	275	pF
		ϕ12	23	200	220	240	pF
Shift register clock pin capacitance 2	$C_{\phi 2}$ Note	ϕ21	10	200	220	240	pF
		ϕ22	24	225	250	275	pF
Last stage shift register clock pin capacitance	$C_{\phi L}$	ϕ2L1	5	4	5	6	pF
		ϕ2L2	28	4	5	6	pF
Reset gate clock pin capacitance	$C_{\phi R}$	ϕR1	4	4	5	6	pF
		ϕR2	29	4	5	6	pF
Reset feed-through level clamp clock pin capacitance	$C_{\phi CP}$	ϕCP1	3	7	8	9	pF
		ϕCP2	30	7	8	9	pF
Transfer gate clock pin capacitance	$C_{\phi TG}$	ϕTG	22	240	270	300	pF

Note $C_{\phi 1}$, $C_{\phi 2}$ are equivalent capacitance with driving device, including the co-capacitance between ϕ1 and ϕ2.

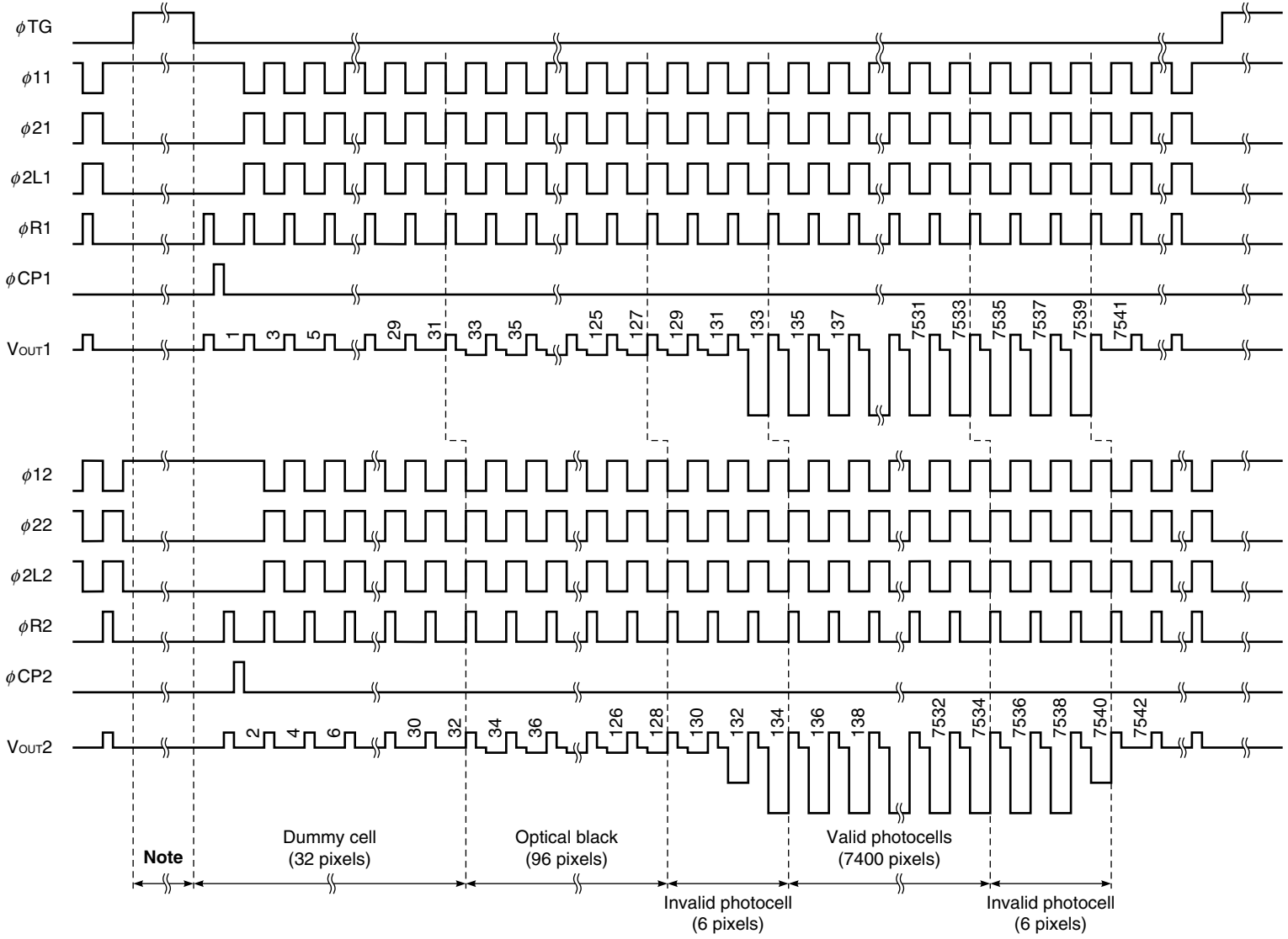
Remark Pins 9 and 23 (ϕ11 and ϕ12), Pins 10 and 24 (ϕ21 and ϕ22) aren't each connected inside of the device.

TIMING CHART 1 (Bit clamp mode, Out of phase operation)



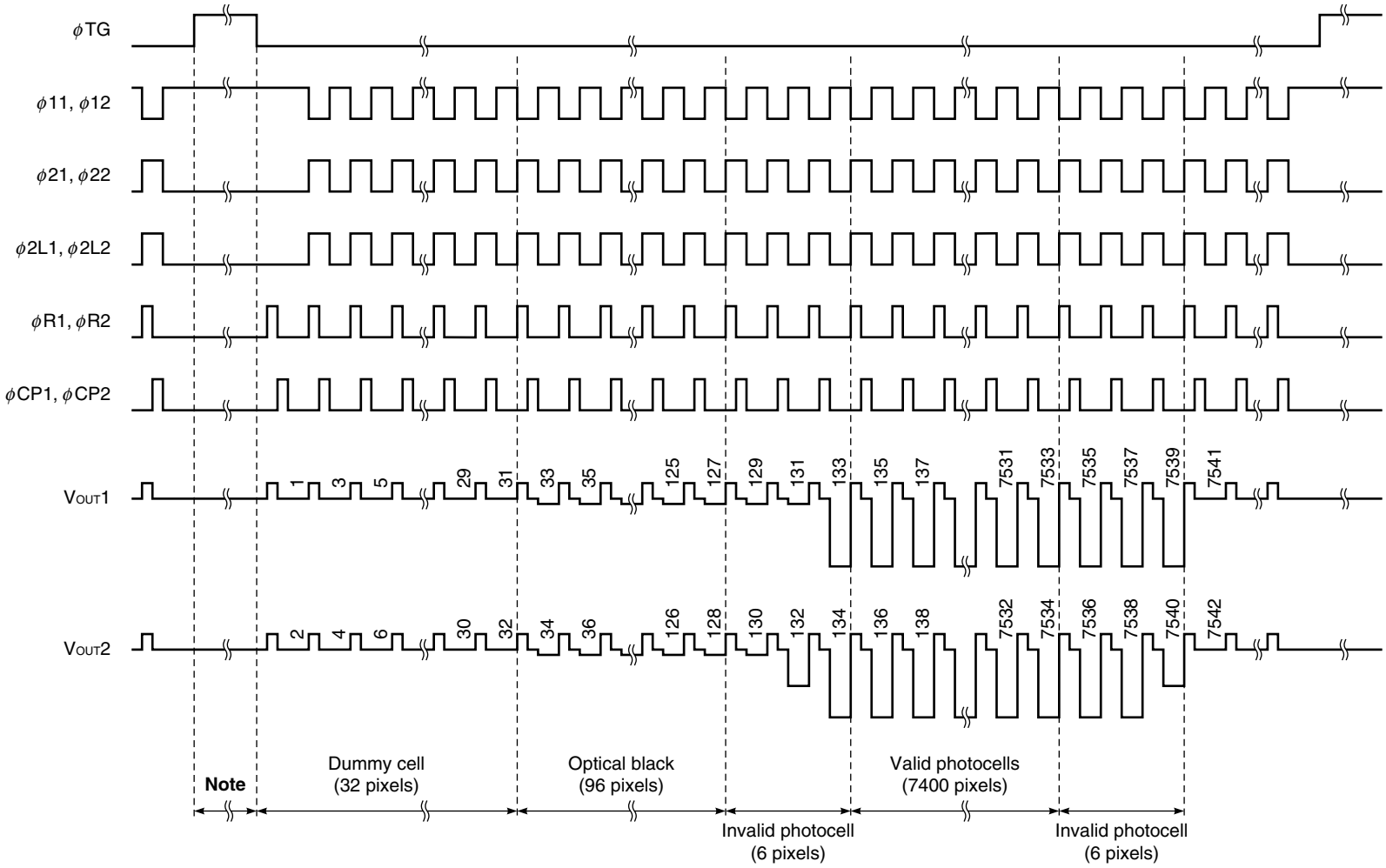
Note Set the φR1, φR2, φCP1 and φCP2 to low level during this period.

TIMING CHART 2 (Line clamp mode, Out of phase operation)



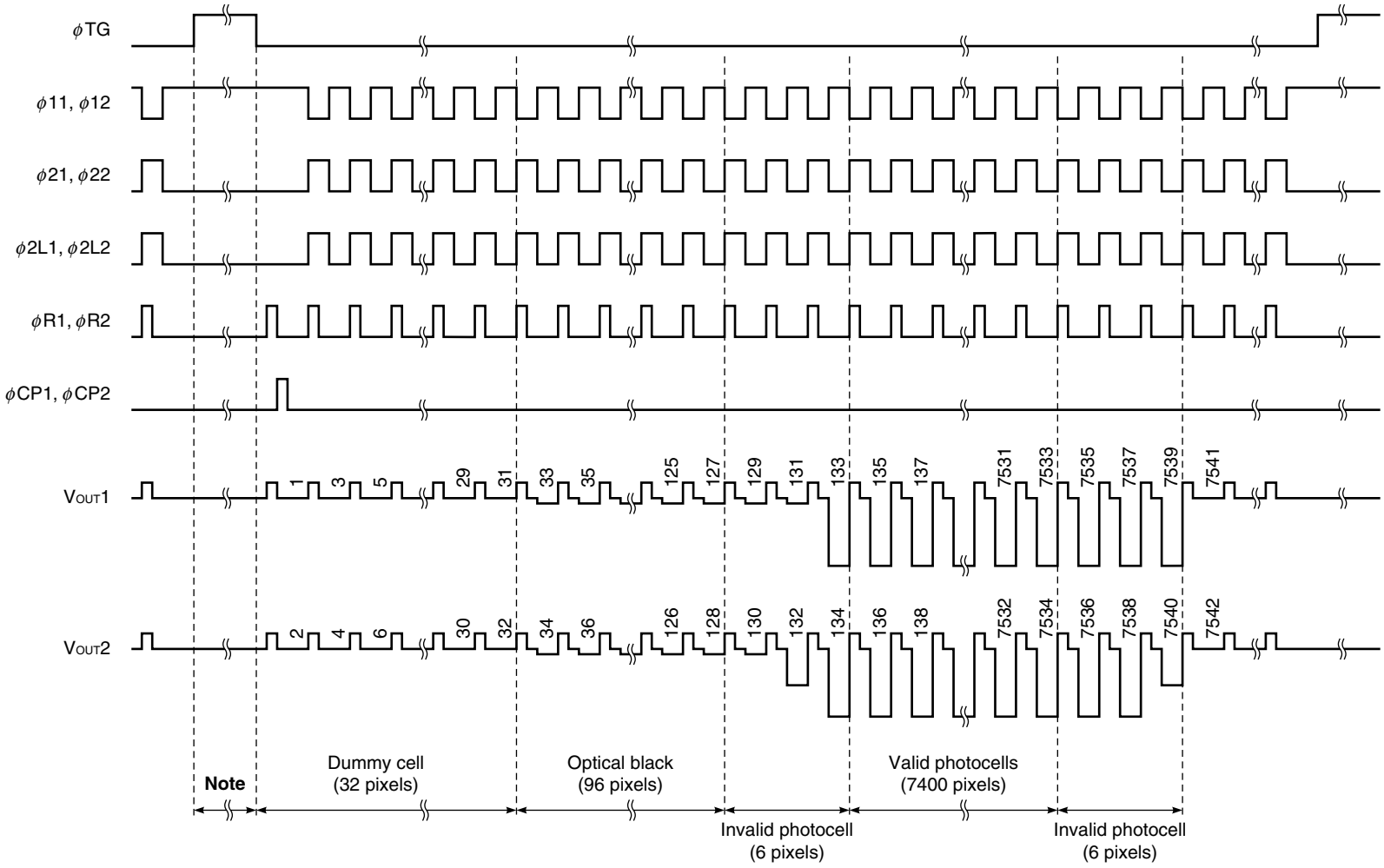
Note Set the φR1, φR2, φCP1 and φCP2 to low level during this period.

TIMING CHART 3 (Bit clamp mode, In phase operation)



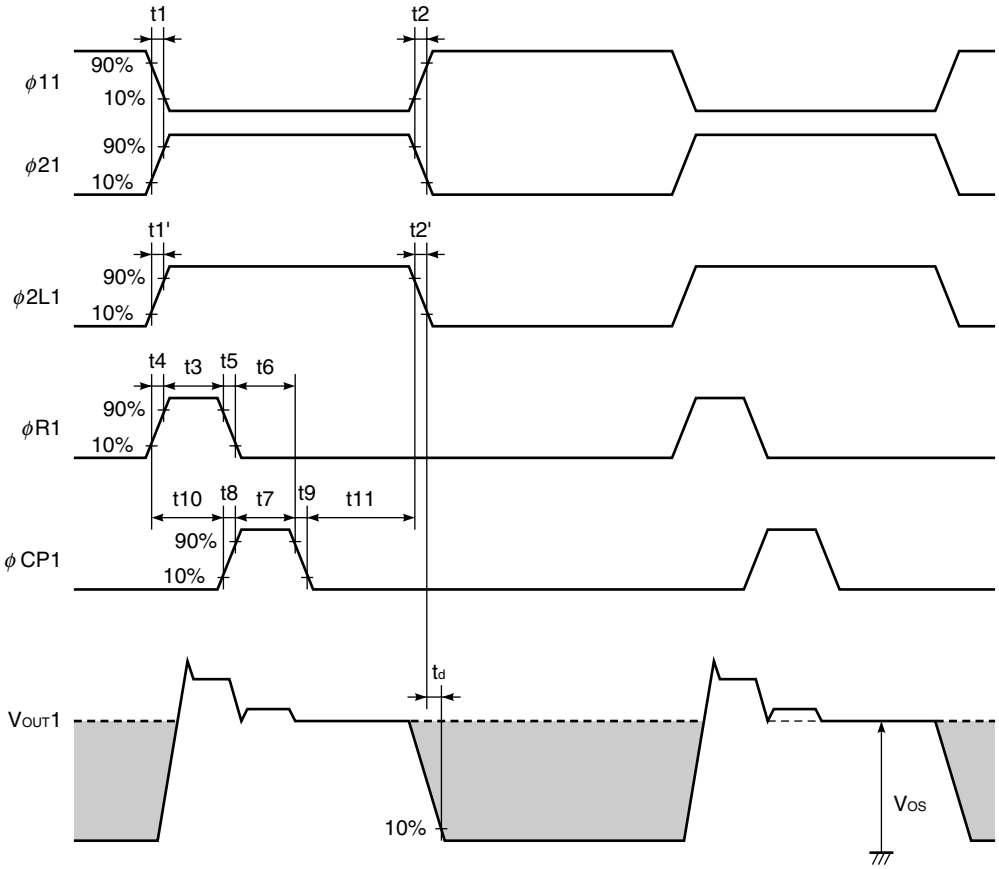
Note Set the φR1, φR2, φCP1 and φCP2 to low level during this period.

TIMING CHART 4 (Line clamp mode, In phase operation)



Note Set the φR1, φR2, φCP1 and φCP2 to low level during this period.

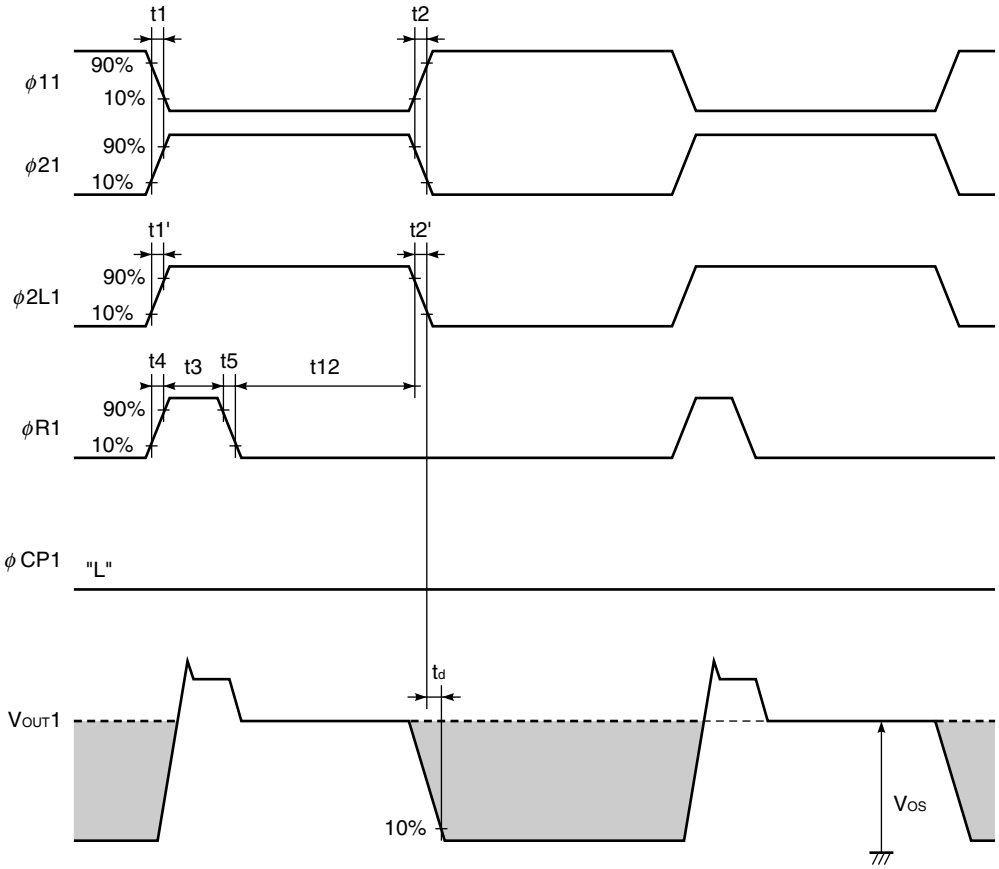
TIMING CHART 5 (Bit clamp mode)



Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	50	–	ns
t1', t2'	0	5	–	ns
t3	10	125	–	ns
t4, t5	0	5	–	ns
t6	5	125	–	ns
t7	5	125	–	ns
t8, t9	0	5	–	ns
t10	0	125	–	ns
t11	0	250	–	ns

Caution This shows timing chart of $V_{OUT}1$ side (φ11, φ21, φ2L1, φR1, φCP1, $V_{OUT}1$). The timing chart of $V_{OUT}2$ side (φ12, φ22, φ2L2, φR2, φCP2, $V_{OUT}2$) is equal.

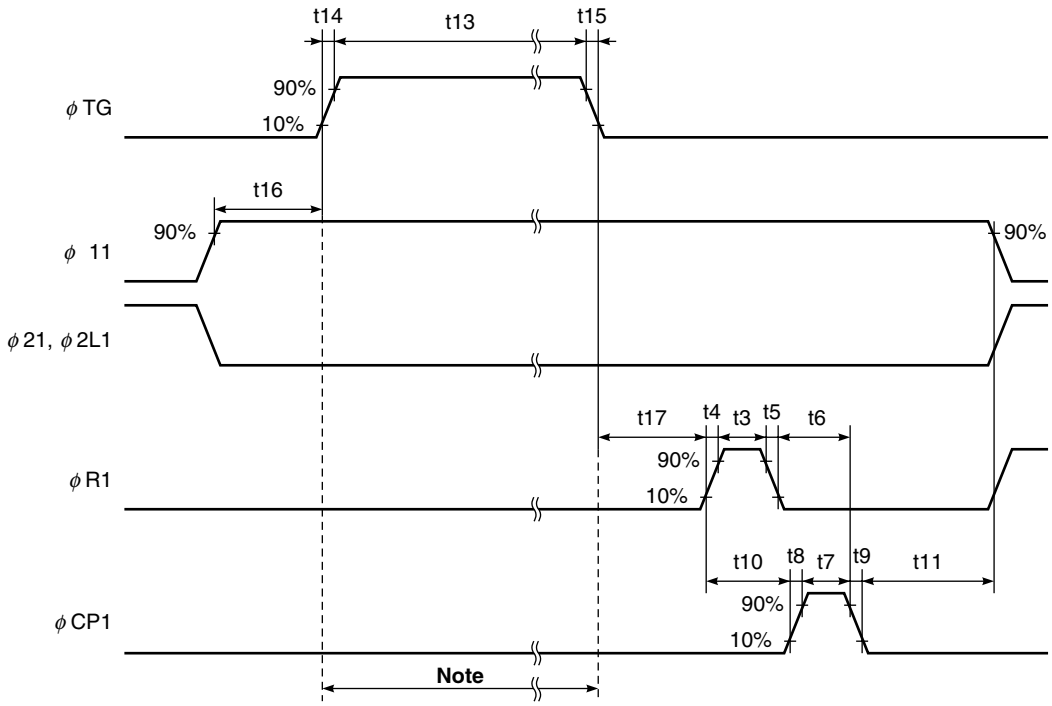
TIMING CHART 6 (Line clamp mode)



Symbol	MIN.	TYP.	MAX.	Unit
t1, t2	0	50	–	ns
t1', t2'	0	5	–	ns
t3	10	125	–	ns
t4, t5	0	5	–	ns
t12	5	250	–	ns

Caution This shows timing chart of $V_{OUT}1$ side (φ11, φ21, φ2L1, φR1, φCP1, $V_{OUT}1$). The timing chart of $V_{OUT}2$ side (φ12, φ22, φ2L2, φR2, φCP2, $V_{OUT}2$) is equal.

TIMING CHART 7 (Bit clamp mode, Line clamp mode)

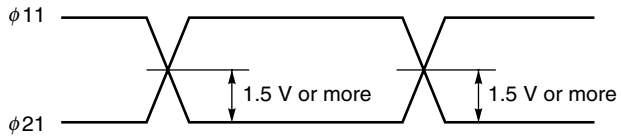


Note Set the ϕR and ϕCP to low level during this period.

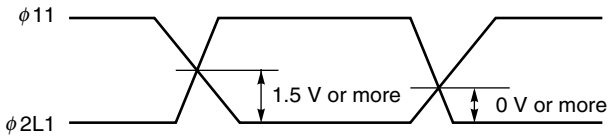
Symbol	MIN.	TYP.	MAX.	Unit
t3	10	125	–	ns
t4, t5	0	5	–	ns
t6	5	125	–	ns
t7	5	125	–	ns
t8, t9	0	5	–	ns
t10	0	125	–	ns
t11	0	250	–	ns
t13	1000	1500	10000	ns
t14, t15	0	50	–	ns
t16, t17	200	300	10000	ns

Caution This shows timing chart of VOUT1 side (ϕ11, ϕ21, ϕ2L1, ϕR1, ϕCP1, VOUT1). The timing chart of VOUT2 side (ϕ12, ϕ22, ϕ2L2, ϕR2, ϕCP2, VOUT2) is equal.

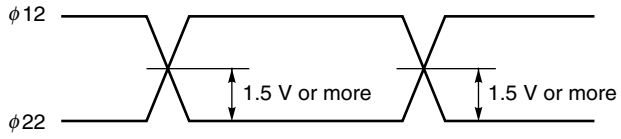
ϕ11, ϕ21 cross points



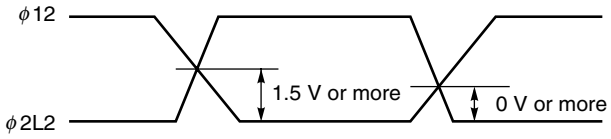
ϕ11, ϕ2L1 cross points



ϕ12, ϕ22 cross points

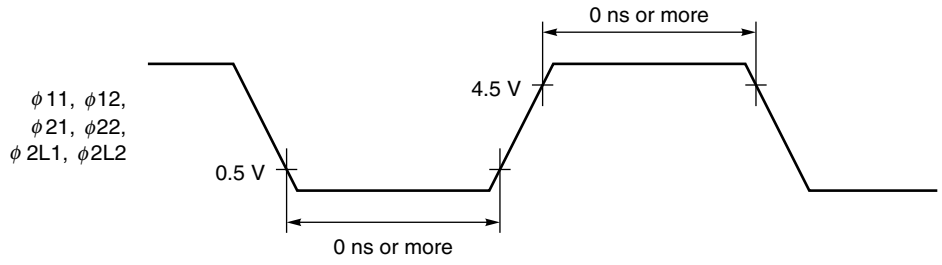


ϕ12, ϕ2L2 cross points



Remark Adjust cross points of (ϕ11, ϕ21), (ϕ11, ϕ2L1), (ϕ12, ϕ22) and (ϕ12, ϕ2L2) with input resistance of each pin.

ϕ11, ϕ12, ϕ21, ϕ22, ϕ2L1, ϕ2L2 clock width



DEFINITIONS OF CHARACTERISTIC ITEMS

1. Saturation voltage : **V_{sat}**
   Output signal voltage at which the response linearity is lost.

2. Saturation exposure : **SE**
   Product of intensity of illumination (lx) and storage time (s) when saturation of output voltage occurs.

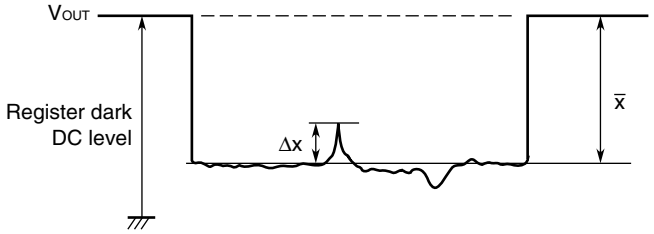
3. Photo response non-uniformity : **PRNU**
   The output signal non-uniformity of all the valid pixels when the photosensitive surface is applied with the light of uniform illumination. This is calculated by the following formula.

$$PRNU\ (\%) = \frac{\Delta x}{\overline{x}} \times 100$$

Δx: maximum of $|x_j - \overline{x}|$

$$\overline{x} = \frac{\sum_{j=1}^{7400} x_j}{7400}$$

x_j: Output voltage of valid pixel number j



4. Average dark signal : **ADS**
   Average output signal voltage of all the valid pixels at light shielding. This is calculated by the following formula.

$$ADS\ (mV) = \frac{\sum_{j=1}^{7400} d_j}{7400}$$

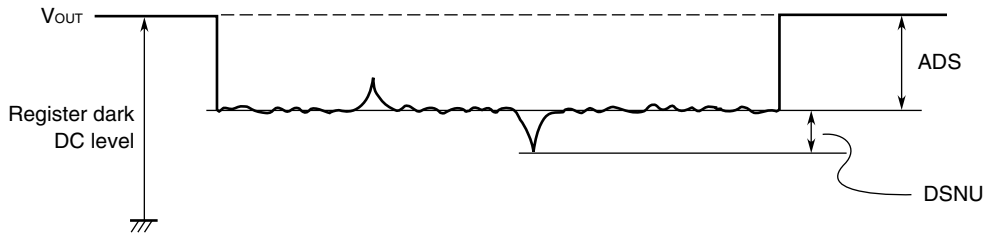
d_j: Dark signal of valid pixel number j

5. Dark signal non-uniformity : **DSNU**

Absolute maximum of the difference between ADS and voltage of the highest or lowest output pixel of all the valid pixels at light shielding. This is calculated by the following formula.

DSNU (mV): maximum of $|d_j - ADS|_{j = 1 \text{ to } 7400}$

d_j: Dark signal of valid pixel number j



6. Output impedance : **Zo**

Impedance of the output pins viewed from outside.

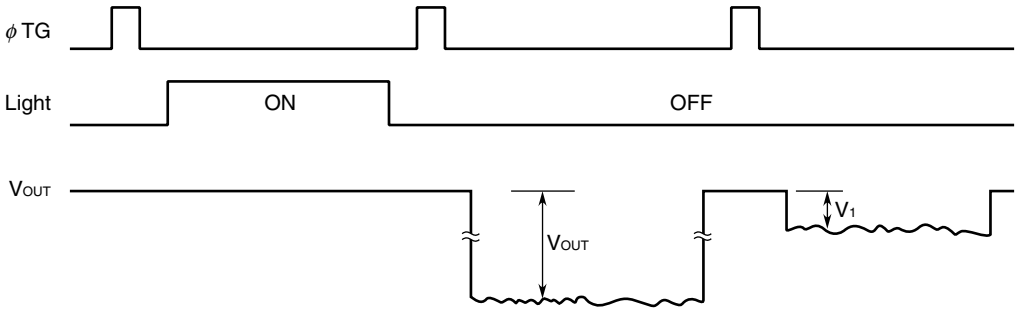
7. Response : **R**

Output voltage divided by exposure (lx•s).

Note that the response varies with a light source (spectral characteristic).

8. Image lag : **IL**

The rate between the last output voltage and the next one after read out the data of a line.

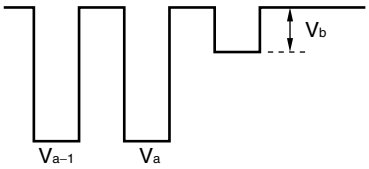


$$IL\ (\%) = \frac{V_1}{V_{OUT}} \times 100$$

9. Total transfer efficiency : **TTE**

The total transfer rate of CCD analog shift register. This is calculated by the following formula, it is difined by each output.

TTE (%) = (1 – V_b / average output of all the valid pixels) × 100



V_{a-1} : The last pixel output – 1 (Odd pixel: 7537th pixel)

V_a : The last pixel output (Odd pixel: 7539th pixel)

V_b : The spilt pixel output (Odd pixel: 7541st pixel)

10. Register imbalance : **RI**

The rate of the difference between the averages of the output voltage of Odd and Even pixels, against the average output voltage of all the valid pixels.

$$RI\ (\%) = \frac{\frac{2}{n}\left|\sum_{j=1}^{\frac{n}{2}} (V_{2j-1} - V_{2j})\right|}{\frac{1}{n}\sum_{j=1}^{n} V_j} \times 100$$

n : Number of valid pixels

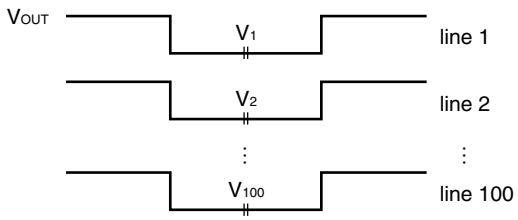
V_j : Output voltage of each pixel

11. Random noise : σ

Random noise σ is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling at dark (light shielding).

$$\sigma\ (mV) = \sqrt{\frac{\sum_{i=1}^{100} (V_i - \overline{V})^2}{100}} \quad , \quad \overline{V} = \frac{1}{100}\sum_{i=1}^{100} V_i$$

V_i : A valid pixel output signal among all of the valid pixels



This is measured by the DC level sampling of only the signal level, not by CDS (Correlated Double Sampling).

12. Shot noise : **σshot**

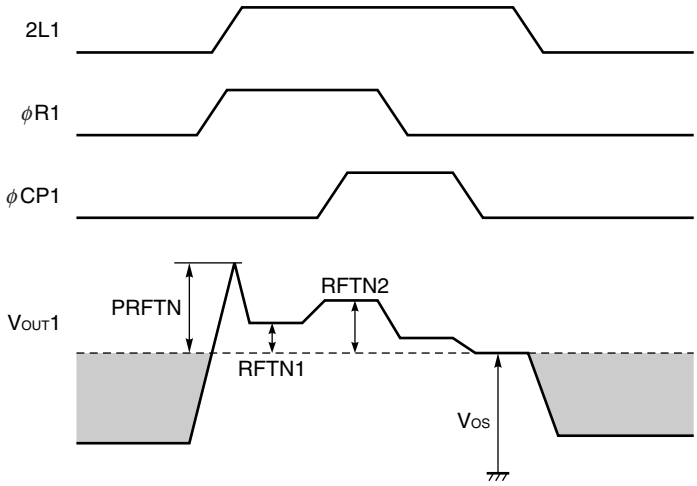
Shot noise is defined as the standard deviation of a valid pixel output signal with 100 times (= 100 lines) data sampling in the light. This includes the random noise.

The formula is the same with that of random noise.

13. Offset level : **Vos**
    DC level of output signal is defined as follows.

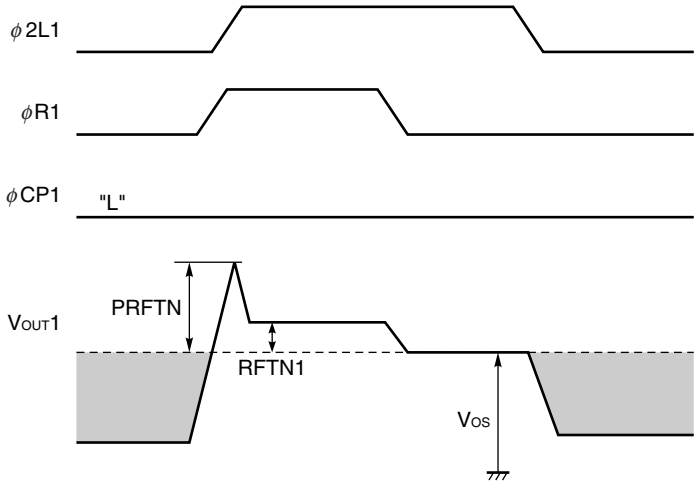
14. Reset feed-through noise and peak reset feed-through noise : **RFTN and PRFTN**
    RTFN is switching noise of ϕR and ϕCP. Reset feed-through noise (RFTN) and peak of RFTN (PRFTN) are defined as follows.

<1> Bit clamp operation



Caution This shows timing of VOUT1 side (ϕ2L1, ϕR1, ϕCP1, VOUT1). The definition of VOUT2 side (ϕ2L2, ϕR2, ϕCP2, VOUT2) is equal.

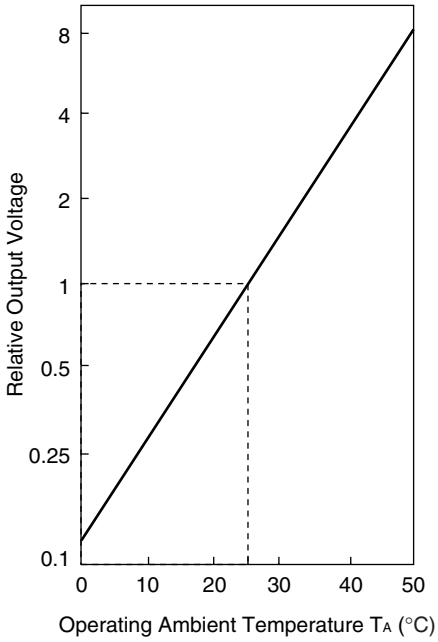
<2> Line clamp operation



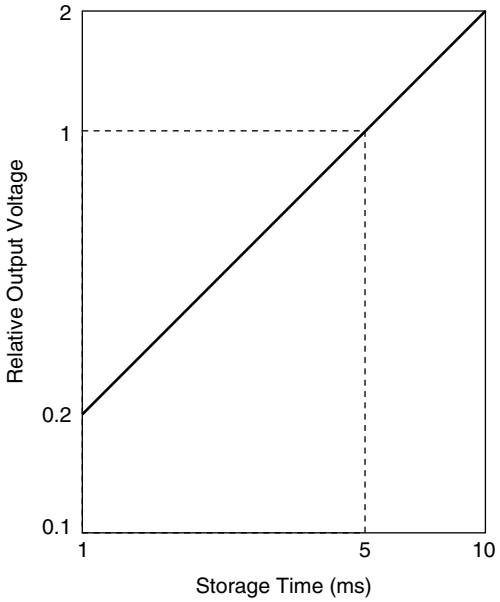
Caution This shows timing of VOUT1 side (ϕ2L1, ϕR1, ϕCP1, VOUT1). The definition of VOUT2 side (ϕ2L2, ϕR2, ϕCP2, VOUT2) is equal.

STANDARD CHARACTERISTIC CURVES (Reference Value)

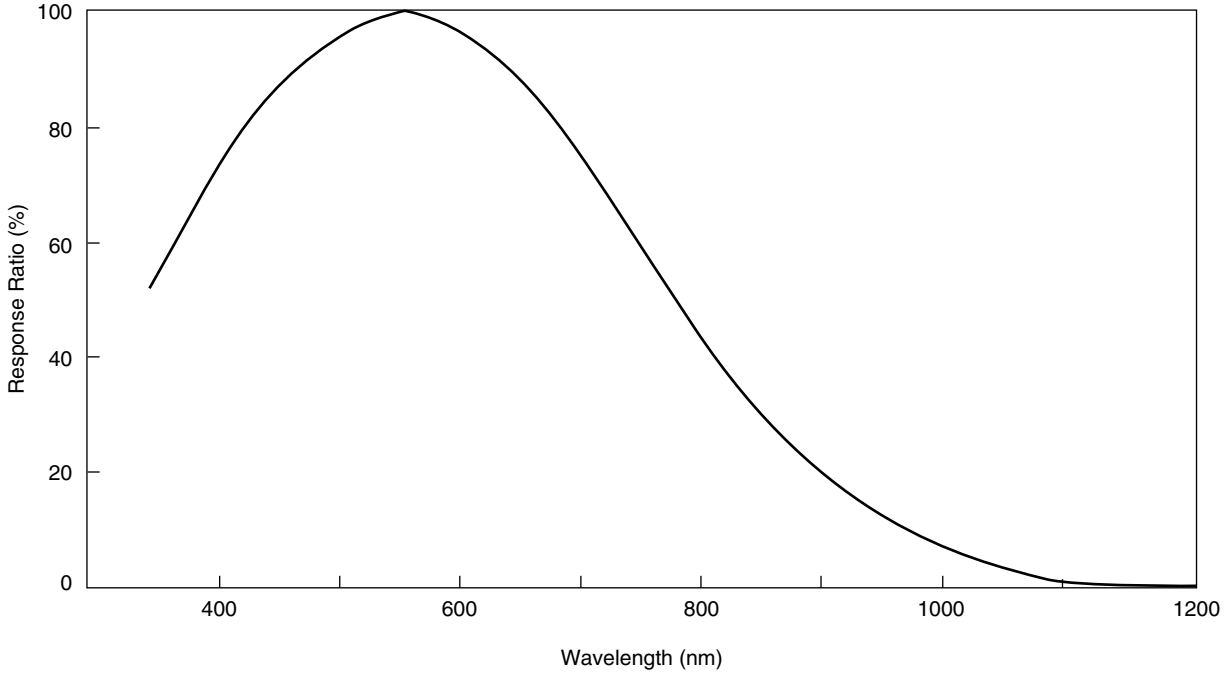
DARK OUTPUT TEMPERATURE CHARACTERISTIC



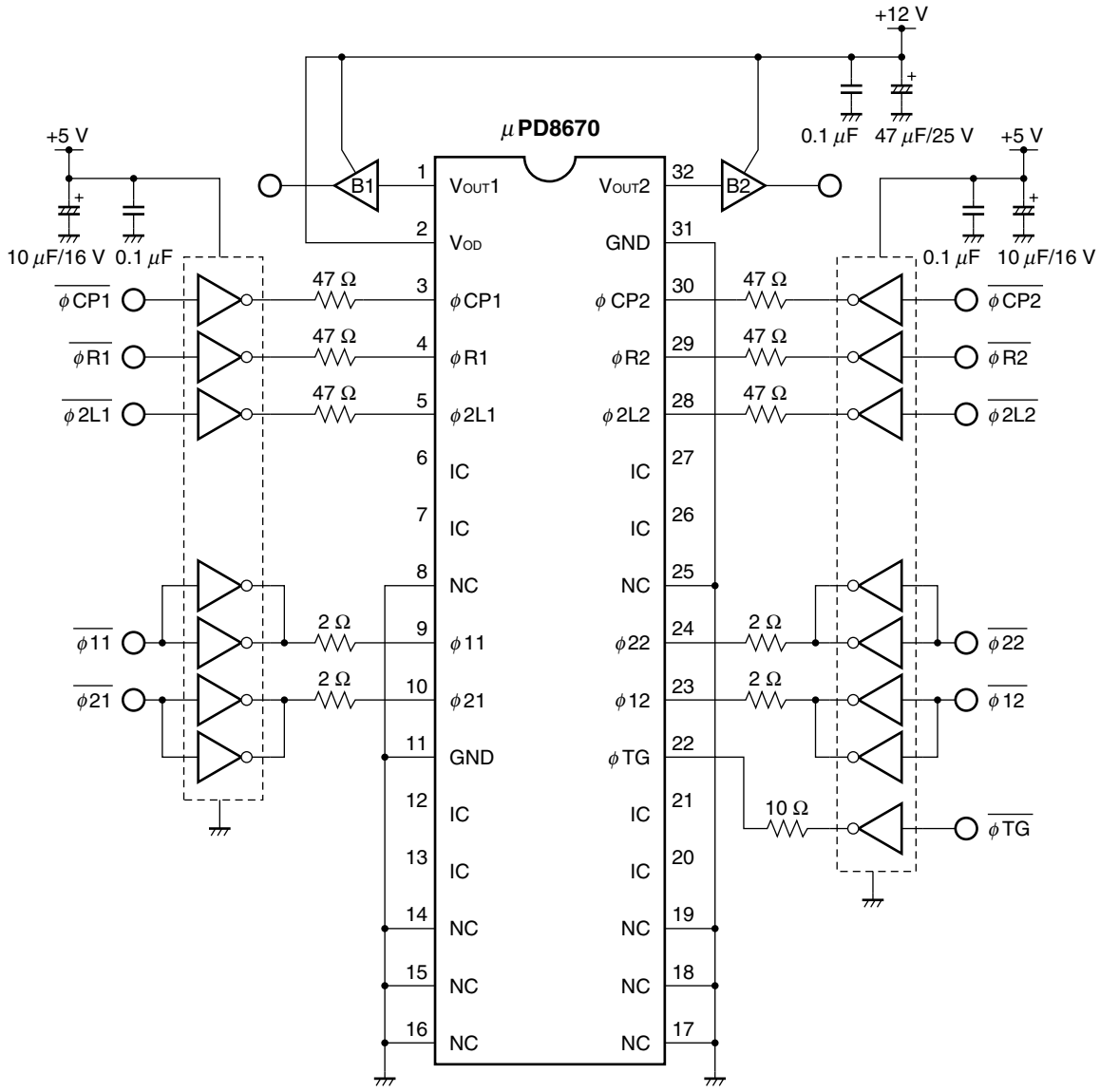
STORAGE TIME OUTPUT VOLTAGE CHARACTERISTIC (T_A = +25°C)



TOTAL SPECTRAL RESPONSE CHARACTERISTIC (without infrared cut filter and heat absorbing filter) (T_A = +25°C)



APPLICATION CIRCUIT EXAMPLE

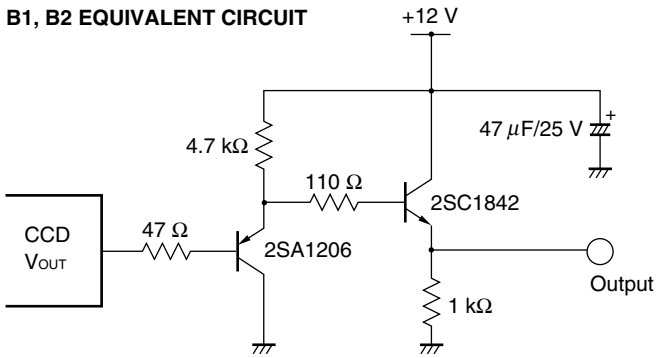


Cautions 1. Leave pins 6, 7, 12, 13, 20, 21, 26 and 27 (IC) unconnected.

2. Connect the No connection pins (NC) to GND.

Remark The inverters shown in the above application circuit example are the 74AC04.

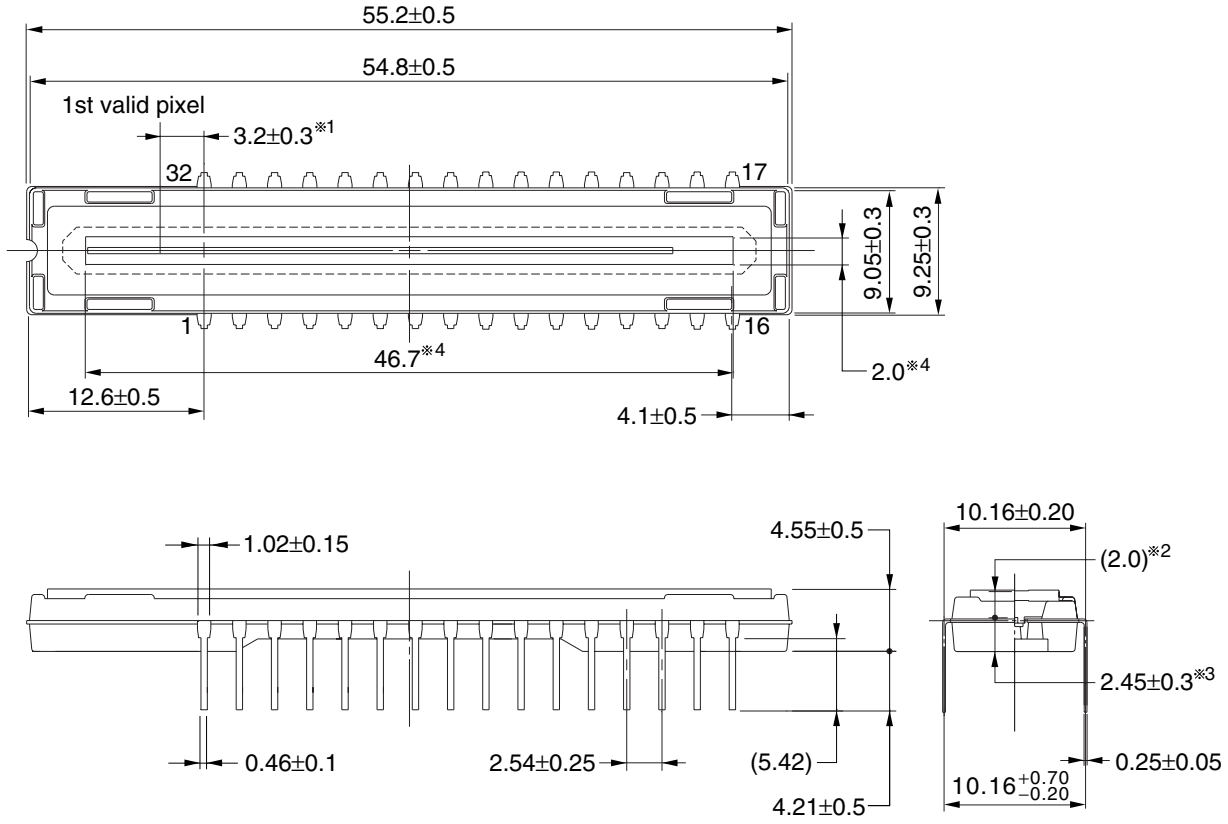
B1, B2 EQUIVALENT CIRCUIT



PACKAGE DRAWING

μPD8670CY
CCD LINEAR IMAGE SENSOR 32-PIN PLASTIC DIP (10.16 mm (400))

(Unit : mm)



Name	Dimensions	Refractive index
Plastic cap	52.2×6.4×0.8 (0.7※5)	1.5

※1 1st valid pixel ←→ The center of the pin1
※2 The surface of the CCD chip ←→ The top of the cap
※3 The bottom of the package ←→ The surface of the CCD chip
※4 Mirror finishied surface
※5 Thickness of mirror finished surface

32C-1CCD-PKG10-1

RECOMMENDED SOLDERING CONDITIONS

When soldering this product, it is highly recommended to observe the conditions as shown below.

If other soldering processes are used, or if the soldering is performed under different conditions, please make sure to consult with our sales offices.

Type of Through-hole Device

μPD8670CY : CCD linear image sensor 32-pin plastic DIP (10.16 mm (400))

Process	Conditions
Partial heating method	Pin temperature : 350°C or below, Heat time : 3 seconds or less (per pin)

Cautions 1. During assembly care should be taken to prevent solder or flux from contacting the plastic cap. The optical characteristics could be degraded by such contact.

2. Soldering by the solder flow method may have deleterious effects on prevention of plastic cap soiling and heat resistance. So the method cannot be guaranteed.

NOTES ON HANDLING THE PACKAGES

① DUST AND DIRT PROTECTING

The optical characteristics of the CCD will be degraded if the cap is scratched during cleaning. Don't either touch plastic cap surface by hand or have any object come in contact with plastic cap surface. Should dirt stick to a plastic cap surface, blow it off with an air blower. For dirt stuck through electricity ionized air is recommended. And if the plastic cap surface is grease stained, clean with our recommended solvents.

○ CLEANING THE PLASTIC CAP

Care should be taken when cleaning the surface to prevent scratches.

We recommend cleaning the cap with a soft cloth moistened with one of the recommended solvents below. Excessive pressure should not be applied to the cap during cleaning. If the cap requires multiple cleanings it is recommended that a clean surface or cloth be used.

○ RECOMMENDED SOLVENTS

The following are the recommended solvents for cleaning the CCD plastic cap.

Use of solvents other than these could result in optical or physical degradation in the plastic cap. Please consult your sales office when considering an alternative solvent.

Solvents	Symbol
Ethyl Alcohol	EtOH
Methyl Alcohol	MeOH
Isopropyl Alcohol	IPA
N-methyl Pyrrolidone	NMP

② MOUNTING OF THE PACKAGE

The application of an excessive load to the package may cause the package to warp or break, or cause chips to come off internally. Particular care should be taken when mounting the package on the circuit board. Don't have any object come in contact with plastic cap. You should not reform the lead frame. We recommended to use a IC-inserter when you assemble to PCB.

Also, be care that the any of the following can cause the package to crack or dust to be generated.

1. Applying heat to the external leads for an extended period of time with soldering iron.
2. Applying repetitive bending stress to the external leads.
3. Rapid cooling or heating

③ OPERATE AND STORAGE ENVIRONMENTS

Operate in clean environments. CCD image sensors are precise optical equipment that should not be subject to mechanical shocks. Exposure to high temperatures or humidity will affect the characteristics. So avoid storage or usage in such conditions.

Keep in a case to protect from dust and dirt. Dew condensation may occur on CCD image sensors when the devices are transported from a low-temperature environment to a high-temperature environment. Avoid such rapid temperature changes.

For more details, refer to our document "Review of Quality and Reliability Handbook" (C12769E)

④ ELECTROSTATIC BREAKDOWN

CCD image sensor is protected against static electricity, but destruction due to static electricity is sometimes detected. Before handling be sure to take the following protective measures.

1. Ground the tools such as soldering iron, radio cutting pliers of or pincer.
2. Install a conductive mat or on the floor or working table to prevent the generation of static electricity.
3. Either handle bare handed or use non-chargeable gloves, clothes or material.
4. Ionized air is recommended for discharge when handling CCD image sensor.
5. For the shipment of mounted substrates, use box treated for prevention of static charges.
6. Anyone who is handling CCD image sensors, mounting them on PCBs or testing or inspecting PCBs on which CCD image sensors have been mounted must wear anti-static bands such as wrist straps and ankle straps which are grounded via a series resistance connection of about 1 MΩ.

[NOTE]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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