54LS/74LS256

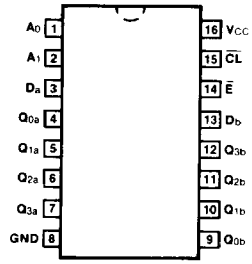
DUAL 4-BIT ADDRESSABLE LATCH

DESCRIPTION — The '256 is a dual 4-bit addressable latch with common control inputs; these include two Address inputs (A_0, A_1), an active LOW Enable input ($\overline{E}$) and an active LOW Clear input ($\overline{CL}$). Each latch has a Data input (D) and four outputs (Q_0 — Q_3).

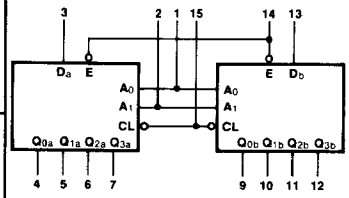
When the Enable ($\overline{E}$) is HIGH and the Clear input ($\overline{CL}$) is LOW, all outputs (Q_0 — Q_3) are LOW. Dual 4-channel demultiplexing occurs when the $\overline{CL}$ and $\overline{E}$ are both LOW. When $\overline{CL}$ is HIGH and $\overline{E}$ is LOW, the selected output (Q_0 — Q_3), determined by the Address inputs, follows D. When the $\overline{E}$ goes HIGH, the contents of the latch are stored. When operating in the addressable latch mode ($\overline{E}$ = LOW, $\overline{CL}$ = HIGH), changing more than one bit of the Address (A_0, A_1) could impose a transient wrong address. Therefore, this should be done only while in the memory mode ($\overline{E}$ = $\overline{CL}$ = HIGH).

- **SERIAL-TO-PARALLEL CAPABILITY**
- **OUTPUT FROM EACH STORAGE BIT AVAILABLE**
- **RANDOM (ADDRESSABLE) DATA ENTRY**
- **EASILY EXPANDABLE**
- **ACTIVE LOW COMMON CLEAR**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE: VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE: VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS256PC		9B
Ceramic DIP (D)	A	74LS256DC	54LS256DM	6B
Flatpak (F)	A	74LS256FC	54LS256FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
A_0, A_1	Common Address Inputs	0.5/0.25
D_a, D_b	Data Inputs	0.5/0.25
$\overline{E}$	Common Enable Input (Active LOW)	1.0/0.5
$\overline{CL}$	Conditional Clear Input (Active LOW)	0.5/0.25
Q_{0a} — Q_{3a}	Side A Latch Outputs	10/5.0 (2.5)
Q_{0b} — Q_{3b}	Side B Latch Outputs	10/5.0 (2.5)

TRUTH TABLE

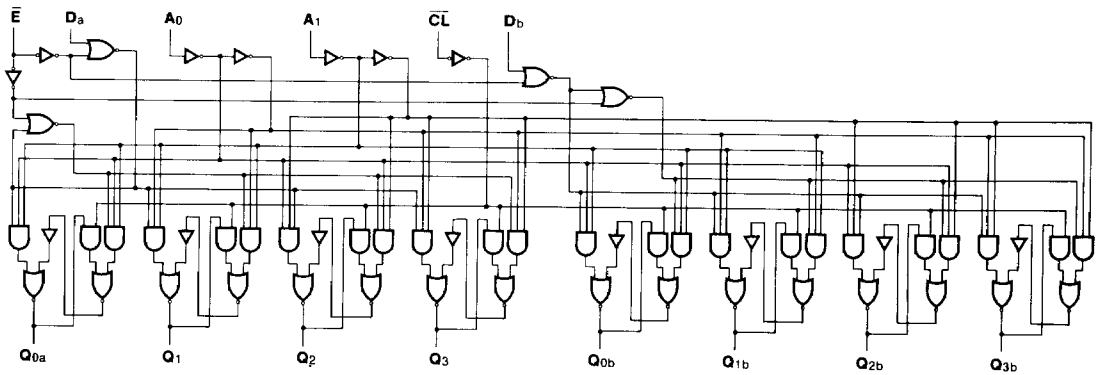
INPUTS				OUTPUTS				MODE
$\overline{CL}$	$\overline{E}$	A_0	A_1	Q_0	Q_1	Q_2	Q_3	
L	H	X	X	L	L	L	L	Clear
L	L	L	L	D	L	L	L	Demultiplex
L	L	H	L	L	D	L	L	
L	L	L	H	L	L	D	L	
L	L	H	H	L	L	L	D	
H	H	X	X	Q_{t-1}	Q_{t-1}	Q_{t-1}	Q_{t-1}	Memory
H	L	L	L	D	Q_{t-1}	Q_{t-1}	Q_{t-1}	Addressable Latch
H	L	H	L	Q_{t-1}	D	Q_{t-1}	Q_{t-1}	
H	L	L	H	Q_{t-1}	Q_{t-1}	D	Q_{t-1}	
H	L	H	H	Q_{t-1}	Q_{t-1}	Q_{t-1}	D	

t-1 = Bit time before address change or rising edge of E
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

MODE SELECTION

$\overline{E}$	$\overline{CL}$	MODE
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 4-Channel Demultiplexers
H	L	Clear

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		25	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n		27 24	ns	Figs. 3-1, 3-9
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n		30 20	ns	Figs. 3-1, 3-5
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n		30 20	ns	Figs. 3-1, 3-20
t_{PHL}	Propagation Delay $\overline{CL}$ to Q_n		18	ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H)	Setup Time HIGH D_n to $\overline{E}$	20		ns	Fig. 3-13
t_h (H)	Hold Time HIGH D_n to $\overline{E}$	0		ns	Fig. 3-13
t_s (L)	Setup Time LOW D_n to $\overline{E}$	15		ns	Fig. 3-13
t_h (L)	Hold Time LOW D_n to $\overline{E}$	0		ns	Fig. 3-13
t_s (H) t_s (L)	Setup Time HIGH or LOW, A_n to $\overline{E}$	0		ns	Fig. 3-21
t_w (L)	$\overline{E}$ Pulse Width LOW	17		ns	Fig. 3-21