

# M62332P/FP, M62337P/FP

R03DS0037EJ0500 Rev.5.00 Jun 03, 2011

8-bit 2ch I<sup>2</sup>C BUS D/A Converter with Buffer Amplifiers

### Description

The M62332/M62337 is an integrated circuit semiconductor of CMOS structure with 2 channels of built in D/A converters with output buffer operational amplifiers.

The input is 2-wires serial method is used for the transfer format of digital data to allow connection with a microcomputer with minimum wiring.

The output buffer operational amplifier employs AB class output circuit with sync and source drive capacity of 1.0 mA or more, and it operates in the whole voltage range from  $V_{CC}$  to ground.

The M62332 and the M62337 differ only in their slave address.

### Features

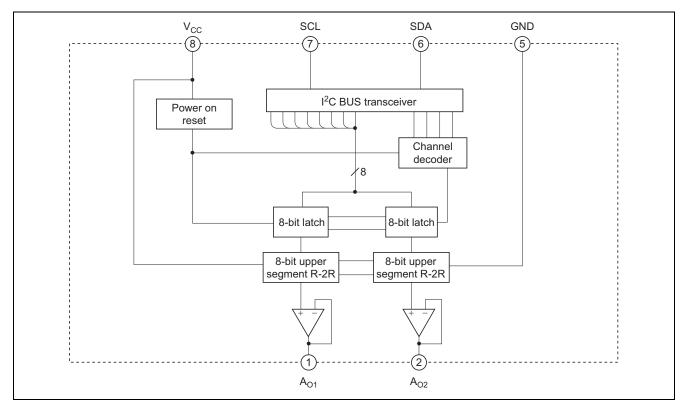
- Digital data transfer format: I<sup>2</sup>C BUS serial data method
- Output buffer operational amplifier: It operates in the whole voltage range from V<sub>CC</sub> to ground.
- High output current drive capacity: ±1.0 mA over

## Application

Conversion from digital data to analog control data for home-use and industrial equipment.

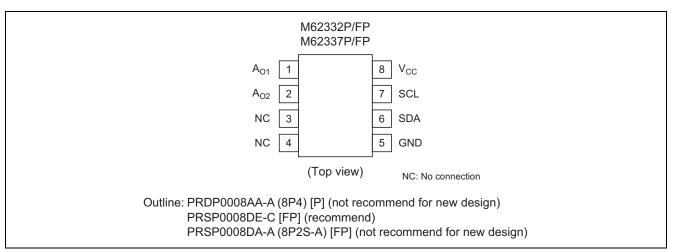
Signal gain control or automatic adjustment of display-monitor or CTV.

### **Block Diagram**





# **Pin Arrangement**



# **Pin Description**

Pin No.	Pin Name	Function						
6	SDA	Serial data input terminal						
7	SCL	erial clock input terminal						
1	A <sub>O1</sub>	3-bit resolution D/A converter output terminal						
2	A <sub>O2</sub>							
8	V <sub>cc</sub>	Power supply terminal						
5	GND	GND terminal						



# **Absolute Maximum Ratings**

ltem	Symbol	Ratings	Unit
Supply voltage	V <sub>CC</sub>	–0.3 to +7.0	V
Input voltage	V <sub>in</sub>	–0.3 to V <sub>CC</sub> + 0.3	V
Output voltage	Vo	–0.3 to V <sub>CC</sub> + 0.3	V
Power dissipation	Pd	417 (P) / 272 (FP)	mW
Operating temperature	Topr	-20 to +85	°C
Storage temperature	Tstg	-40 to +125	°C

# **Electrical Characteristics**

(V<sub>CC</sub> = +5 V  $\pm$  10%, GND = 0 V, Ta = -20 to +85°C unless otherwise noted)

		( · tt		,		
		Limits				
ltem	Symbol	Min	Тур	Max	Unit	Test Conditions
Supply voltage	V <sub>CC</sub>	2.7	5.0	5.5	V	
Supply current	I <sub>CC</sub>	0	0.6	2.5	mA	CLK = 500 kHz operation, $I_{AO} = 0 \ \mu A$ Data: 6Ah (at maximum current)
		0	0.4	1.6	mA	$SDA = SCL = GND, I_{AO} = 0 \mu A$
Output low voltage (SDA)	V <sub>OL</sub>	_	_	0.4	V	lsink = 3 mA
Input leak current	I <sub>ILK</sub>	-10	_	10	μΑ	$V_{IN} = 0$ to $V_{CC}$
Input low voltage	V <sub>IL</sub>	_	_	0.2 V <sub>CC</sub>	V	
Input high voltage	V <sub>IH</sub>	0.8 V <sub>CC</sub>	_	—	V	
Buffer amplifier output	V <sub>AO</sub>	0.1	_	$V_{CC} - 0.1$	V	I <sub>AO</sub> = ±100 μA
voltage range		0.2	_	$V_{CC} - 0.2$	V	I <sub>AO</sub> = ±500 μA
Buffer amplifier output drive range	I <sub>AO</sub>	-1.0	_	1.0	mA	Upper side saturation voltage = 0.3 V Lower side saturation voltage = 0.2 V
Differential nonlinearity	S <sub>DL</sub>	-1.0	_	1.0	LSB	V <sub>CC</sub> = 5.12 V (20 mV/LSB)
Nonlinearity	SL	-1.5	_	1.5	LSB	without load $(I_{AO} = 0)$
Zero code error	SZERO	-2.0	_	2.0	LSB	
Full scale error	SFULL	-2.0		2.0	LSB	
Output capacitate load	Co			0.1	μF	
Buffer amplifier output impedance	R <sub>o</sub>		5.0	—	Ω	

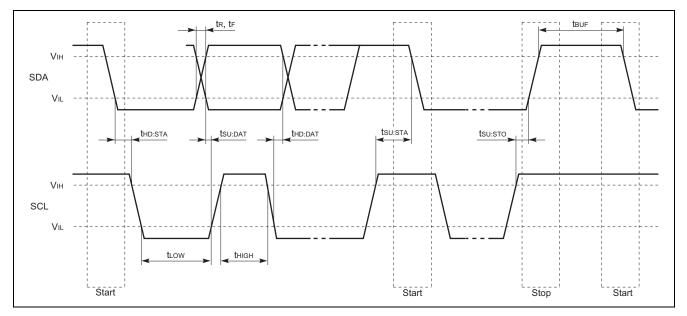


# I<sup>2</sup>C BUS Line Characteristics

Item	Symbol	Min	Мах	Unit
SCL clock frequency	f <sub>SCL</sub>	0	100	kHz
Time the bus must be free before a new transmission can	t <sub>BUF</sub>	4.7	—	μS
start				
Hold time START condition	t <sub>HD:STA</sub>	4.0	—	μS
(After this period, the first clock pulse is generated)				
Low period of the clock	t <sub>LOW</sub>	4.7	—	μS
High period of the clock	t <sub>HIGH</sub>	4.0	—	μS
Set-up time for START condition	t <sub>SU:STA</sub>	4.7	—	μS
(Only relevant for a repeated START condition)				
Hold time DATA	t <sub>HD:DAT</sub>	0	—	μS
Set-up time DATA	t <sub>SU:DAT</sub>	250	—	μS
Rise time of both SDA and SCL lines	t <sub>R</sub>	_	1000	ns
Fall time of both SDA and SCL lines	t <sub>F</sub>	—	300	ns
Set-up time for STOP condition	t <sub>SU:STO</sub>	4.0	—	μS

Note: Transmitter must internal provide at least a hold time to bridge the undefined region (300 ns Max) of the falling edge of SCL.

# **Timing Chart**



# I<sup>2</sup>C BUS Format

STA	Slave address	W	А	Sub address	Α	DAC data	Α	STP	
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Note: STA: start condition, A: affirmation bit, W: write (SDA = Low), STP: stop condition

Slave address

M62332



First -						► Last
1	0	0	1	1	0	1

#### • Sub address

First -							➤ Last
х	х	х	х	х	Х	х	S0
-		Dor	n't care				Channel elect data

#### Channel select data

M62337

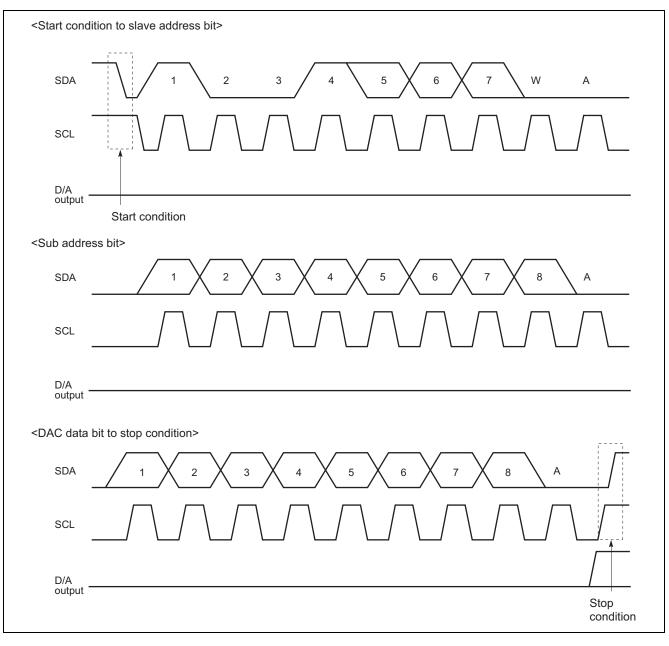
S0	Channel Selection
0	ch1 selection
1	ch2 selection

#### • DAC data

First MSB			t 3					
D7	D6	D5	D4	D3	D2	D1	D0	
First MSB							→ Las LSE	
D7	D6	D5	D4	D3	D2	D1	D0	DAC output
0	0	0	0	0	0	0	0	$V_{CC}$ / 256 $\times$ 1
0	0	0	0	0	0	0	1	$V_{CC}$ / 256 $\times$ 2
0	0	0	0	0	0	1	0	$V_{CC}$ / 256 $\times$ 3
0	0	0	0	0	0	1	1	$V_{CC}$ / 256 $ imes$ 4
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	0	$V_{CC}$ / 256 $\times$ 255
1	1	1	1	1	1	1	1	V <sub>CC</sub>

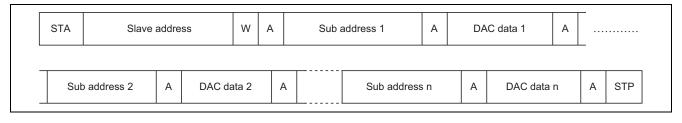


# **Timing Chart (Model)**



- Start condition With SCL at High, SDA line goes from High to Low
  - Stop condition With SCL at High, SDA line goes from Low to High
- (Under normal circumstances, SDA is changed when SCL is Low)
- Acknowledge bit The receiving IC has to pull down SDA line whenever receive slave data. (The transmitting IC releases the SDA line just then transmit 8-bit data.)

# **Digital Data Formats**

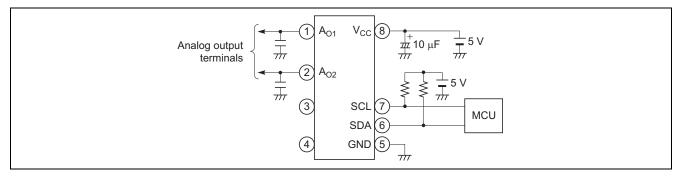




### **Precaution for Use**

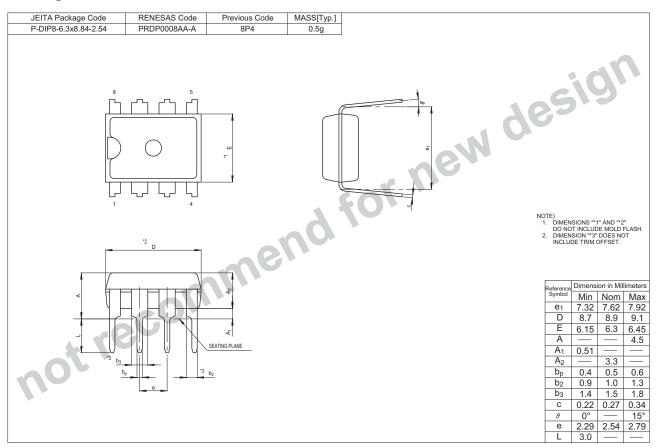
- Supply voltage terminal (V<sub>CC</sub>) is also used for D/A converter upper reference voltage setting. If ripple or spike is input this terminal, accuracy of D/A conversion is down. So, when use this device, please connect capacitor among V<sub>CC</sub> to GND for stable D/A conversion.
- This IC's output amplifier has an advantage to capacitive load. So it's no problem at device action when connect capacitor (0.1  $\mu$ F Max) among output to GND for every noise eliminate.
- Purchase of Renesas's I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components an I<sup>2</sup>C system, provided that the system conforms to I<sup>2</sup>C Standard Specification as defined by Philips.

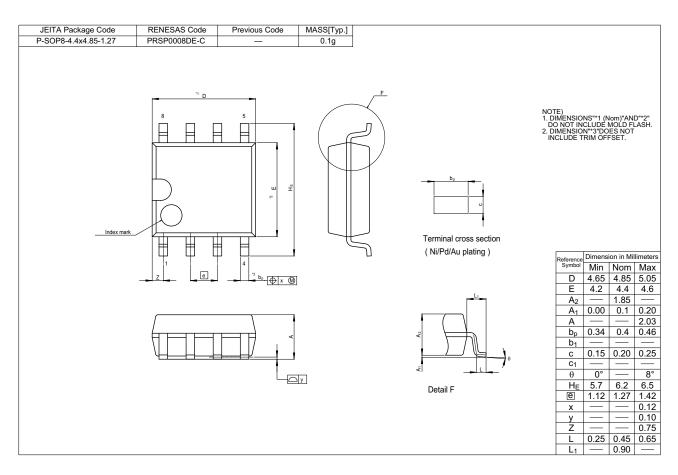
# **Application Example**





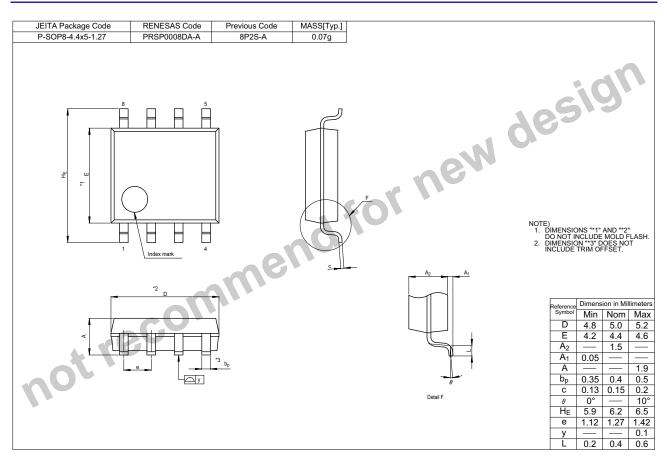
### **Package Dimensions**







#### M62332P/FP, M62337P/FP





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