QUALITY SEMICONDUCTOR, INC.

High-Speed CMOS 18-Bit Register

QS74FCT16823T
QS74FCT162823T

ADVANCE INFORMATION

FEATURES/BENEFITS

- Pin and function compatible with T.I. Widebus™ and IDT Double-Density™ families
- CMOS power levels: <1μW typical standby
- SSOP (PV) and TSSOP (PA) packages
- Low output skew: 0.5ns $t_{SK(O)}$
- Flow-through pinout for easy layout
- Power off disable allows hot plugging
- Industrial temperature: –40°C to +85°C
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise

FCT16823T

- High drive standard FCT-T outputs: I_{OL} = +64mA, I_{OH} = –32mA
- Incident switching for driving buses and large loads

FCT162823T

- Balanced output drivers: ±24mA
- Reduced switching noise for point to point signals

DESCRIPTION

The FCT16823 family of products are 18-bit registers with three-state outputs that are ideal for driving address and data buses. Two independent 9-bit registers are used with separate controls to permit independent control of data flow in parity-based systems. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for system designers. All outputs have ground bounce suppression circuitry (see QSI Application Note AN-01) and many power and ground pins provide low ground bounce. To accommodate hot-plug or live insertion applications, both versions of this product are designed not to load an active bus when V_{CC} is removed. In applications where bus signals are point-to-point or driving light capacitance loads, the balanced drive FCT162823 is recommended.

Figure 1. Functional Block Diagram

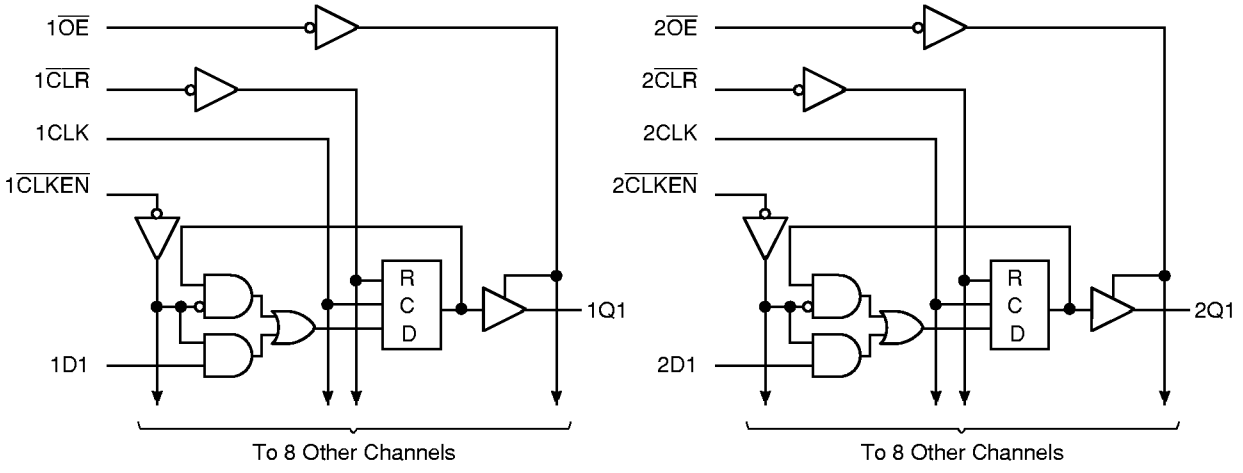

Figure 2. Pin Configuration (All Pins Top View)

SSOP, TSSOP

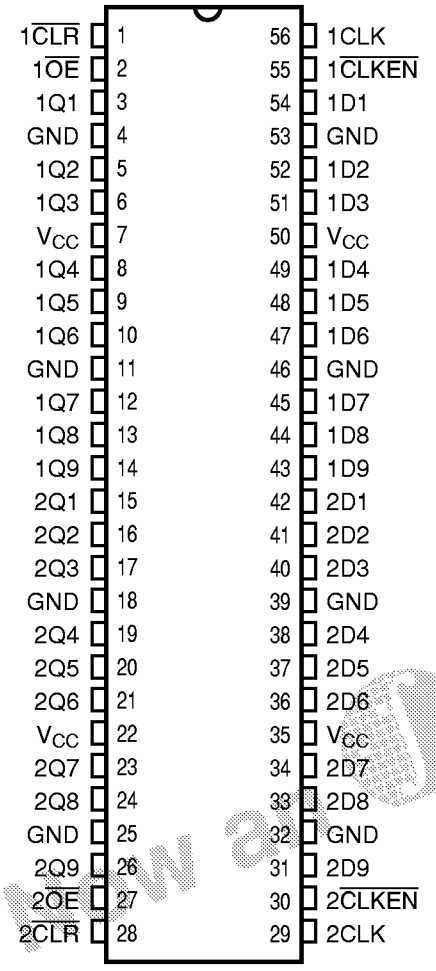

Table 1. Pin Description

Name	I/O	Description
xDx	I	Data Inputs
xQx	O	Data Outputs-Three State
x$\overline{OE}$	I	Output Enables (Active Low)
xCLK	I	Clock Inputs
x$\overline{CLKEN}$	I	Clock Enables (Active Low)
x$\overline{CLR}$	I	Asynchronous Clear

Table 2. Absolute Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Output Voltage V_{OUT}	–0.5V to +7.0V
DC Input Voltage V_{IN}	–0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20 ns)	–3.0V
DC Input Diode Current with $V_{IN} < 0$	–20mA
DC Output Diode Current with $V_{OUT} < 0$	–50mA
DC Output Current Max. Sink Current/Pin	120mA
Maximum Power Dissipation	1.0W
T_{STG} Storage Temperature	–65° to +150°C

Note: Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

Table 3. Capacitance

T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V

Pins	Typ	Max	Unit
All	6.0	9.0	pF

Table 4. Function Table

Inputs					Int.	O/P	
$\overline{OE}$	$\overline{CLR}$	$\overline{CLKEN}$	Di	CLK	Qi	Yi	Function
H	X	X	X	X	X	X	High Z
H	L	X	X	X	L	Hi-Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Hi-Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	L	↑	L	Hi-Z	Load
H	H	L	H	↑	H	Hi-Z	Load
L	H	L	L	↑	L	L	Load
L	H	L	H	↑	H	H	Load

Table 5. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_{OUT}	Voltage Applied to Output or I/O	0	V_{CC}	V
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V
T_A	Operating Free Air Temperature	–40	+85	°C

Table 6. DC Electrical Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise noted.

Symbol	Parameter	Test Conditions[1]	Min	Typ[2]	Max	Unit
V_{IH}	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
V_{IL}	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
ΔV_T	Input Hysteresis[4]	$V_{TLH} - V_{THL}$ for All Inputs	—	100	—	mV
$\lvert I_{IH} \rvert$ $\lvert I_{IL} \rvert$	Input Current Input HIGH or LOW	V_{CC} = Max., $0 \le V_{IN} < V_{CC}$	—	—	1	µA
$\lvert I_{OZ} \rvert$	Off-State Output Current (Hi-Z)	V_{CC} = Max., $0 \le V_{OUT} \le V_{CC}$	—	—	1	µA
$\lvert I_{OFF} \rvert$	Power off leakage[5]	V_{CC} = 0V, $V_{IN}/_{OUT} \le 4.5V$	—	—	1	µA
I_{OS}	Short Circuit Current[3,4]	V_{CC} = Max., V_{OUT} = GND	–80	–140	–225	mA
I_O	Output Current Drive[3]	V_{CC} = Max., V_{OUT} = 2.5V	–50	—	–180	mA
V_{IK}	Input Clamp Voltage	V_{CC}= Min., I_{IN} = –18mA	—	–0.7	–1.2	V

Notes:
1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
3. Not more than one output should be tested at one time. Duration of test should not exceed one second.
4. These parameters are guaranteed by design but not tested.
5. The test limit for this parameter is ± 5µA at T_A = –55°C

Table 7. Output Drive Characteristics for FCT16823T

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –3mA	2.5	3.4	—	V
			I_{OH} = –15mA	2.4	3.2	—	V
			I_{OH} = –32mA[4]	2.0	3.0	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	—	0.3	0.55	V

Table 8. Output Drive Characteristics for FCT162823T

Symbol	Parameter	Test Conditions[1]		Min	Typ[2]	Max	Unit
I_{ODL}	Output LOW Current[3]	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V		60	115	150	mA
I_{ODH}	Output HIGH Current[3]	V_{CC} = 5V, V_{IN} = V_{IH} or V_{IL} V_{OUT} = 1.5V		–60	–115	–150	mA
V_{OH}	Output HIGH Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OH} = –24mA	2.4	3.3	—	V
V_{OL}	Output LOW Voltage	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24mA	—	0.3	0.55	V

Notes:
1. For conditions shown as Min. or Max. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values indicate V_{CC} = 5.0V and T_A = 25°C.
3. Not more than one output should be shorted and the duration is ≤1 second.
4. Duration of the condition should not exceed one second.

Table 9. Power Supply Characteristics

Symbol	Parameter	Test Conditions[1]		Typ [2]	Max	Unit
I_{CCL} I_{CCH} I_{CCZ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		5	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max., V_{IN} = 3.4V[3]		0.5	1.5	mA
Q_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open One Bit Toggling @ 50% Duty Cycle xDIR = $x\overline{OE}$ = GND	V_{IN} = V_{CC} V_{IN} = GND	75	120	µA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open One Bit Toggling @ 50% Duty Cycle f_i = 5MHz, f_{CP} = 10MHz (xCLKBA) $x\overline{OE}$ = $x\overline{CLKEN}$ = GND	V_{IN} = V_{CC} V_{IN} = GND	0.8	1.7[5]	mA
			V_{IN} = 3.4 V V_{IN} = GND	1.3	3.2[5]	mA
		V_{CC} = Max., Outputs Open Eighteen Bits Toggling @ 50% Duty Cycle f_i = 2.5MHz, f_{CP} = 10MHz (xCLKBA) $x\overline{OE}$ = $x\overline{CLKEN}$ = GND	V_{IN} = V_{CC} V_{IN} = GND	4.2	7.1[5]	mA
			V_{IN} = 3.4 V V_{IN} = GND	9.2	22.1[5]	mA

Notes:

1. For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V). All Other Inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed by design but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$.
   $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP}/2 + f_i N_i)$.
   I_{CCQ} = Quiescent Current (I_{CCL}, I_{CCH}, and I_{CCZ}).
   ΔI_{CC} = Power Supply Current for a TTL-High Input (V_{IN} = 3.4V).
   D_H = Duty Cycle for TTL High Inputs.
   N_T = Number of TTL High Inputs.
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
   f_{CP} = Clock Frequency for Register devices (Zero for Non-Register Devices).
   N_{CP} = Number of Clock Inputs at f_{CP}.
   f_i = Input Frequency.
   N_i = Number of Inputs at f_i.

Table 10. Switching Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise specified.

Symbol	Parameter[1]	Condition	FCT16823AT FCT162823AT		FCT16823BT FCT162823BT		FCT16823CT FCT162823CT		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay xCLK to xQX	C_L = 50pF R_L = 500Ω	1.5	10.0	1.5	7.5	1.5	6.0	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	20.0	1.5	15.0	1.5	12.5	
t_{PHL}	Propagation Delay x$\overline{CLR}$ to xQX	C_L = 50pF R_L = 500Ω	1.5	14.0	1.5	9.0	1.5	8.0	ns
t_{PZH} t_{PZL}	Output Enable Time x$\overline{OE}$ to xQX	C_L = 50pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	7.0	ns
		C_L = 300pF[3] R_L = 500Ω	1.5	23.0	1.5	15.0	1.5	12.5	
t_{PHZ} t_{PLZ}	Output Disable Time[3] x$\overline{OE}$ to xQX	C_L = 5pF R_L = 500Ω	1.5	7.0	1.5	6.5	1.5	6.2	ns
		C_L = 50pF R_L = 500Ω	1.5	8.0	1.5	7.5	1.5	6.5	
t_{SU}	Set-up Time HIGH or LOW xDx to xCLK	C_L = 50pF R_L = 500Ω	4.0	—	3.0	—	3.0	—	
t_H	Hold Time HIGH or LOW xDx to xCLK		2.0	—	1.5	—	0.0	—	ns
t_{SU}	Set-up Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		4.0	—	3.0	—	3.0	—	ns
t_H	Hold Time HIGH or LOW x$\overline{CLKEN}$ to xCLK		2.0	—	0	—	0	—	ns
t_W	xCLK Pulse Width HIGH or LOW		7.0	—	6.0	—	6.0	—	ns
t_W	x$\overline{CLR}$ Pulse Width LOW		6.0	—	6.0	—	6.0	—	ns
t_{REM}	Recovery Time x$\overline{CLR}$ to xCLK		6.0	—	6.0	—	6.0	—	ns
$t_{SK(O)}$	Output skew[2]		—	0.5	—	0.5	—	0.5	ns

Notes:

1. Minimums are guaranteed but not production tested. See test circuit and waveforms.
2. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization.
3. This condition is guaranteed by characterization but not production tested.