



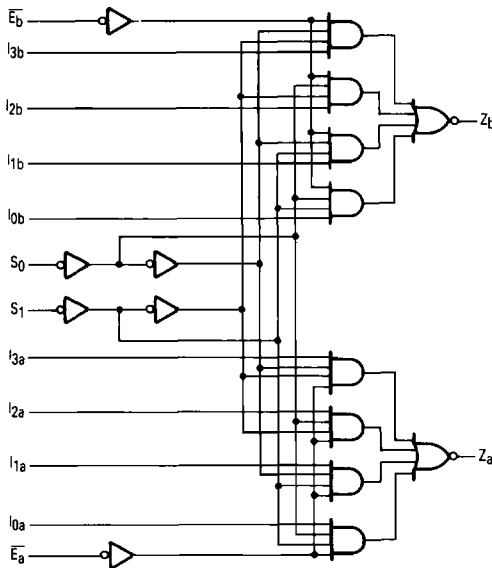
Dual 4-Input Data Selector/ Multiplexer With Inverted Outputs

**ELECTRICALLY TESTED PER:
MIL-M-38510/33909**

The 54F352 is a very high-speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'F352 is the functional equivalent of the 'F153 except with inverted outputs.

- Inverted Version of 'F153
- Separate Enable For Each Multiplexer
- Input Clamp Diode Limits High Speed Termination Effects

LOGIC DIAGRAM



Military 54F352



AVAILABLE AS:

- 1) JAN: JM38510/33909BXA
- 2) SMD: *
- 3) 883C: 54F352/BXAJC

**X = CASE OUTLINE AS FOLLOWS:
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2**

***Call Factory for latest update**

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION A)
\bar{E}_a	1	1	2	VCC
S1	2	2	3	VCC
I3a	3	3	4	VCC
I2a	4	4	5	VCC
I1a	5	5	7	VCC
I0a	6	6	8	VCC
\bar{Z}_a	7	7	9	OPEN
GND	8	8	10	GND
\bar{Z}_b	9	9	12	OPEN
I0b	10	10	13	VCC
I1b	11	11	14	VCC
I2b	12	12	15	VCC
I3b	13	13	17	VCC
S0	14	14	18	VCC
\bar{E}_b	15	15	19	VCC
VCC	16	16	20	VCC

**BURN-IN CONDITIONS:
VCC = 5.0 V MIN/6.0 V MAX**

54F352

FUNCTIONAL DESCRIPTION

The 'F352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a, \overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a, \overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a, \overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

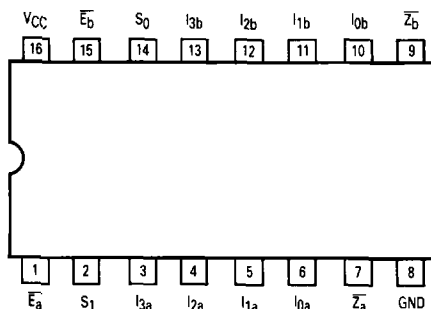
$$\overline{Z}_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

The 'F352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the select inputs. A less obvious application is as a function generator. The 'F352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

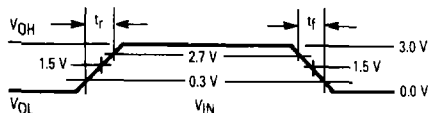
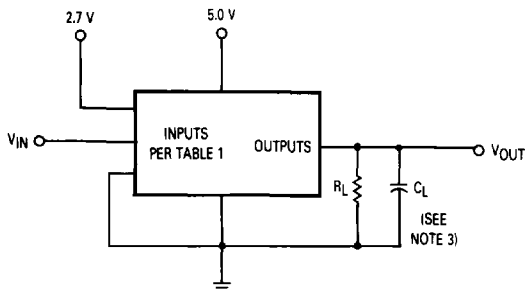
TRUTH TABLE							
Select Inputs		Inputs (a or b)				Output	
S_0	S_1	\overline{E}	I_0	I_1	I_2	I_3	\overline{Z}
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

CONNECTION DIAGRAM

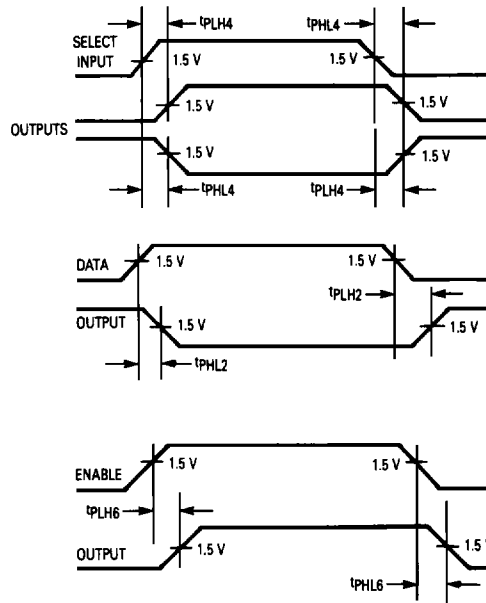


AC TEST CIRCUIT



54F352

WAVEFORMS



NOTES:

1. V_{IN} input pulse has the following characteristics:
 $t_r = t_f \leq 2.5$ ns, $PRR \leq 1.0$ MHz, $Z_{OUT} = 50 \Omega$.
2. Terminal conditions (pins not designated may be high ≥ 2.0 V, low ≤ 0.8 V, or open).
3. $C_L = 50$ pF $\pm 10\%$, including scope probe, wiring and stray capacitance without package in test fixture.
4. Voltage measurements are to be made with respect to network ground terminal.
5. $R_L = 499 \Omega \pm 5.0\%$.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 1		Subgroup 2		Subgroup 3			
	Min	Max	Min	Max	Min	Max			
V _{OH}	Logical "1" Output Voltage	2.5		2.5		2.5		V	V _{CC} = 4.5 V, I _{OH} = -1.0 mA, V _{IL} = 0.8 V, other inputs are open, E _{a/b} = 0.8 V/2.0 V, S _{1/0} = 0.8 V/2.0 V.
V _{OL}	Logical "0" Output Voltage		0.5		0.5		0.5	V	V _{CC} = 4.5 V, I _{OL} = 20 mA, V _{IH} = 2.0 V, other inputs are open, E _{a/b} = 0.8 V/open, S _{1/0} = 0.8 V/2.0 V.
V _{IC}	Input Clamping Voltage		-1.2					V	V _{CC} = 4.5 V, I _{IN} = -18 mA, other inputs are open.
I _{IH}	Logical "1" Input Current		20		20		20	μA	V _{CC} = 5.5 V, V _{IH} = 2.7 V, other inputs are open, E _{a/b} = 4.5 V or (2.7 V), S _{1/0} = 0 V, 4.5 V or (2.7 V).
I _{IHH}	Logical "1" Input Current		100		100		100	μA	V _{CC} = 5.5 V, V _{IHH} = 7.0 V, other inputs are open, E _{a/b} = 4.5 V or (7.0 V), S _{1/0} = 0.7 V, 0 V or (4.5 V).
I _{OD}	Diode Current	60		60		60		mA	V _{CC} = 4.5 V, V _{IN} = 5.5 V, other inputs are open, E _{a/b} & S _{1/0} = 0 V, V _{OUT} = 2.5 V.
I _{IL}	Logical "0" Input Current	-0.03	-0.6	-0.03	-0.6	-0.03	-0.6	mA	V _{CC} = 5.5 V, V _{IN} = 0.5 V, other inputs are open, E _{a/b} = 0 V or (0.5 V), S _{1/0} = 0 V, 4.5 V or (0.5 V).
I _{OS}	Output Short Circuit Current	-60	-150	-60	-150	-60	-150	mA	V _{CC} = 5.5 V, V _{IN} = 0 V, other inputs are open, V _{OUT} = 0 V, E _{a/b} & S _{1/0} = 0 V.
I _{CCH}	Power Supply Current Off		14		14		14	mA	V _{CC} = 5.5 V, V _{IN} = 0 V (all inputs).
I _{CCL}	Power Supply Current Off		20		20		20	mA	V _{CC} = 5.5 V, V _{IN} = 4.5 V (all inputs), E _{a/b} & S _{1/0} = 0 V.
V _{IH}	Logical "1" Input Voltage	2.0		2.0		2.0		V	V _{CC} = 4.5 V.
V _{IL}	Logical "0" Input Voltage		0.8		0.8		0.8	V	V _{CC} = 4.5 V.
	Functional Tests	Subgroup 7		Subgroup 8A		Subgroup 8B			per Truth Table with V _{CC} = 4.5 V, (Repeat at), V _{CC} = 5.5 V, V _{INL} = 0.5 V, and V _{INH} = 2.5 V.

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Symbol	Parameter	Limits						Units	Test Condition (Unless Otherwise Specified)
		+25°C		+125°C		-55°C			
		Subgroup 9		Subgroup 10		Subgroup 11			
		Min	Max	Min	Max	Min	Max		
t _{PHL2}	Propagation Delay /Data-Output I _n to Z _n	1.7	6.0	1.5	7.5	1.5	7.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLH2}	Propagation Delay /Data-Output I _n to Z _n	2.0	7.0	2.0	9.0	2.0	9.0	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PHL4}	Propagation Delay /Data-Output S _n to Z _n	3.5	13	3.5	15	3.5	15	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLH4}	Propagation Delay /Data-Output S _n to Z _n	3.5	13	3.5	14.5	3.5	14.5	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PHL6}	Propagation Delay /Data-Output E _n to Z _n	3.0	11	3.5	13	3.5	13	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.
t _{PLH6}	Propagation Delay /Data-Output E _n to Z _n	3.5	14	3.5	17	3.5	17	ns	V _{CC} = 5.0 V, C _L = 50 pF, R ₁ = R ₂ = 499 Ω.