
11 V Input 150 mA LDO

No. EA-256-180709

OUTLINE

The RP173x is a voltage regulator featuring 150 mA output and low supply current of Typ. 2.0 μ A. It consists of a voltage reference unit, an error amplifier, a resistor-net for voltage setting, a current limit circuit, a chip enable circuit and a Reverse Current Protection Circuit. RP173x is suitable for the power source such as the equipment being in the standby-mode. The A version with CE input pin has reduced CE pull-up resistance to make its supply current ultra low.

The RP173x has Max.11 V Input voltage and is applicable to the portable communication equipment that requires the 2-cell Li-ion battery. Also it is applicable to the non-portable communication equipments. As the RP173x includes Reverse Current Protection Circuit, there is little leakage current, if it is used as back-up circuit.

Packages are available in SOT-23-5, SC-88A, and 1-mm square DFN(PLP)1010-4 packages. High density mounting of the ICs on boards is possible.

FEATURES

- Output Current Typ. 150 mA
- Supply Current Typ. 2.0 μ A
- Standby Current Typ. 0.2 μ A
- Dropout Voltage Typ. 0.13 V ($I_{OUT} = 30$ mA, $V_{OUT} = 3.0$ V)
Typ. 0.90 V ($I_{OUT} = 150$ mA, $V_{OUT} = 3.0$ V)
- Output Voltage Accuracy $\pm 1.0\%$ (1.5 V < $V_{OUT} \leq 5.5$ V, $T_a = 25^\circ$ C)
- Line Regulation Typ. 0.02%/V
- Packages DFN(PLP)1010-4, SC-88A, SOT-23-5
- Input Voltage Range 2.5 V to Set $V_{OUT} + 6.5$ V (Max. 11 V)
- Output Voltage Range 1.2 V to 5.5 V (0.1 V step)
- Built-in Reverse Current Protection Circuit
- Short Current Limit Typ. 45 mA
- Built-in Peak Current Limit Circuit
- Output capacitors 0.1 μ F or more

APPLICATIONS

- Power source for portable communication equipments.
- Power source for battery-powered equipments.
- Power source for electrical appliances such as cameras, VSRs and camcorders.
- Power source for digital home appliances.

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SELECTION GUIDE

The output voltage, the auto-discharge function⁽¹⁾, and the package for the ICs are user-selectable options.

Selection Guide

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
RP173Kxx1*-TR	DFN(PLP)1010-4	10,000 pcs	Yes	Yes
RP173Qxx2*-TR-FE	SC-88A	3,000 pcs	Yes	Yes
RP173Nxx1*-TR-FE	SOT-23-5	3,000 pcs	Yes	Yes

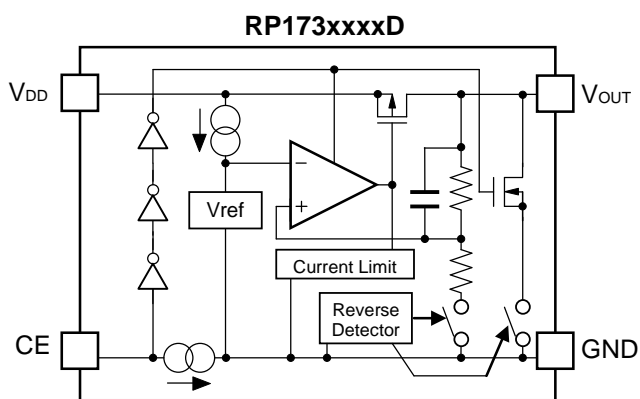
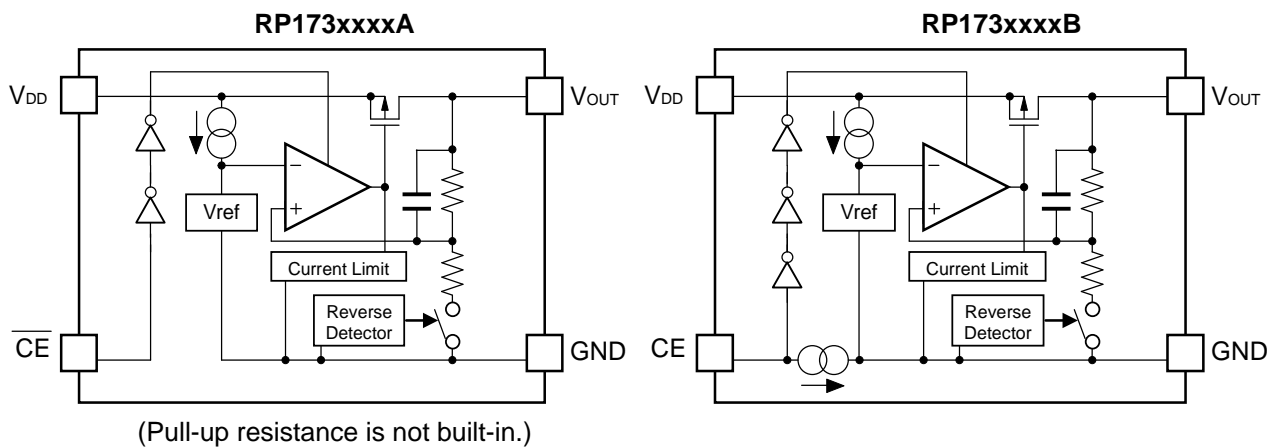
xx: The output voltage can be designated in the range of 1.2 V (12) to 5.5 V (55) in 0.1 V step.

* : The auto discharge function at off state are options as follows.

- (A) "L" active, without auto discharge function at off state (Pull-up resistance is not built-in)
- (B) "H" active, without auto discharge function at off state
- (D) "H" active, with auto discharge function at off state

⁽¹⁾ Auto-discharge function quickly lowers the output voltage to 0 V, when the chip enable signal is switched from the active mode to the standby mode, by releasing the electrical charge accumulated in the external capacitor.

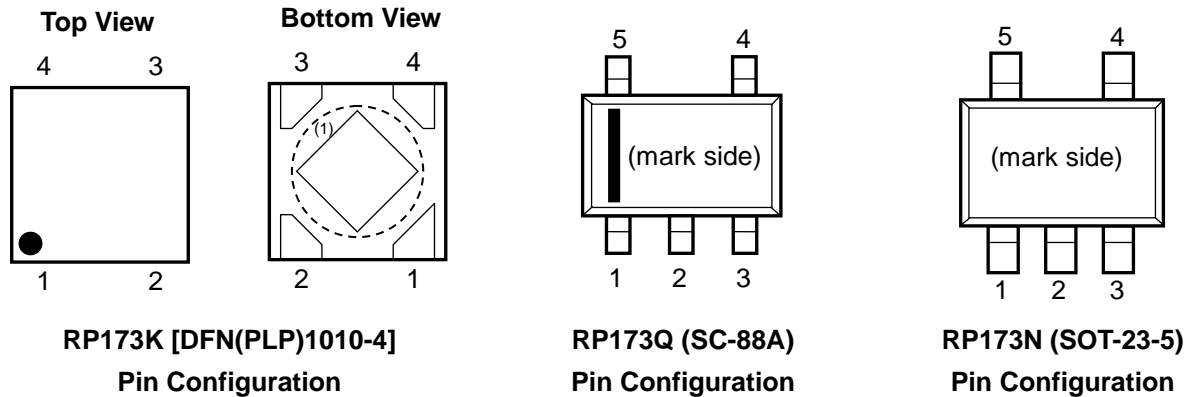
BLOCK DIAGRAMS



RP173x

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PIN DESCRIPTIONS



RP173K Pin Descriptions

Pin No.	Symbol	Description
1	V_{OUT}	Output Pin
2	GND	Ground Pin
3	\overline{CE} /CE	Chip Enable Pin
4	V_{DD}	Input Pin

RP173Q Pin Descriptions

Pin No.	Symbol	Description
1	\overline{CE} /CE	Chip Enable Pin
2 ⁽²⁾	NC	No Connection
3	GND	Ground Pin
4	V_{OUT}	Output Pin
5	V_{DD}	Input Pin

RP173N Pin Descriptions

Pin No.	Symbol	Description
1	V_{DD}	Input Pin
2	GND	Ground Pin
3	\overline{CE} /CE	Chip Enable Pin
4	NC	No Connection
5	V_{OUT}	Output Pin

⁽¹⁾ The tab on the bottom of the package enhances thermal performance and is electrically connected to GND (substrate level). It is recommended that the tab be connected to the ground plane on the board, or otherwise be left floating.

⁽²⁾ Pin No. 2 is connected to the bottom of the IC. It is recommended that the pin be connected to the ground plane on the board, or otherwise be left floating so that there is no contact with other potentials.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings

Symbol	Item		Rating	Unit	
V _{IN}	Input Voltage		12	V	
V _{CE}	Input Voltage (CE pin)		12	V	
V _{OUT}	Output Voltage		-0.3 to 6.0	V	
I _{OUT}	Output Current		165	mA	
P _D	Power Dissipation ⁽¹⁾	DFN(PLP)1010-4	JEDEC STD. 51-7 Test Land Pattern	800	mW
		SC-88A	Standard Test Land Pattern	380	
		SOT-23-5	JEDEC STD. 51-7 Test Land Pattern	660	
T _j	Junction Temperature Range		-40 to 125	°C	
T _{stg}	Storage Temperature Range		-55 to 125	°C	

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the lifetime and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS

Recommended Operating Conditions

Symbol	Item	Rating	Unit
V _{IN}	Input Voltage	2.5 to 11.0 ⁽²⁾	V
T _a	Operating Temperature Range	-40 to 85	°C

RECOMMENDED OPERATING CONDITIONS

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

⁽¹⁾ Refer to *POWER DISSIPATION* for detailed information.

⁽²⁾ V_{SET} + 6.5 V ≤ 11.0 V

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ELECTRICAL CHARACTERISTICSUnless otherwise noted, $V_{IN} = \text{Set } V_{OUT} + 1.0 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = C_{OUT} = 0.1 \mu\text{F}$.The specifications surrounded by \square are guaranteed by design engineering at $-40^\circ\text{C} \leq T_a \leq 85^\circ\text{C}$.**RP173xxxxA**

(Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	
V_{OUT}	Output Voltage	Ta = 25°C	$V_{OUT} > 1.5 \text{ V}$	x0.99		x1.01	V
			$V_{OUT} \leq 1.5 \text{ V}$	-15		15	mV
		$-40^\circ\text{C} \leq T_a \leq 85^\circ\text{C}$	$V_{OUT} > 1.5 \text{ V}$	\square x0.982		\square x1.018	V
			$V_{OUT} \leq 1.5 \text{ V}$	\square -28		\square 27	mV
I_{OUT}	Output Current		\square 150			mA	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	$0.1 \text{ mA} \leq I_{OUT} \leq 150 \text{ mA}$	\square -30	-3	\square 35	mV	
V_{DIF}	Dropout Voltage	$I_{OUT} = 150 \text{ mA}$	Refer to the <i>PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS</i>				
I_{SS}	Supply Current	$I_{OUT} = 0 \text{ mA}$		2.0	\square 3.7	μA	
$I_{standby}$	Standby Current	$V_{IN} = V_{IN} (\text{Max.})$ $V_{CE} = V_{IN}$		0.2	0.6	μA	
$\Delta V_{OUT}/\Delta V_{IN}$	Load Regulation	Set $V_{OUT} + 0.5 \text{ V} \leq V_{IN} \leq V_{IN} (\text{Max.})$ When $V_{OUT} \leq 2.0 \text{ V}$, $2.5 \text{ V} \leq V_{IN} \leq V_{IN} (\text{Max.})$		0.02	\square 0.20	%/V	
RR	Ripple Rejection	f = 1 kHz, Ripple 0.2 Vp-p, $I_{OUT} = 10 \text{ mA}$ *When $V_{OUT} < 2.0 \text{ V}$, $V_{IN} = 3.0 \text{ V}$		30		dB	
V_{IN}	Input Voltage	$1.2 \leq V_{OUT} < 4.5$	\square 2.5		\square Vset + 6.5	V	
		$4.5 \leq V_{OUT} \leq 5.5$	\square 2.5		\square 11		
I_{SC}	Short Current Limit Circuit	$V_{OUT} = 0 \text{ V}$		45		mA	
V_{CEH}	$\overline{\text{CE}}$ Input Voltage "H"		\square 1.7			V	
V_{CEL}	$\overline{\text{CE}}$ Input Voltage "L"				\square 0.8	V	
I_{REV}	Reverse Current	$0 \leq V_{IN} \leq 11.0 \text{ V}$, $V_{OUT} \geq 1.5 \text{ V}$		0	0.16	μA	
$V_{REV_DET}^{(1)}$	Reverse Current Protection Mode Detection Offset, $V_{REV} = V_{DD} - V_{OUT}$	$0 \leq V_{IN} \leq 11.0 \text{ V}$, $V_{OUT} \geq 1.5 \text{ V}$		55	\square 100	mV	
$V_{REV_REL}^{(1)}$	Reverse Current Protection Mode Release Offset	$0 \leq V_{IN} \leq 11.0 \text{ V}$, $V_{OUT} \geq 1.5 \text{ V}$		70	\square 120	mV	

All of units are tested and specified under the pulse load conditions such that $T_j \approx T_a = 25^\circ\text{C}$ except for Ripple Rejection.(1) The operation coverage of the Reverse Current Protection Circuit is $V_{OUT} \geq 1.5 \text{ V}$. However, under the condition of $V_{IN} = V_{OUT} = 0 \text{ V}$, always the Reverse Current Protection Circuit is operating.

Unless otherwise noted, $V_{IN} = \text{Set } V_{OUT} + 1.0 \text{ V}$, $I_{OUT} = 1 \text{ mA}$, $C_{IN} = C_{OUT} = 0.1 \mu\text{F}$.

 The specifications surrounded by are guaranteed by design engineering at $-40^\circ\text{C} \leq T_a \leq 85^\circ\text{C}$.

RP173xxxxB/D

(Ta = 25°C)

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit	
V_{OUT}	Output Voltage	Ta = 25°C	$V_{OUT} > 1.5 \text{ V}$	x0.99		x1.01	V
			$V_{OUT} \leq 1.5 \text{ V}$	-15		15	mV
		$-40^\circ\text{C} \leq T_a \leq 85^\circ\text{C}$	$V_{OUT} > 1.5 \text{ V}$	x0.982		x1.018	V
			$V_{OUT} \leq 1.5 \text{ V}$	-28		27	mV
I_{OUT}	Output Current		150			mA	
$\Delta V_{OUT}/\Delta I_{OUT}$	Load Regulation	$0.1 \text{ mA} \leq I_{OUT} \leq 150 \text{ mA}$	-30	-3	35	mV	
V_{DIF}	Dropout Voltage	$I_{OUT} = 150 \text{ mA}$	Refer to the <i>PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS</i>				
I_{SS}	Supply Current	$I_{OUT} = 0 \text{ mA}$		2.0	3.7	μA	
$I_{standby}$	Standby Current	$V_{IN} = V_{IN} (\text{Max.})$ $V_{CE} = 0 \text{ V}$		0.2	0.6	μA	
$\Delta V_{OUT}/\Delta V_{IN}$	Load Regulation	Set $V_{OUT} + 0.5 \text{ V} \leq V_{IN} \leq V_{IN} (\text{Max.})$ When $V_{OUT} \leq 2.0 \text{ V}$, $2.5 \text{ V} \leq V_{IN} \leq V_{IN} (\text{Max.})$		0.02	0.20	%/V	
RR	Ripple Rejection	f = 1kHz, Ripple 0.2 Vp-p, $I_{OUT} = 10 \text{ mA}$ *When $V_{OUT} < 2.0 \text{ V}$, $V_{IN} = 3.0 \text{ V}$		30		dB	
V_{IN}	Input Voltage	$1.2 \leq V_{OUT} < 4.5$	2.5		Vset + 6.5	V	
		$4.5 \leq V_{OUT} \leq 5.5$	2.5		11		
I_{SC}	Short Current Limit Circuit	$V_{OUT} = 0 \text{ V}$		45		mA	
I_{PD}	CE Pull-down Current			0.30	0.90	μA	
V_{CEH}	CE Input Voltage "H"		1.7			V	
V_{CEL}	CE Input Voltage "L"				0.8	V	
I_{REV}	Reverse Current	$0 \leq V_{IN} \leq 11.0 \text{ V}$, $V_{OUT} \geq 1.5 \text{ V}$		0	0.16	μA	
$V_{REV_DET}^{(1)}$	Reverse Current Protection Mode Detection Offset, $V_{REV} = V_{DD} - V_{OUT}$	$0 \leq V_{IN} \leq 11.0 \text{ V}$, $V_{OUT} \geq 1.5 \text{ V}$		55	100	mV	
$V_{REV_REL}^{(1)}$	Reverse Current Protection Mode Release Offset	$0 \leq V_{IN} \leq 11.0 \text{ V}$, $V_{OUT} \geq 1.5 \text{ V}$		70	120	mV	
R_{LOW}	Auto-discharge Nch Tr. ON Resistance (RP173xxxxD only)	$V_{IN} = 7.0 \text{ V}$, $V_{CE} = 0 \text{ V}$		380		Ω	

 All of units are tested and specified under the pulse load conditions such that $T_j \approx T_a = 25^\circ\text{C}$ except for Ripple Rejection.

⁽¹⁾ The operation coverage of the Reverse Current Protection Circuit is $V_{OUT} \geq 1.5 \text{ V}$. However, under the condition of $V_{IN} = V_{OUT} = 0 \text{ V}$, always the Reverse Current Protection Circuit is operating.

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PRODUCT-SPECIFIC ELECTRICAL CHARACTERISTICS**RP173x Product-specific Electrical Characteristics**

Product Name	V_{OUT}						V_{DIF}	
	$T_a = 25^{\circ}\text{C}$			$-40^{\circ}\text{C} \leq T_a \leq 85^{\circ}\text{C}$			Typ.	Max.
	Min.	Typ.	Max.	Min.	Typ.	Max.		
RP173x12xx	1.185	1.200	1.215	1.172	1.200	1.227	1.680	2.590
RP173x12xx5	1.235	1.250	1.265	1.222	1.250	1.277	1.680	2.590
RP173x13xx	1.285	1.300	1.315	1.272	1.300	1.327	1.630	2.490
RP173x14xx	1.385	1.400	1.415	1.372	1.400	1.427	1.630	2.490
RP173x15xx	1.485	1.500	1.515	1.472	1.500	1.527	1.480	2.230
RP173x16xx	1.584	1.600	1.616	1.571	1.600	1.629	1.480	2.230
RP173x17xx	1.683	1.700	1.717	1.669	1.700	1.731	1.480	2.230
RP173x17xx5	1.733	1.750	1.768	1.719	1.750	1.782	1.480	2.230
RP173x18xx	1.782	1.800	1.818	1.768	1.800	1.832	1.160	2.190
RP173x18xx5	1.832	1.850	1.869	1.817	1.850	1.883	1.160	2.190
RP173x19xx	1.881	1.900	1.919	1.866	1.900	1.934	1.160	2.190
RP173x20xx	1.980	2.000	2.020	1.964	2.000	2.036	1.160	2.190
RP173x21xx	2.079	2.100	2.121	2.062	2.100	2.138	1.160	2.190
RP173x22xx	2.178	2.200	2.222	2.160	2.200	2.240	1.160	2.190
RP173x23xx	2.277	2.300	2.323	2.259	2.300	2.341	0.900	1.470
RP173x24xx	2.376	2.400	2.424	2.357	2.400	2.443	0.900	1.470
RP173x25xx	2.475	2.500	2.525	2.455	2.500	2.545	0.900	1.470
RP173x26xx	2.574	2.600	2.626	2.553	2.600	2.647	0.900	1.470
RP173x27xx	2.673	2.700	2.727	2.651	2.700	2.749	0.900	1.470
RP173x28xx	2.772	2.800	2.828	2.750	2.800	2.850	0.900	1.470
RP173x28xx5	2.822	2.850	2.879	2.799	2.850	2.901	0.900	1.470
RP173x29xx	2.871	2.900	2.929	2.848	2.900	2.952	0.900	1.470
RP173x30xx	2.970	3.000	3.030	2.946	3.000	3.054	0.610	1.050
RP173x31xx	3.069	3.100	3.131	3.044	3.100	3.156	0.610	1.050
RP173x32xx	3.168	3.200	3.232	3.142	3.200	3.258	0.610	1.050
RP173x33xx	3.267	3.300	3.333	3.241	3.300	3.359	0.610	1.050
RP173x34xx	3.366	3.400	3.434	3.339	3.400	3.461	0.610	1.050
RP173x35xx	3.465	3.500	3.535	3.437	3.500	3.563	0.610	1.050
RP173x36xx	3.564	3.600	3.636	3.535	3.600	3.665	0.610	1.050
RP173x37xx	3.663	3.700	3.737	3.633	3.700	3.767	0.610	1.050
RP173x38xx	3.762	3.800	3.838	3.732	3.800	3.868	0.610	1.050
RP173x39xx	3.861	3.900	3.939	3.830	3.900	3.970	0.610	1.050
RP173x40xx	3.960	4.000	4.040	3.928	4.000	4.072	0.390	0.760
RP173x41xx	4.059	4.100	4.141	4.026	4.100	4.174	0.390	0.760
RP173x42xx	4.158	4.200	4.242	4.124	4.200	4.276	0.390	0.760
RP173x43xx	4.257	4.300	4.343	4.223	4.300	4.377	0.390	0.760
RP173x44xx	4.356	4.400	4.444	4.321	4.400	4.479	0.390	0.760
RP173x45xx	4.455	4.500	4.545	4.419	4.500	4.581	0.390	0.760
RP173x46xx	4.554	4.600	4.646	4.517	4.600	4.683	0.390	0.760
RP173x47xx	4.653	4.700	4.747	4.615	4.700	4.785	0.390	0.760
RP173x48xx	4.752	4.800	4.848	4.714	4.800	4.886	0.390	0.760
RP173x49xx	4.851	4.900	4.949	4.812	4.900	4.988	0.390	0.760
RP173x50xx	4.950	5.000	5.050	4.910	5.000	5.090	0.390	0.760
RP173x51xx	5.049	5.100	5.151	5.008	5.100	5.192	0.390	0.760
RP173x52xx	5.148	5.200	5.252	5.106	5.200	5.294	0.390	0.760
RP173x53xx	5.247	5.300	5.353	5.205	5.300	5.395	0.390	0.760
RP173x54xx	5.346	5.400	5.454	5.303	5.400	5.497	0.390	0.760
RP173x55xx	5.445	5.500	5.555	5.401	5.500	5.599	0.390	0.760

THEORY OF OPERATION

REVERSE CURRENT PROTECTION CIRCUIT

The RP173 Series include a Reverse Current Protection Circuit, which stops the reverse current from V_{OUT} pin to V_{DD} pin or to GND pin when V_{OUT} becomes higher than V_{IN} .

Usually, the LDO using Pch output transistor contains a parasitic diode between V_{DD} pin and V_{OUT} pin. Therefore, if V_{OUT} is higher than V_{IN} , the parasitic diode becomes forward direction. As a result, the current flows from V_{OUT} pin to V_{DD} pin.

The ICs of this series switches the mode to the reverse current protection mode before V_{IN} becomes lower than V_{OUT} by connecting the parasitic diode of Pch output transistor to the backward direction, and connecting the gate to V_{OUT} pin. As a result, the Pch output transistor is turned off and the all the current pathways from V_{OUT} pin to GND pin are shut down to maintain the reverse current lower than $[I_{REV}]$ of the Electrical Characteristics.

Switching to either the normal mode or to the reverse current protection mode is determined by the magnitude of V_{IN} voltage and V_{OUT} voltage. For the stable operation, offset and hysteresis are set as the threshold. The detection/ release thresholds of both normal and reverse current protection modes are specified by $[V_{REV_DET}]$ and $[V_{REV_REL}]$ of the Electrical Characteristics. Therefore, the minimum dropout voltage under the small load current condition is restricted by the value of $[V_{REV_REL}]$.

Fig.1 and Fig.2 show the diagrams of each mode, and Fig.3 shows the load characteristics of each mode. When giving the V_{OUT} pin a constant-voltage and decreasing the V_{IN} voltage, the dropout voltage will become lower than the $[V_{REV_DET}]$. As a result, the reverse current protection starts to function to stop the load current. By increasing the dropout voltage higher than the $[V_{REV_REL}]$, the protection mode will be released to let the load current to flow. If the dropout voltage to be used is lower than $[V_{REV_REL}]$, the detection and the release may be repeated.

The operation coverage of the Reverse Current Protection Circuit is $V_{OUT} \geq 1.5V$. However, under the condition of $V_{IN}=0V$, always the reverse current protection mode is operating.

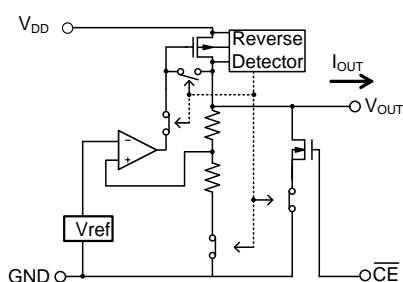


Fig. 1 Normal Mode

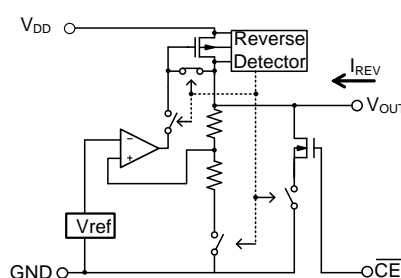


Fig. 2 Reverse Current Protection Mode

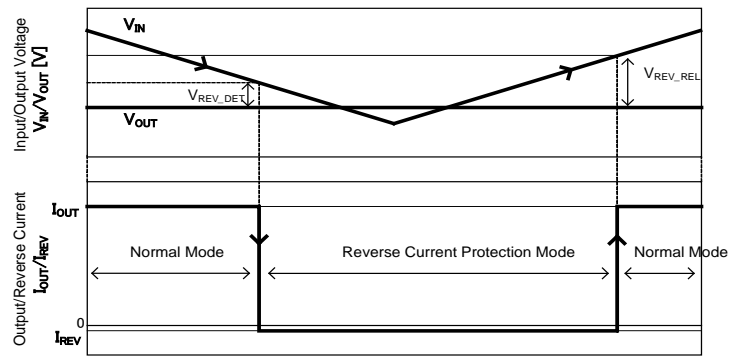
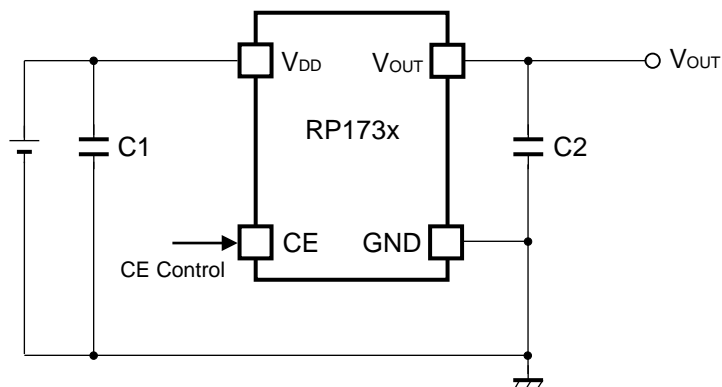


Fig. 3 Reverse Current Protection Mode Detection/ Release & Reverse Current/ Output Current Characteristics

APPLICATION INFORMATION

TYPICAL APPLICATIONS



Recommended External Components

Symbol	Description
C2 (C _{OUT})	0.1 μF, GRM155B31C104KA87D, MURATA

NOTES ON SELECTING EXTERNAL COMPONENTS

Phase Compensation

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, use a 0.1 μF or more capacitor C2.

In case of using a tantalum capacitor, the output may be unstable due to inappropriate ESR. Therefore, the full range of operating conditions for the capacitor in the application should be considered.

PCB Layout

Make V_{DD} and GND lines sufficient. If their impedance is high, noise pickup or unstable operation may result. Connect a capacitor C1 with a capacitance value as much as 0.1 μF or more between V_{DD} and GND pin, and as close as possible to the pins.

Set external components, especially the output capacitor C2, as close as possible to the ICs, and make wiring as short as possible.

TECHNICAL NOTES

POWER ACTIVATION

If the ICs are started up with V_{IN} and V_{CE} under the no-load condition, the both pin voltages have to be started up with faster than 2.0V/s. If the IC is started up with slower than 2.0V/s under the no-load condition, start up the IC only with V_{CE} .

ESR vs. Output Current

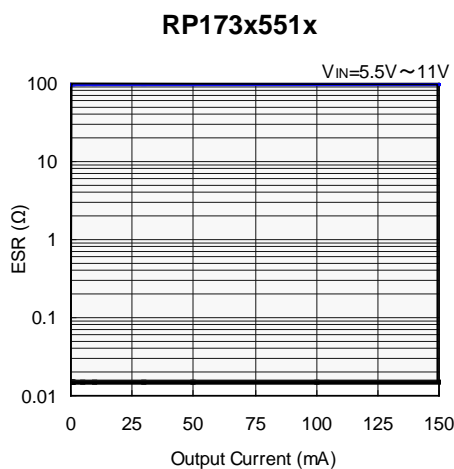
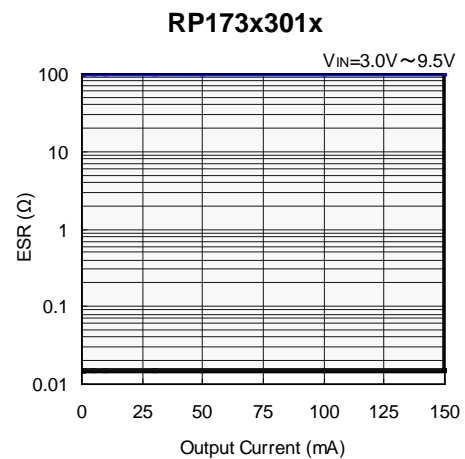
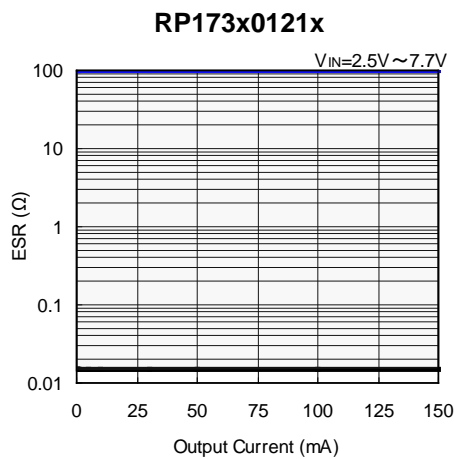
When using these ICs, consider the following points: The relations between I_{OUT} (Output Current) and ESR of an output capacitor are shown below. The conditions when the white noise level is under 40 μ V (Avg.) are marked as the hatched area in the graph.

Measurement Conditions

Frequency Band: 10 Hz to 2 MHz

Temperature : -40°C to 85°C

C1, C2 : 0.1 μ F

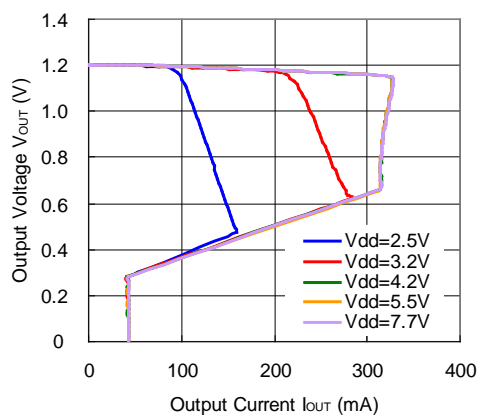


TYPICAL CHARACTERISTICS

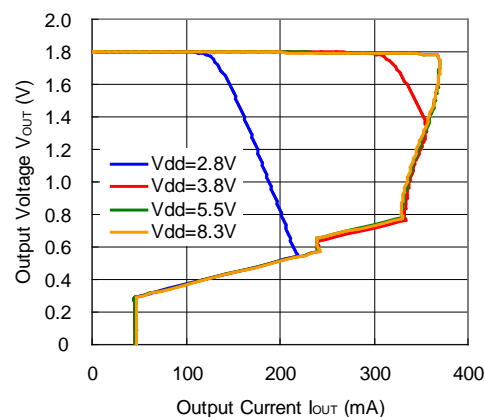
Note: Typical Characteristics are intended to be used as reference data; they are not guaranteed.

1) Output Voltage vs. Output Current (C1 = Ceramic 0.1 μ F, C2 = Ceramic 0.1 μ F, Ta = 25°C)

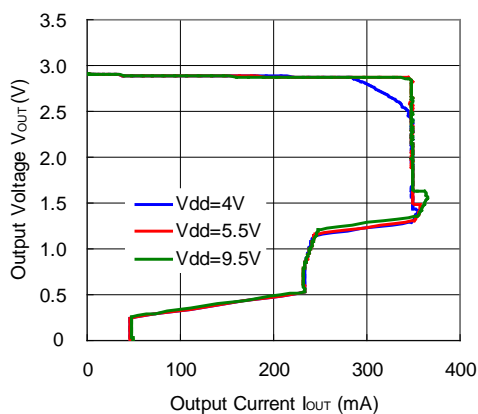
RP173x12xx



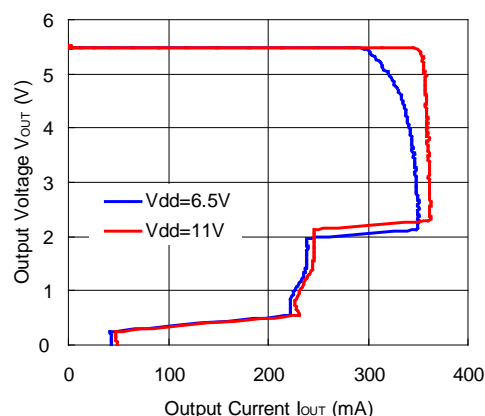
RP173x18xx



RP173x30xx

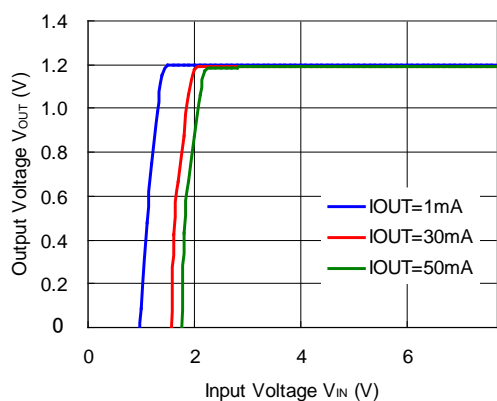


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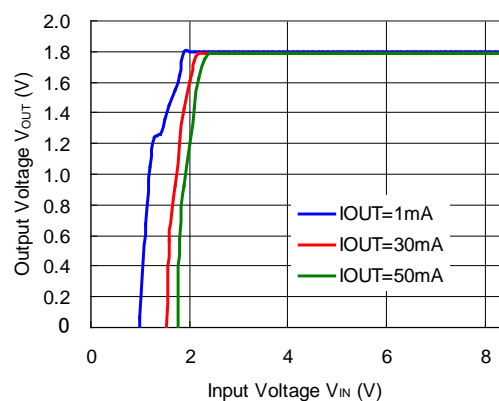


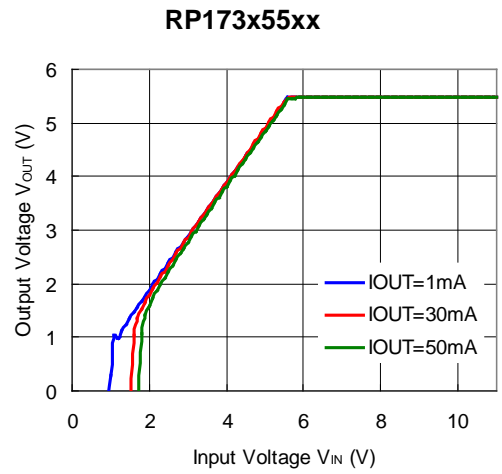
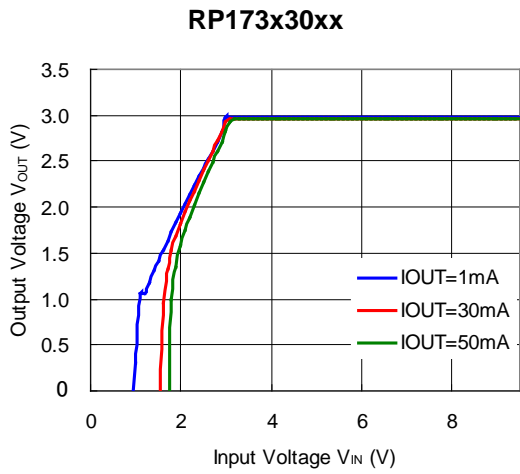
2) Output Voltage vs. Input Voltage (C1 = Ceramic 0.1 μ F, C2 = Ceramic 0.1 μ F, Ta = 25°C)

RP173x12xx

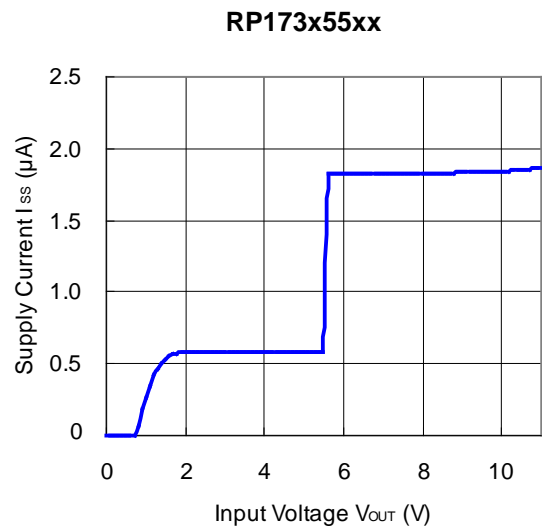
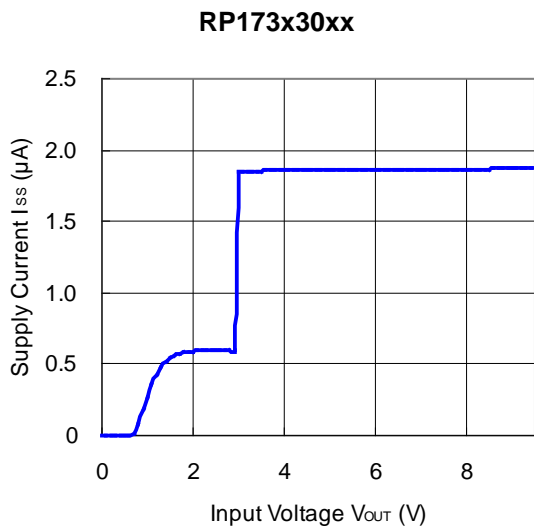
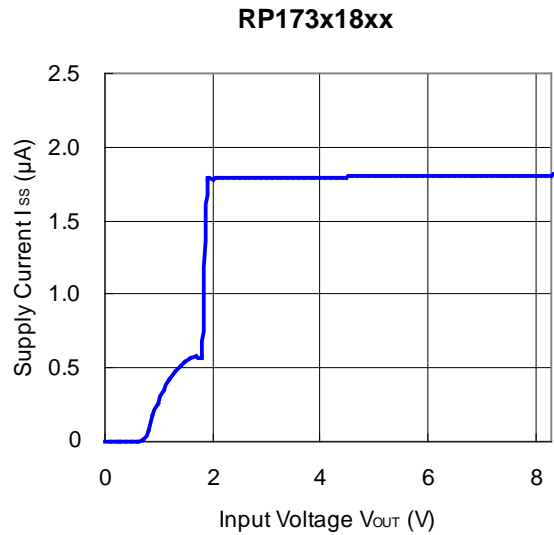
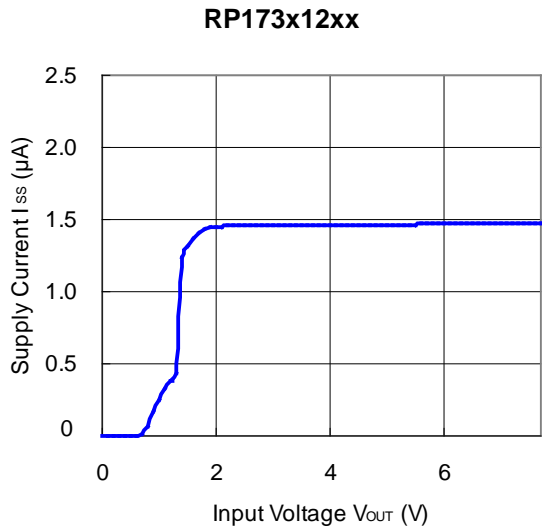


RP173x18xx



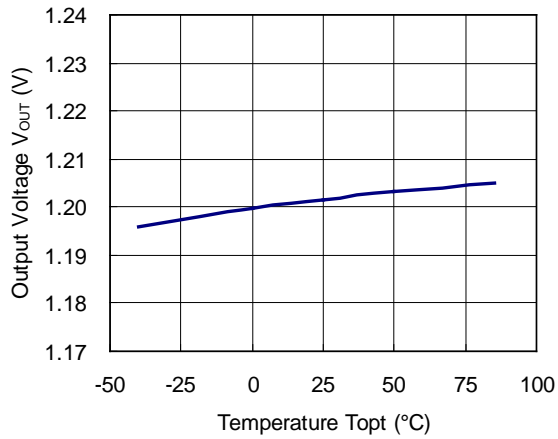


3) Supply Current vs. Input Voltage (C1 = Ceramic 0.1 μ F, C2 = Ceramic 0.1 μ F, Ta = 25°C)

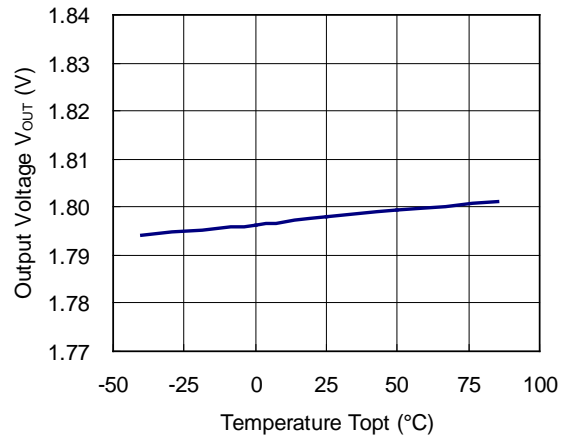


4) Output Voltage vs. Temperature (C1 = Ceramic 0.1 μ F, C2 = Ceramic 0.1 μ F, $I_{OUT} = 1$ mA)

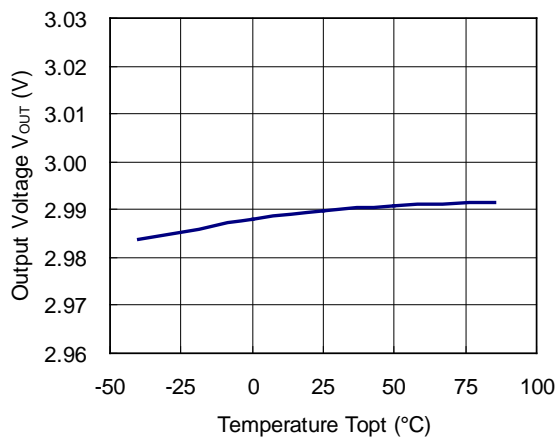
RP173x12xx



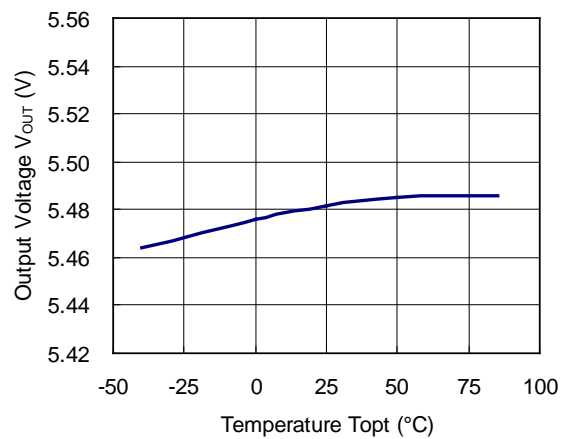
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RP173x30xx

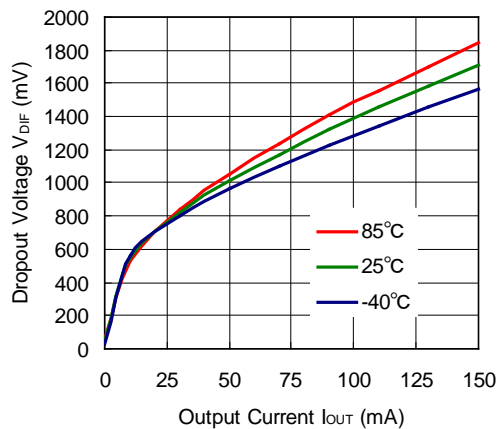


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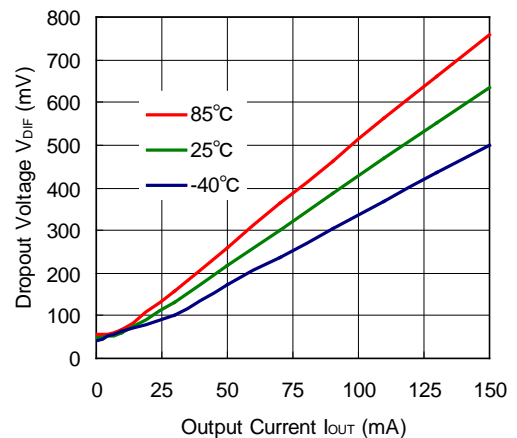


5) Dropout Voltage vs. Output Current (C1 = Ceramic 0.1 μ F, C2 = Ceramic 0.1 μ F)

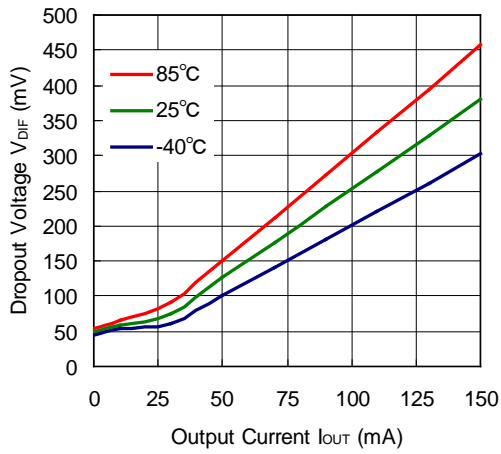
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RP173x30xx

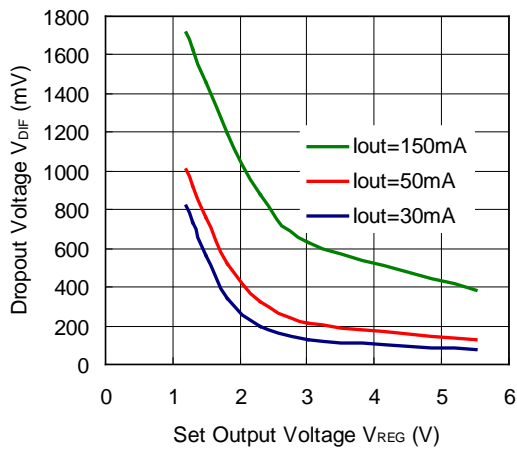


RP173x55xx

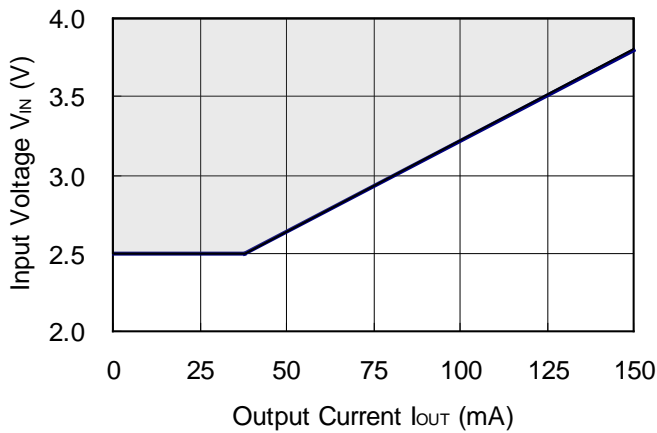


6) Dropout Voltage vs. Set Output Voltage (C1 = Ceramic 0.1 μ F, C2 = Ceramic 0.1 μ F, Ta = 25°C)

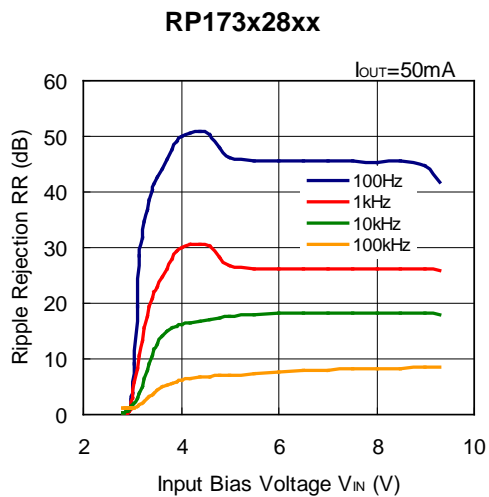
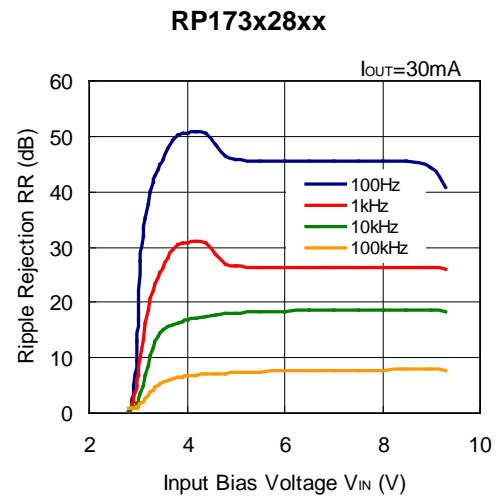
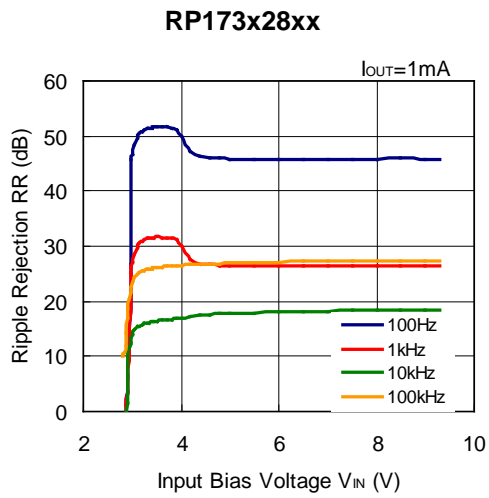
RP173x



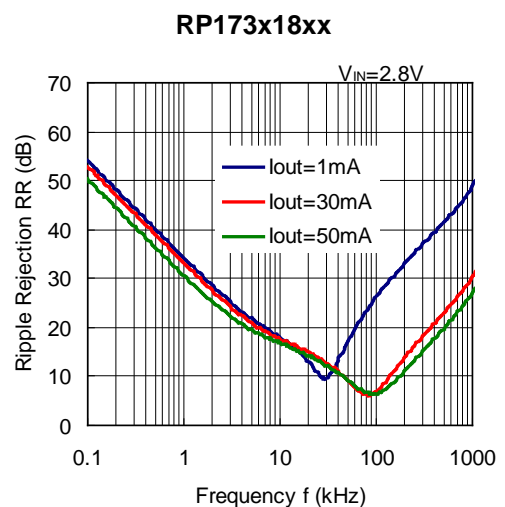
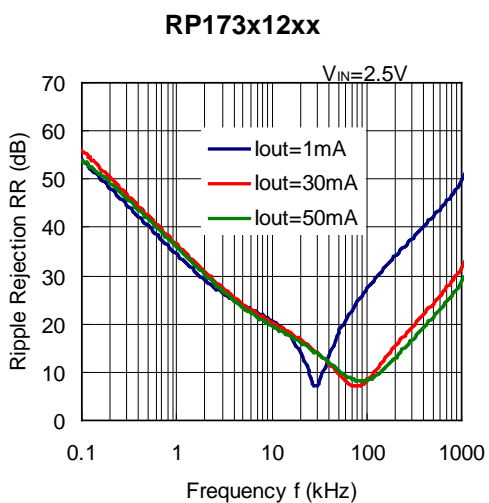
7) Minimum Operating Voltage (C1 = Ceramic 0.1 μ F, C2 = Ceramic 0.1 μ F, Ta = -40 to 85°C)



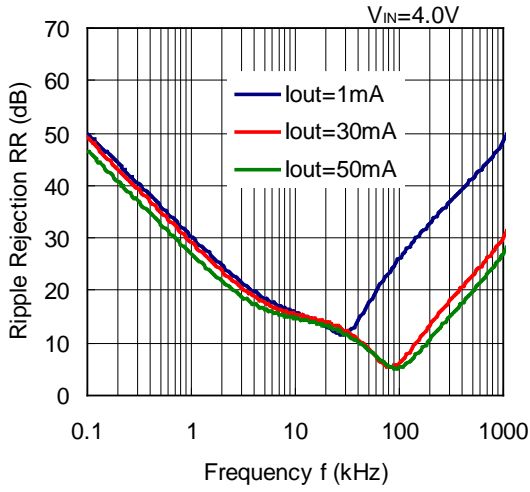
8) Ripple Rejection vs. Input Bias Voltage (C1 = none, C2 = Ceramic 0.1 μ F, Ripple = 0.2 Vp-p, Ta = 25°C)



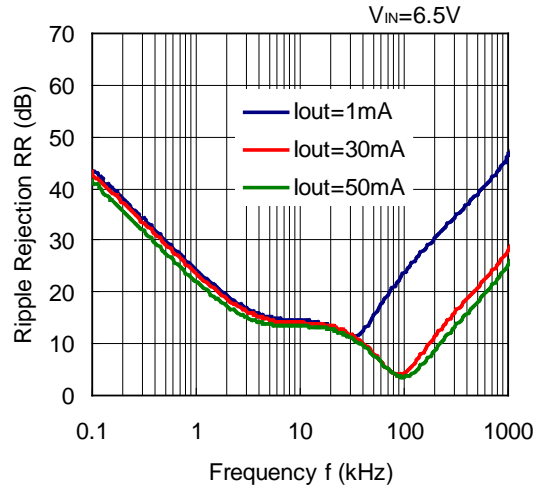
9) Ripple Rejection vs. Temperature (C1 = none, C2 = Ceramic 0.1 μ F, Ripple = 0.2 Vp-p, Ta = 25°C)



RP173x30xx

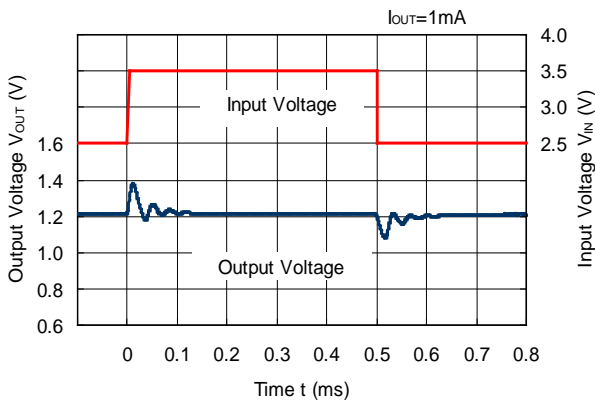


RP173x55xx

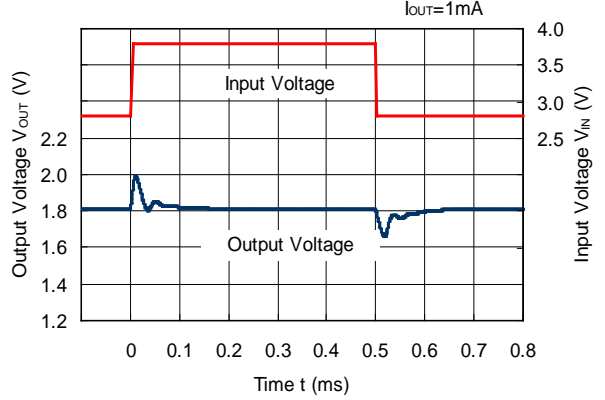


10) Input Transient Response (C1 = none, C2 = Ceramic 0.1 μF , $t_r = t_f = 5.0 \mu s$, $T_a = 25^\circ C$)

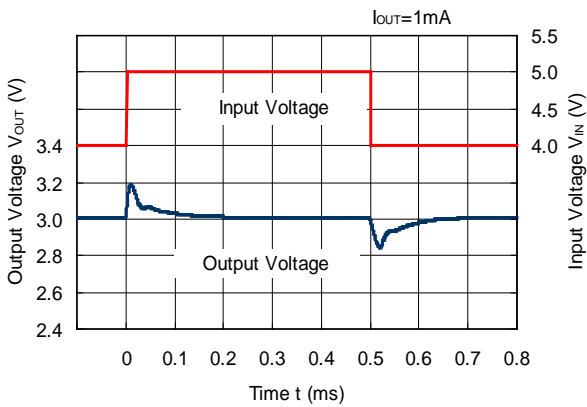
RP173x12xx



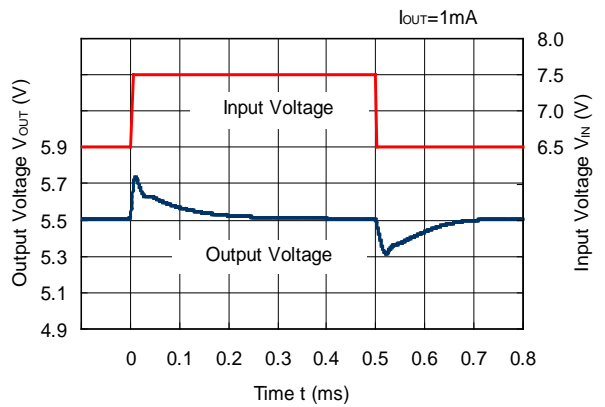
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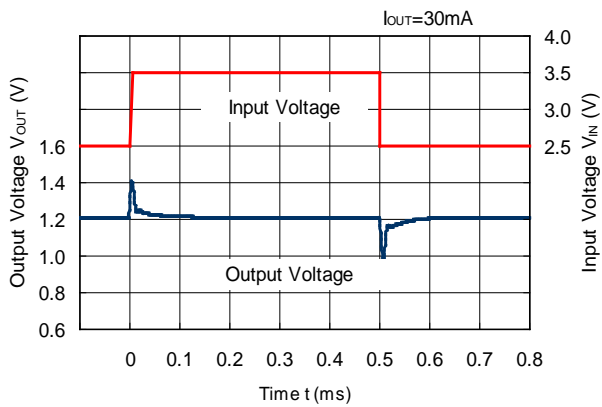
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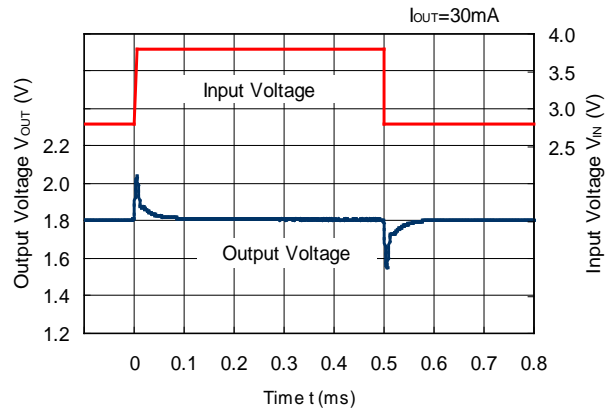
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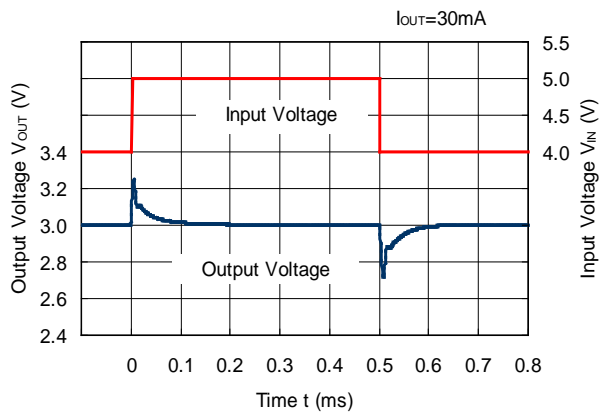
RP173x12xx



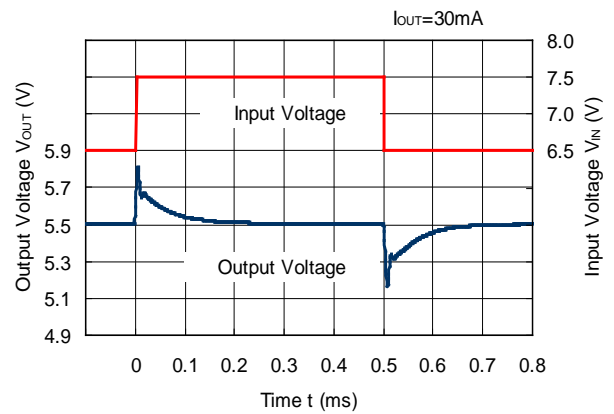
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RP173x30xx

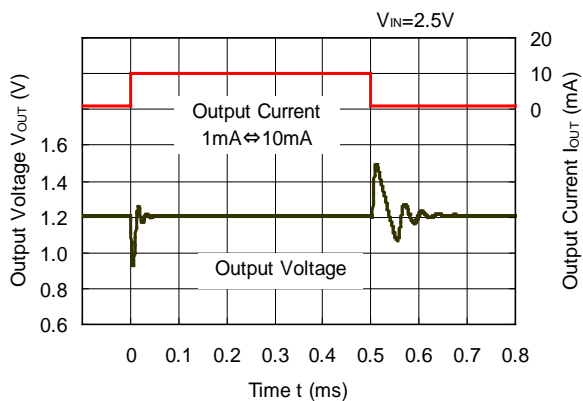


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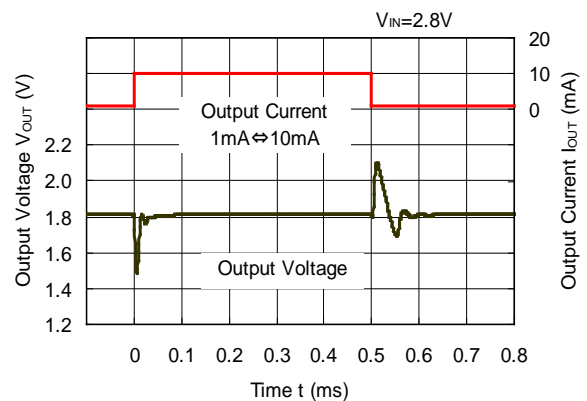


11) Load Transient Response (C1 = Ceramic 0.1 μF , C2 = Ceramic 0.1 μF , $t_r = t_f = 0.5 \mu s$, $T_a = 25^\circ C$)

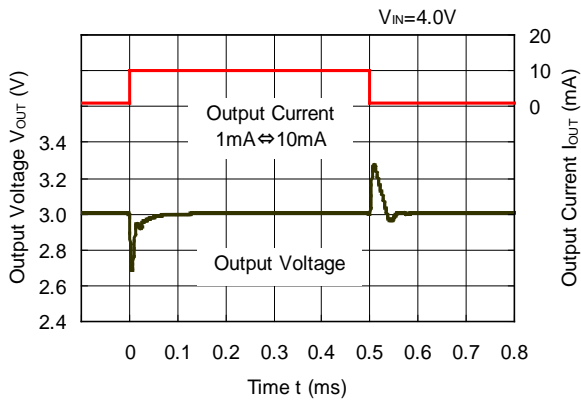
RP173x12xx



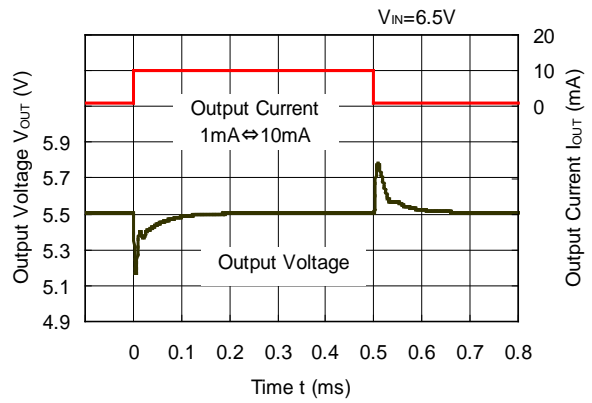
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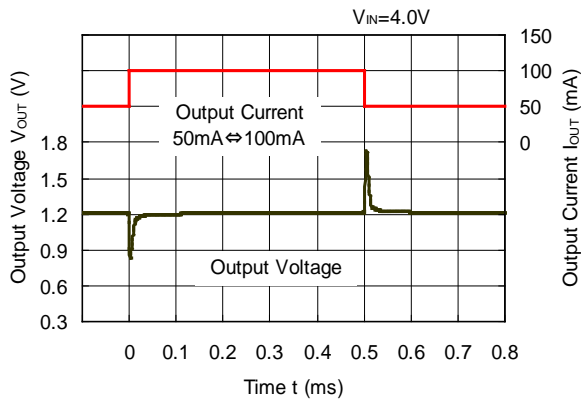
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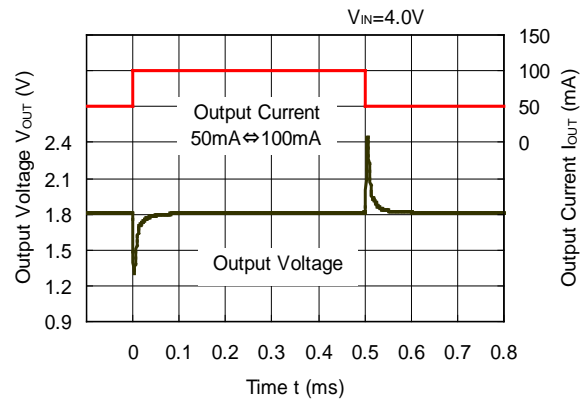
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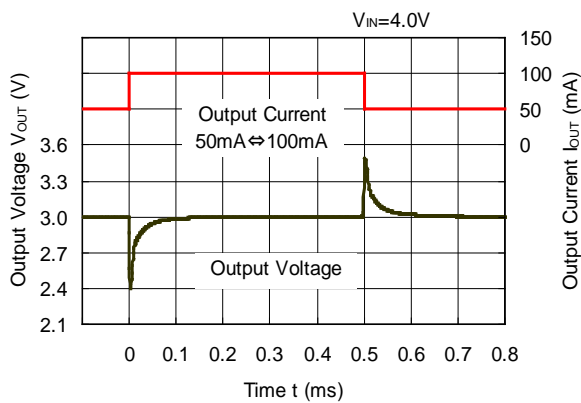
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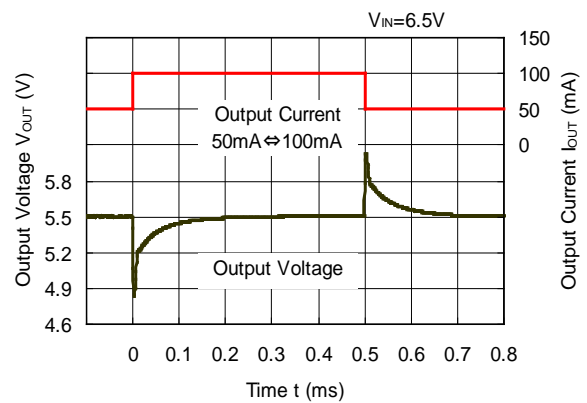
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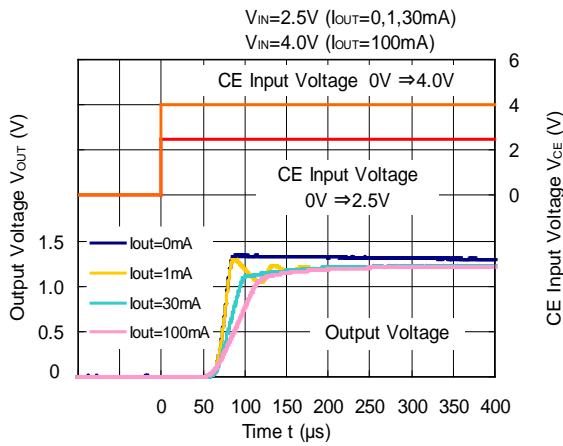


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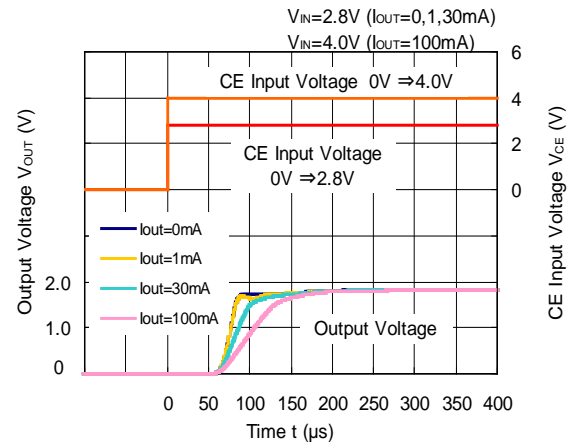


12) Turn on Speed (C1 = Ceramic 0.1 μ F, C2 = Ceramic 0.1 μ F, Ta = 25°C)

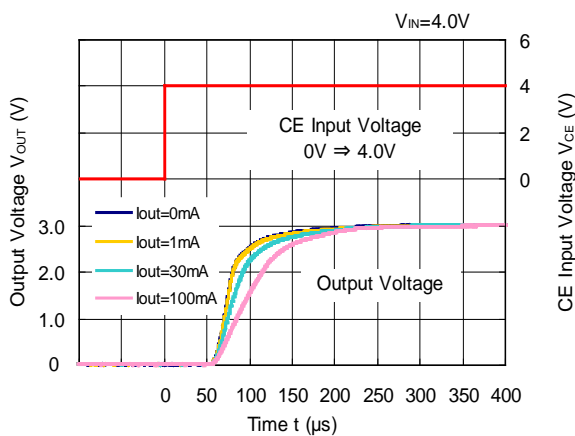
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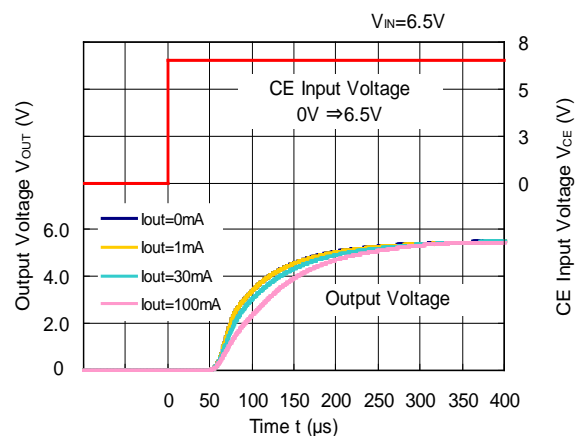
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RP173x30xx

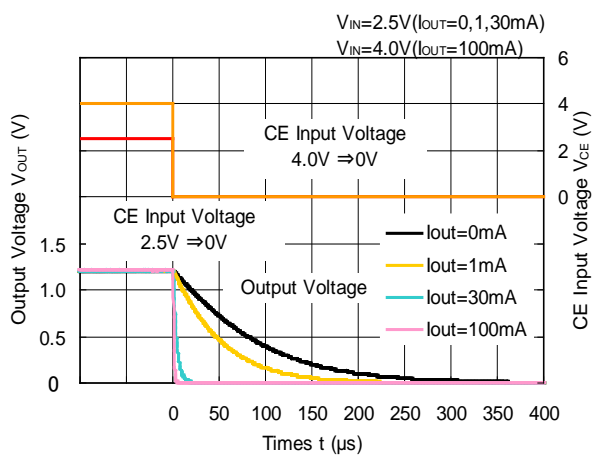


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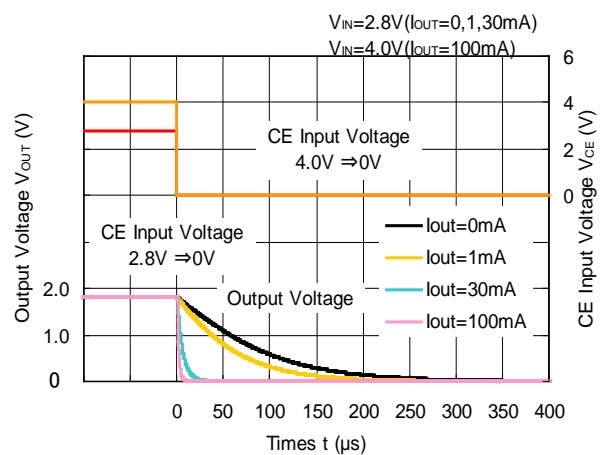


13) Turn off Speed with CE pin (C1 = Ceramic 0.1 μ F, C2 = Ceramic 0.1 μ F, Ta = 25°C)

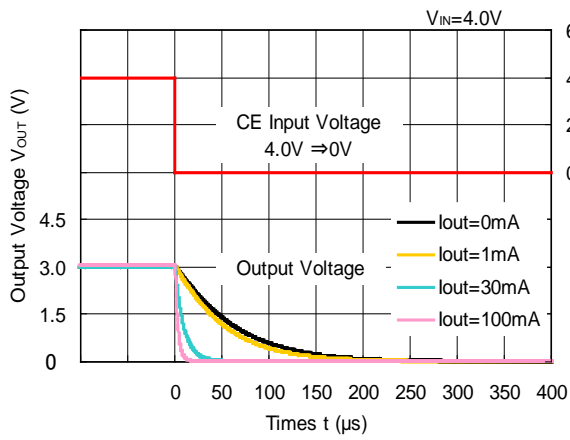
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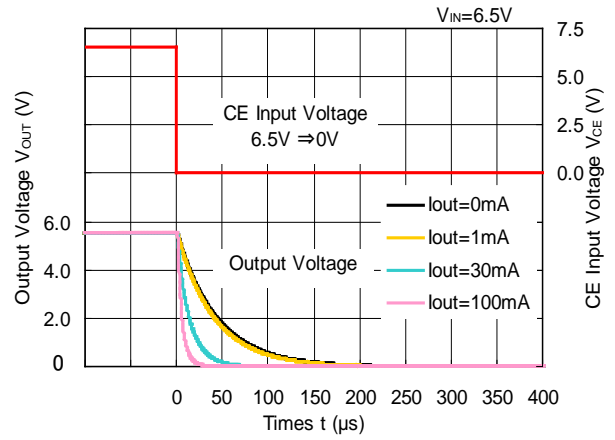
RP173x18xx



RP173x30xx



RP173x55xx



The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.2 mm × 11 pcs

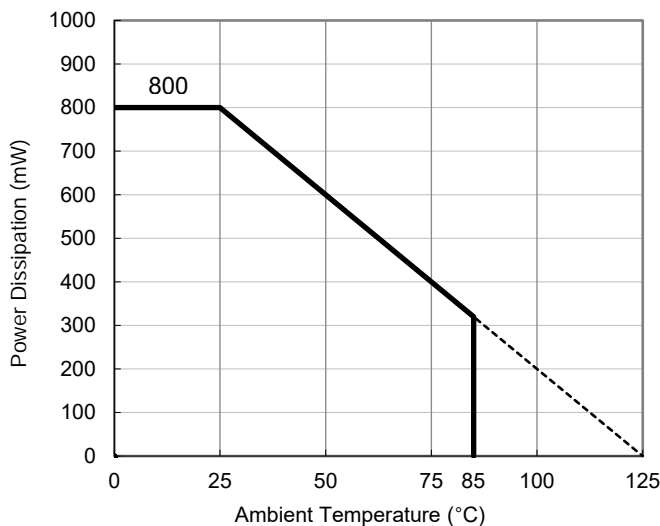
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

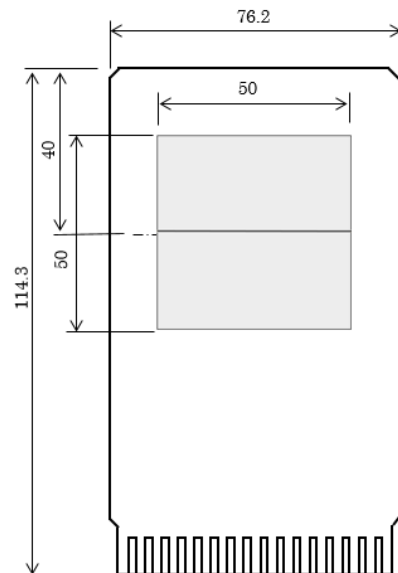
Item	Measurement Result
Power Dissipation	800 mW
Thermal Resistance (θja)	θja = 125°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 58°C/W

θja: Junction-to-Ambient Thermal Resistance

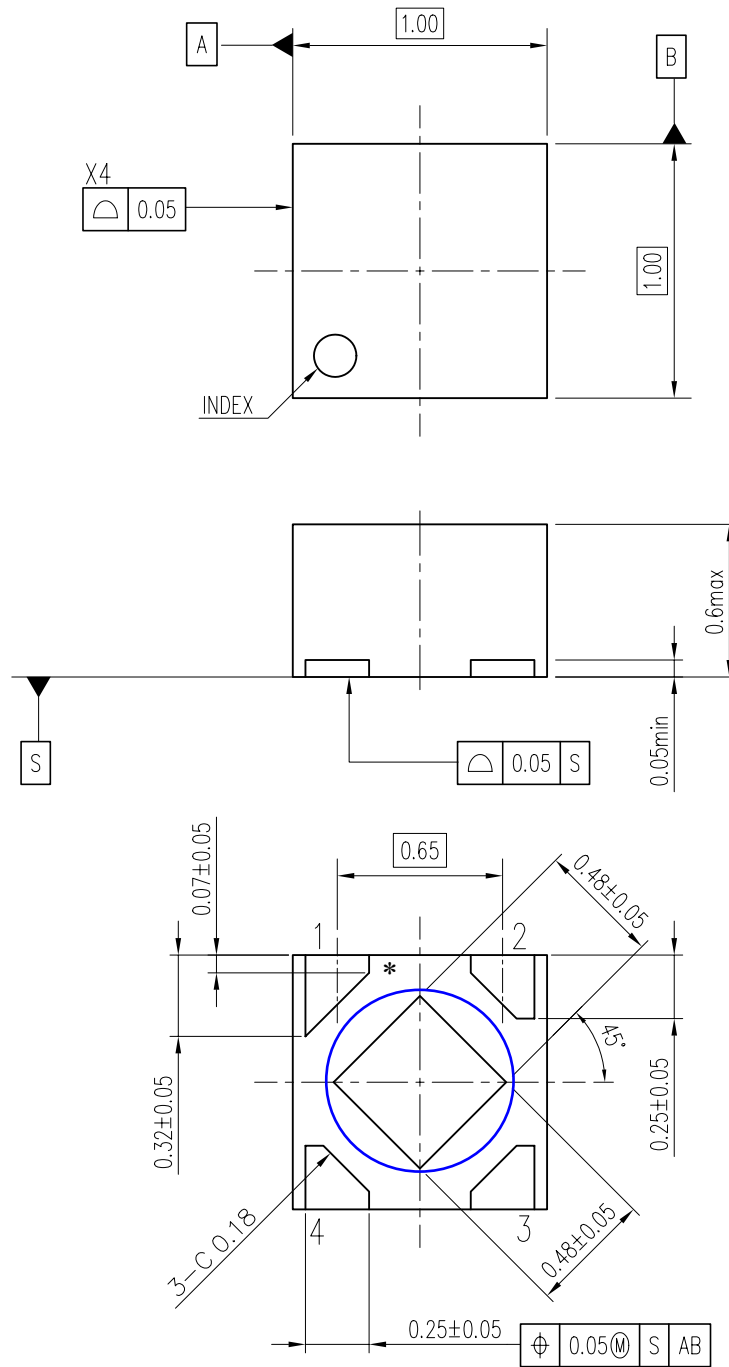
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



DFN(PLP)1010-4 Package Dimensions (Unit: mm)

* The tab on the bottom of the package shown by blue circle is a substrate potential (GND). It is recommended that this tab be connected to the ground plane on the board but it is possible to leave the tab floating.

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following conditions are used in this measurement.

Measurement Conditions

Item	Standard Test Land Pattern
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Double-Sided Board)
Board Dimensions	40 mm × 40 mm × 1.6 mm
Copper Ratio	Top Side: Approx. 50% Bottom Side: Approx. 50%
Through-holes	φ 0.5 mm × 44 pcs

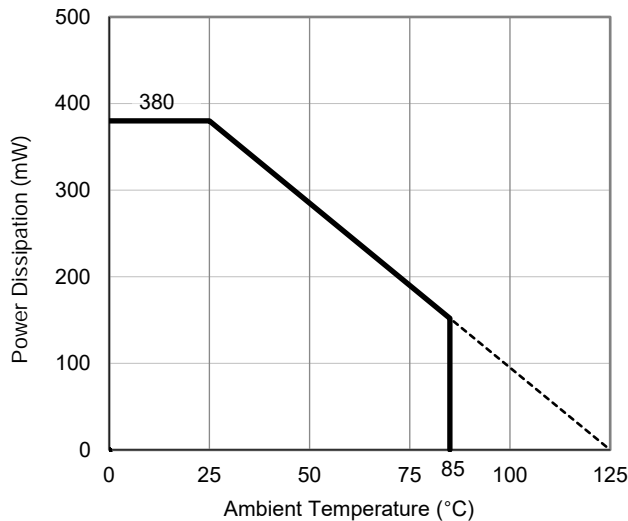
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

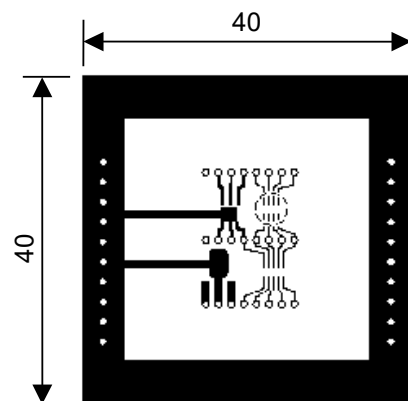
Item	Standard Test Land Pattern
Power Dissipation	380 mW
Thermal Resistance (θja)	θja = 263°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 75°C/W

θja: Junction-to-Ambient Thermal Resistance

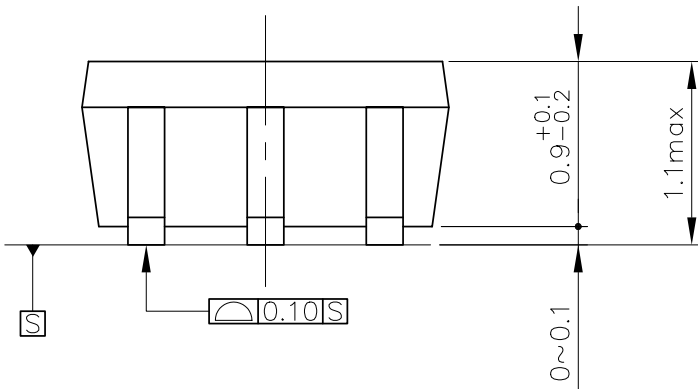
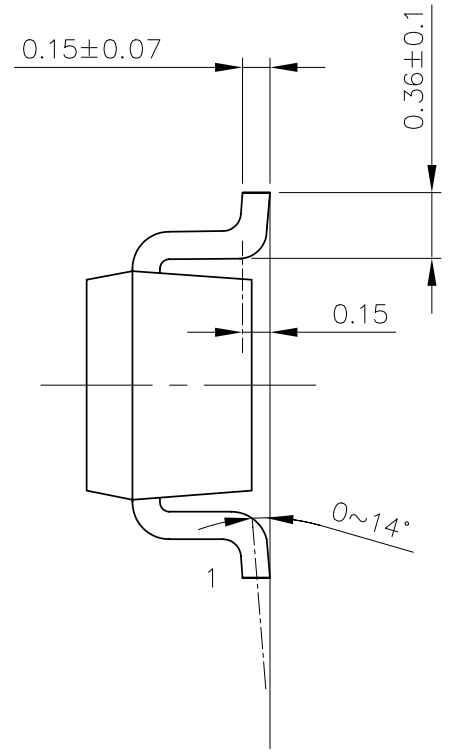
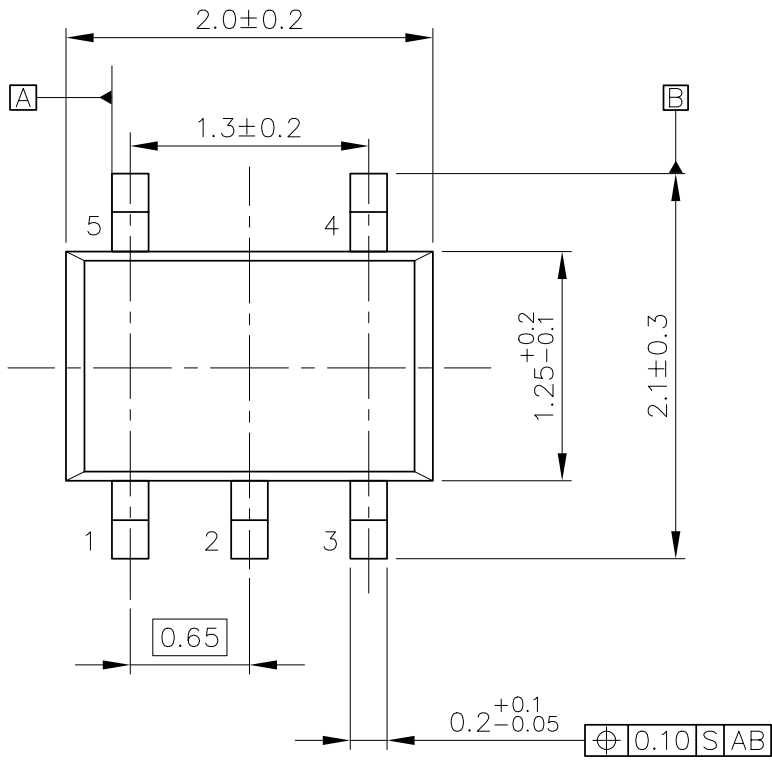
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



UNIT: mm

SC-88A Package Dimensions

The power dissipation of the package is dependent on PCB material, layout, and environmental conditions. The following measurement conditions are based on JEDEC STD. 51-7.

Measurement Conditions

Item	Measurement Conditions
Environment	Mounting on Board (Wind Velocity = 0 m/s)
Board Material	Glass Cloth Epoxy Plastic (Four-Layer Board)
Board Dimensions	76.2 mm × 114.3 mm × 0.8 mm
Copper Ratio	Outer Layer (First Layer): Less than 95% of 50 mm Square Inner Layers (Second and Third Layers): Approx. 100% of 50 mm Square Outer Layer (Fourth Layer): Approx. 100% of 50 mm Square
Through-holes	φ 0.3 mm × 7 pcs

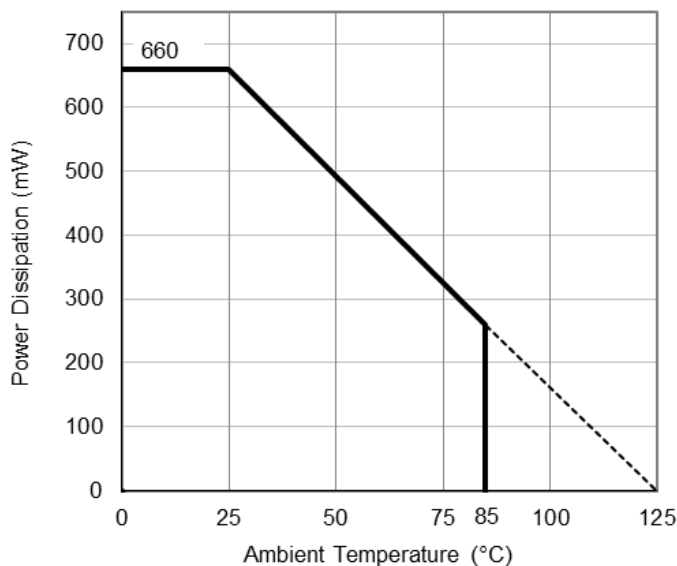
Measurement Result

(Ta = 25°C, Tjmax = 125°C)

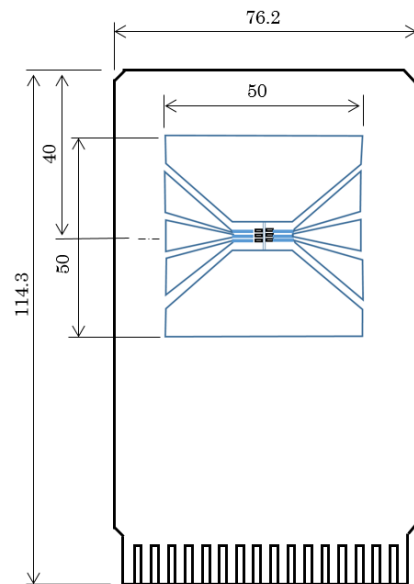
Item	Measurement Result
Power Dissipation	660 mW
Thermal Resistance (θja)	θja = 150°C/W
Thermal Characterization Parameter (ψjt)	ψjt = 51°C/W

θja: Junction-to-Ambient Thermal Resistance

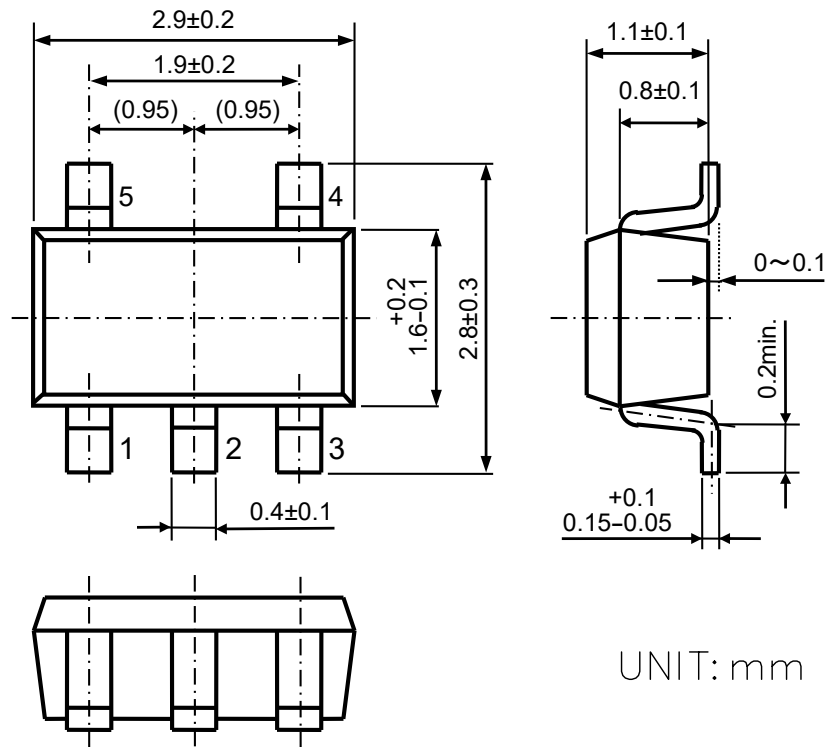
ψjt: Junction-to-Top Thermal Characterization Parameter



Power Dissipation vs. Ambient Temperature



Measurement Board Pattern



SOT-23-5 Package Dimensions



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