

Am8127

AmZ8000 Clock Generator

DISTINCTIVE CHARACTERISTICS

- High-drive high-level clock output**
 Special output provides clock signal matched to requirements of AmZ8000* CPU (4MHz and some 6MHz applications), MMU and DMA devices.
- Synchronized WAIT state and time-out controls**
 On-chip logic generates WAIT signal under control of Halt, Single-step, Status and Ready signals. Automatic time-out of peripheral wait requests.
- Four TTL-level clocks**
 Generates synchronized TTL compatible clocks at 16MHz, 2MHz and 1MHz to drive memory circuits and LSI peripheral devices. An additional TTL clock is synchronized with the CPU high-level clock for registers, latches and other peripherals.

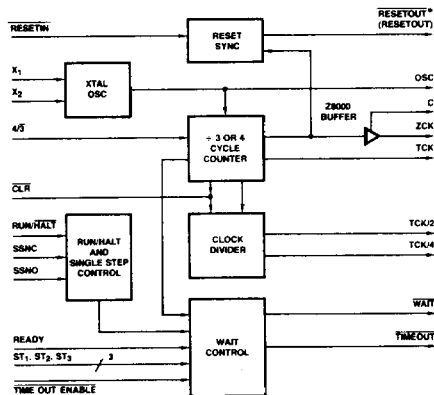
GENERAL DESCRIPTION

The Am8127 Clock Generator and Controller provides the clock oscillator, frequency dividers and clock drivers for the complete array of AmZ8000 CPUs, peripherals and memory system configurations. In addition to the special 4MHz output driver for the AmZ8001* and AmZ8002* CPUs, a standard buffered TTL 16MHz oscillator output is provided for a dynamic memory timing and control. In addition to 4MHz applications, the Am8127 will also function in some 6MHz Z8000 applications. The Am8127 forms an integral part of the dynamic memory support chip set including the Am8163 EDC and Refresh Controller, Am2964 Dynamic Memory Controller, Am2960 Error Detection and Correction Unit and Am2961/Am2962 EDC Bus Buffers. The oscillator is designed to operate with a 16MHz crystal or with external 16MHz drive. The Am8127 uses an internal divide-by-4 to provide 4MHz clock drive to the AmZ8001/AmZ8002 CPU. Additional dividers generate synchronous buffered 4, 2 and 1MHz clock outputs for use by peripheral devices. The clock divider counters are clearable to allow synchronization of the multiple clock outputs.

The controller functions include RESET, RUN/HALT, SINGLE-STEP, READY and a READY TIMEOUT counter which limits a peripheral's wait request to 16 clock cycles. The CPU's WAIT input is controlled by RUN/HALT, Single-Step, Status and READY. When RUN/HALT is LOW the Am8127 drives the WAIT output LOW causing the CPU to add wait states (TW). The READY input is used by peripherals to request wait states. The active LOW input timeout enable, TOEN, is used to force TIME-OUT LOW and WAIT HIGH 16 clock cycles after a peripheral has requested a wait but fails to release the request. The CPU status lines ST₁, ST₂ and ST₃ are decoded in the Am8127 to disable the TIMEOUT counter during CPU "Internal Operations" and during refresh.

The 4/3 input controls the clock duty cycle. An internal pull-up resistor pulls this input high for AmZ8000 CPUs. A LOW input causes the cycle counter to output a 33% duty cycle.

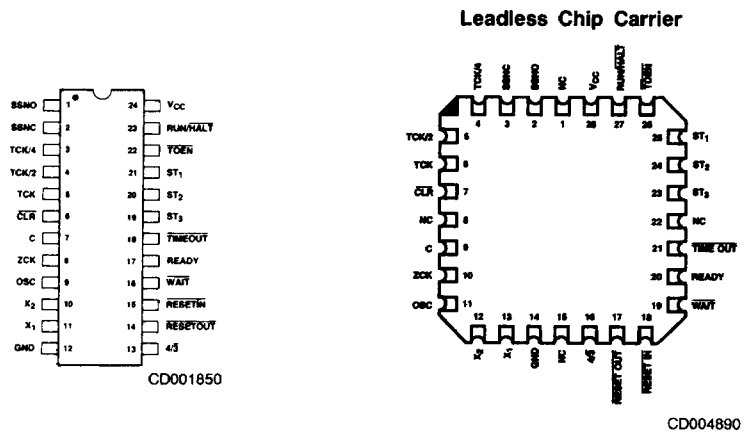
BLOCK DIAGRAM CLOCK GENERATOR



BD001370

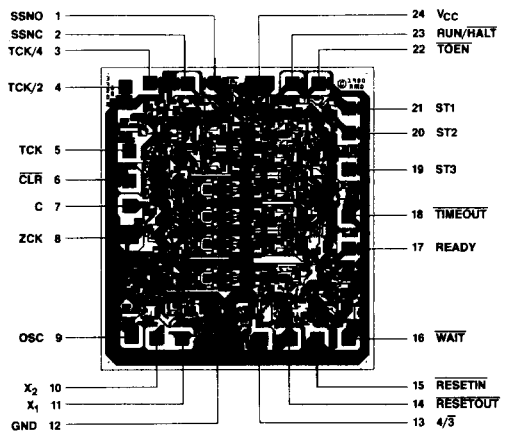
*RESETOUT is active LOW when 4/3 = HIGH

CONNECTION DIAGRAM Top View



24 Pin 0.3" wide
Pin 1 is marked for orientation

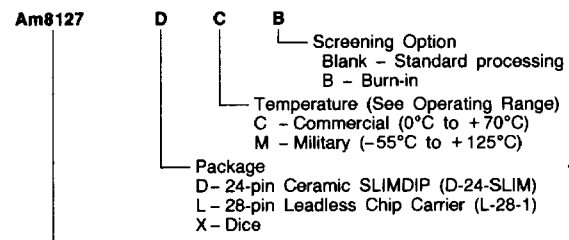
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.098" x 0.088"

ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).




Device type
AmZ8000 Clock Generator

Valid Combinations	
Am8127	DC, DCB, DM, DMB, LC, LCB, LM, LMB, XC, XM

Valid Combinations
Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

PIN DESCRIPTION




Pin No.	Name	I/O	Description
8	ZCK	O	Buffered clock output for CPU and peripherals. This output has under/overshoot control and provides the high level output voltage required ($V_{CC} - 0.4V$). This output is capable of driving multiple CPU clock inputs (or DMA, MMU, etc).
7	C	I	Bootstrap input. The capacitor C_B is connected from the ZCK clock output to C to provide faster ZCK risetime.
5	TCK	O	TTL level buffered clock output. TCK is the same frequency as ZCK and is synchronized with ZCK. TCK is in phase with ZCK when the 4/3 duty cycle control input is HIGH (50% duty cycle) and out of phase with ZCK when 4/3 is LOW (33% ZCK duty cycle).
3, 4	TCK/2, TCK/4	O	TTL buffered clocks for peripherals. TCK/2 and TCK/4 are 1/2 and 1/4 the TCK frequency and are synchronized with the rising edge of TCK.
9	OSC	O	The clock oscillator TTL buffered output. This output provides a high speed clock for dynamic memory timing (e.g. AmZ8000 uses this output to generate RAS/MUX-Select/CAS timing for dynamic RAMs) or other system application. The ZCK and TCK outputs are synchronized to the OSC rising edge.
13	4/3	I	Clock duty cycle control for ZCK and TCK. A HIGH input (no connection - input has internal pull-up) will result in a 50% duty cycle for AmZ8000 application. A LOW input will cause a 33% duty cycle ZCK output.
6	CLR	I	The clear active LOW input for internal counters. A LOW input meeting set-up and hold time requirements will clear the internal clock counters on the rising edge of OSC.
16	WAIT	O	The WAIT output for connection to the CPU WAIT input. This latched output controls when the CPU enters wait states in response to the READY, ST ₁ , ST ₂ , ST ₃ , RUN/HALT and Single Step inputs.
17	READY	I	The active HIGH READY input is used by peripherals to request wait states. Ready inputs must meet the wait latch set-up and hold time requirements.
18	TIMEOUT	O	The Timeout Counter active LOW output. The Timeout Counter counts ZCK/TCK clock cycles and is used to force WAIT HIGH 15 clock cycles after a peripheral has requested a wait but has failed to release the request. This output is normally used to interrupt the CPU.
22	TOEN	I	The Timeout Enable active LOW input. A LOW input allows the Timeout Counter to count, causes the TIMEOUT output to go LOW for one ZCK/TCK clock period after 15 cycles and forces WAIT HIGH at the rising edge of the 16th cycle. A HIGH input disables the counter and allows WAIT to be controlled by the READY, RUN/HALT and Single Step inputs.
14	RESET- OUT (RESET- OUT)	O	The Reset Output to the CPU. It is active LOW when the 4/3 input is HIGH and active HIGH when the 4/3 input is LOW.
15	RESETIN	I	The active LOW Reset Input. A LOW input will cause RESETOUT to go LOW synchronous with ZCK  . Pushbutton reset is implemented by momentarily grounding RESETIN. Power-up reset is implemented by connecting a capacitor from RESETIN to ground. Capacitor values from 10µF to 22µF will provide a power-up of less than one second.
23	RUN/ HALT	I	A debounced input to allow halt and Single Step control modes. A HIGH input allows the CPU to run. A LOW input forces the WAIT output LOW causing the CPU to enter continuous wait states until the ZCK period after RUN/HALT is returned to HIGH.
1	SSNO, SSNC	I	Single Step control inputs. These debounced input allow the CPU to Single Step from one wait state to the next by momentarily disconnecting SSNC from ground and grounding SSNO. RUN/HALT must be LOW for Single Step operation.
19, 20, 21	ST ₁ , ST ₂ , ST ₃	I	Status inputs from AmZ8000 CPU's and peripherals. Continuous LOW inputs indicate that the CPU is executing "internal operation" or "refresh." During this time the time out is disabled to avoid signaling an inappropriate interrupt. The status inputs are subject to the set-up and hold time requirements of the WAIT latch.
10, 11	X ₁ , X ₂	I	External crystal connections (see application section). X ₁ may be driven directly by a TTL input.

*RESETOUT is active LOW when 4/3 = HIGH.

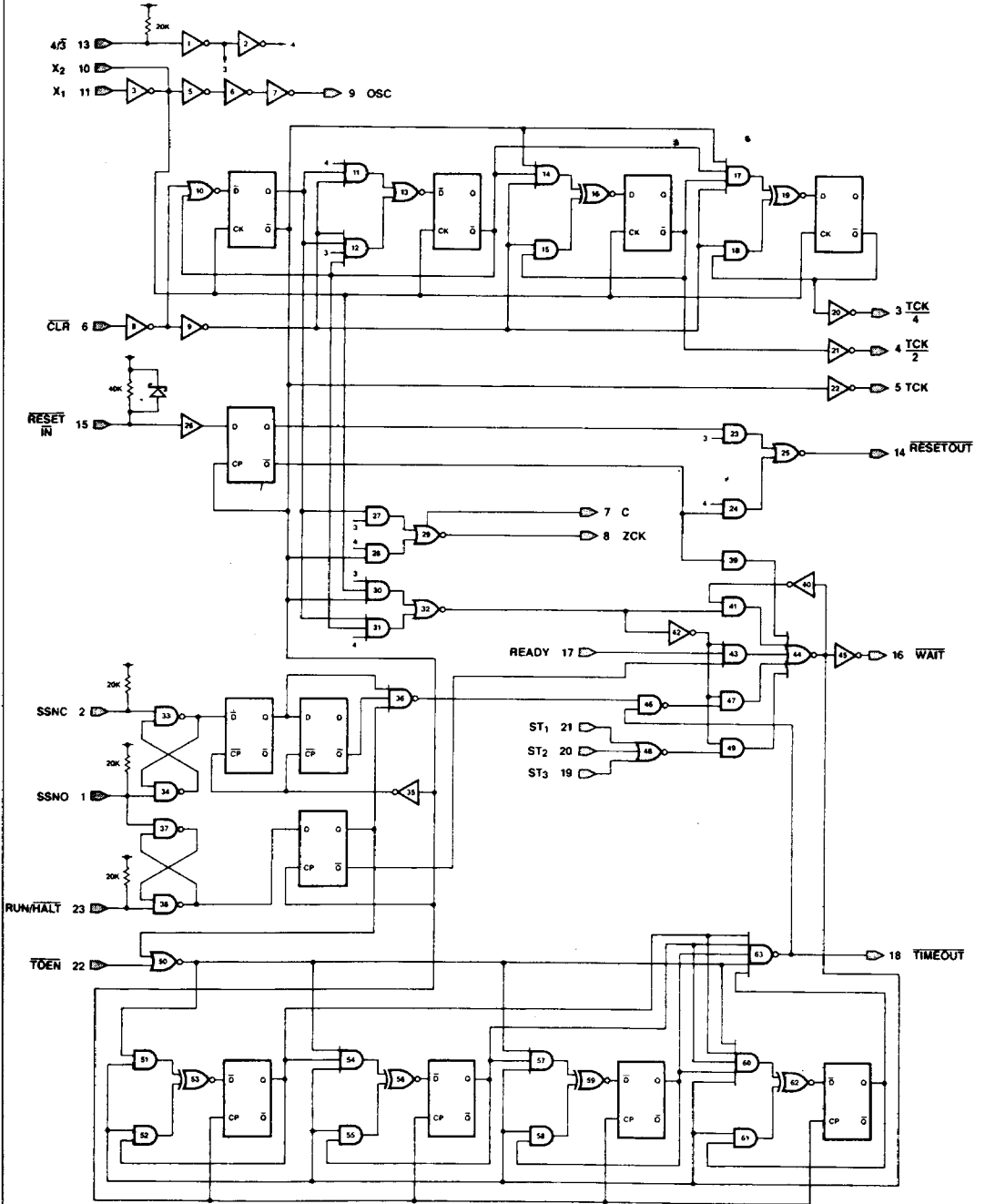
TYPICAL CRYSTAL SPEC

Mode	Fundamental AT cut
Resonance	Parallel or Series
Load	32pF (Net of 56pF C's shown + stray C)
Stability	±0.01% (or to user requirement)

WAIT, TIMEOUT FUNCTION TABLE

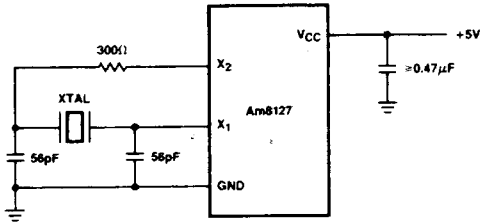
RUN/HALT	SSNC	ST ₃	ST ₂	ST ₁	READY	TOEN	TIMEOUT COUNTER	TIMEOUT	WAIT
H	X	L	L	L	H	X	Cleared	H	H
		L	L	L	L	X	Cleared	H	H
		Any ST _i = H	H	L	L	H	H	H	H
			L	H	L	H	H	H	L
L	L	X	X	X	X	X	Count + 1 on ZCK 	H until 16 clocks after ready  , then LOW one ZCK period	L until 16 clocks after ready  , then HIGH one ZCK period
	H						L	H	L

BLOCK DIAGRAM



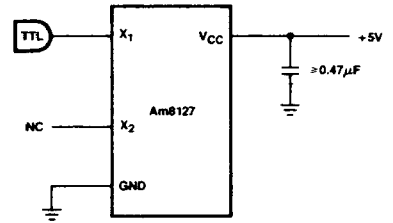
BD001560

CRYSTAL CONTROLLED OSCILLATOR



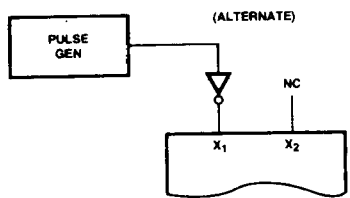
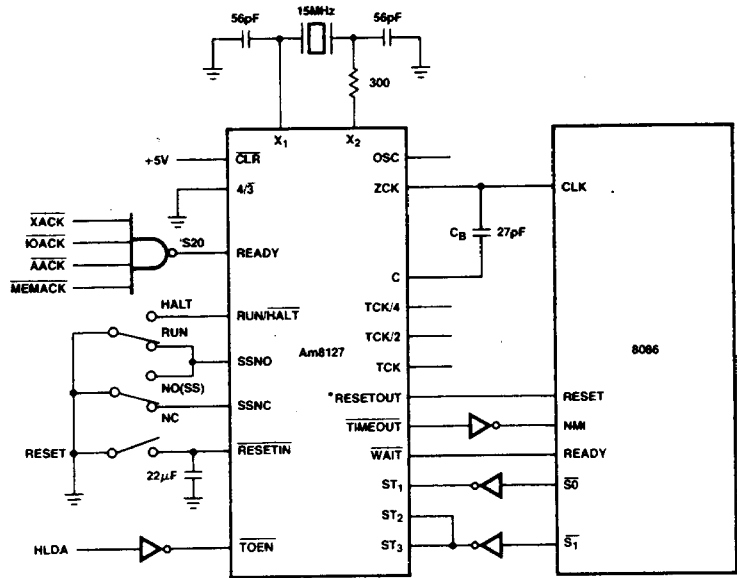
DF000380

EXTERNAL CLOCK DRIVE



DF000370

AmZ8000 APPLICATION
(50% Duty Cycle ZCK)



*RESETOUT is active LOW when 4/3 = HIGH

DF000350

The typical operating configuration for Am8127 is shown above. The component values shown provide a 4MHz clock output for the AmZ8002 CPU. The 27pF capacitor from C to ZCK is a bootstrap to ensure clock rise to $V_{CC} - 0.4V$ within

the specified rise time. The $22\mu F$ reset capacitor is chosen to guarantee reset, plus adequate delay for reset during power-up with a slowly rising V_{CC} supply voltage. Ground SSNO if RUN/HALT or S-S isn't used.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential (Pin 24 to Pin 12) Continuous	-0.5V to +7.0V
DC Voltage Applied to Outputs For High Output State	-0.5V to +V _{CC} max
DC Input Voltage X ₁ , 4/3, SSNO, SSNC, RUN/ HALT	-0.5V to V _{CC} + 0.5V
Other Inputs	-0.5V to +5.5V
DC Voltage Applied to C	-0.5V to +8V
DC Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices Temperature	0°C to +70°C
Supply Voltage	+4.75V to +5.25V
Military (M) Devices Temperature	-55°C to +125°C
Supply Voltage	+4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Parameter	Description		Test Conditions (Note 1)	Min	Typ (Note 2)	Max	Units	
V _{OH}	Output HIGH Voltage	V _{CC} = MIN	ZCK	I _{OH} = -0.1mA	V _{CC} -0.4	V _{CC} -0.1	Volts	
			TTL Outputs	MIL	I _{OH} = -1mA	2.4	3.4	Volts
				COM'L	I _{OH} = -2.6mA			
V _{OL}	Output LOW Voltage	V _{CC} = MIN	I _{OL} = 0.1mA, ZCK Output			0.4	Volts	
			I _{OL} = 16mA, TTL Output			0.5	Volts	
V _{IH}	Input HIGH Level	Guaranteed input HIGH Voltage	RESETIN	2.8	2.25		Volts	
			ST ₁ , ST ₂ , ST ₃ , CLR, TOEN, X ₁ , READY	2.0			Volts	
V _{IL}	Input LOW Level	Guaranteed input LOW Voltage	ST ₁ , ST ₂ , ST ₃ , CLR, TOEN, X ₁ , READY			0.8	Volts	
V _I	Input Clamp Voltage	V _{CC} = MIN, I _{IN} = -18mA (Note 3)				-1.5	Volts	
V _{IN} -V _{IL}	RESETIN Hysteresis	V _{CC} = MIN		400	650		mV	
I _{IL}	Input LOW Current	V _{CC} = MAX, V _{IN} = 0.4V	SSNO			-1.6	mA	
			SSNC, 4/3, RUN/HALT, READY			-1.2	mA	
			TOEN, CLR, X ₁			-0.72	mA	
			RESETIN, ST ₁ , ST ₂ , ST ₃			-0.36	mA	
I _{IH}	Input HIGH Current	V _{CC} = MAX, V _{IN} = 2.7V	4/3, SSNC, SSNO RUN/HALT		(Note 4)	-300	μA	
			RESETIN		(Note 4)	-200	μA	
			CLR, READY, TOEN			+50	μA	
			ST ₁ , ST ₂ , ST ₃			+600	μA	
I _I	Input HIGH Current	V _{CC} = MAX, V _{IN} = 5.5V	CLR, READY, TOEN ST ₁ , ST ₂ , ST ₃			+1.0	mA	
I _{SC}	Output Short Circuit Current (Note 5)	V _{CC} = MAX	ZCK Output	-50		-240	mA	
			Others	-40		-130	mA	
I _{CC}	Power Supply Current	V _{CC} = MAX	X ₁ = 2.4V, ZCK = TCK's = LOW		95	140	mA	
			Operating, I _{OSC} ≤ 24MHz (Note 6)		120	180		

- Notes: 1. For conditions shown as MIN or MAX, use the appropriate value specified under Operating Range for the applicable device type.
 2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
 3. Not applicable to X₁.
 4. Specification is negative because of internal input pull-up resistors.
 5. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
 6. For oscillator frequencies up to 24MHz, outputs open.

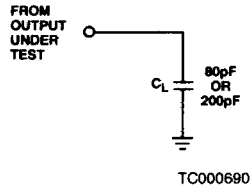
STATIC INPUT ELECTRICAL CHARACTERISTICS

The static control inputs, SSNO, SSNC (Single Step), RUN/ $\overline{\text{HALT}}$ and $4/\overline{3}$ (clock duty cycle control), are Low-Power Schottky TTI compatible inputs with internal pull-up resistors

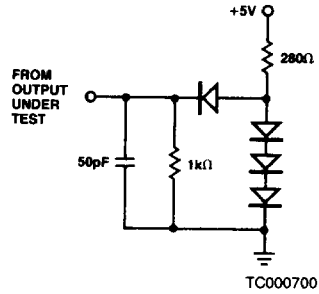
to the +5V supply. They may be left open for a HIGH input (e.g., $4/\overline{3}$ is left open for operation with AmZ8001/8002), or grounded for a LOW input. SSNO, SSNC and RUN/ $\overline{\text{HALT}}$ are intended to be grounded or opened by switches. $4/\overline{3}$ is normally left open for AmZ8001/8002. These inputs are specified at 0.4V/2.4V for test convenience.

Parameter	Description	Test Conditions		Min	Typ	Max	Units
V _{IH}	Input HIGH Voltage	Guaranteed HIGH input voltage	RUN $\overline{\text{HALT}}$, SSNO	2.4			Volts
V _{IL}	Input LOW Voltage	Guaranteed LOW input voltage	SSNC, $4/\overline{3}$			0.4	Volts

SWITCHING TEST CIRCUIT



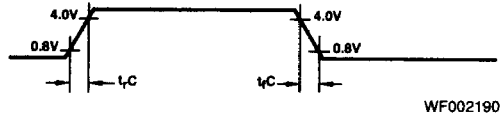
ZCK Output



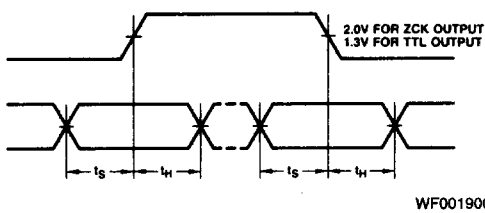
TTL Outputs

SWITCHING TEST WAVEFORMS

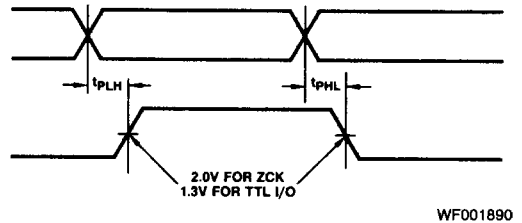
ZCK RISE AND FALL TIMES



SET-UP AND HOLD TIMES



PROPAGATION DELAY TIMES



SWITCHING CHARACTERISTICS —OSCILLATOR, WAIT AND ZCK OUTPUT

($T_A = +25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$)

Parameters	Description	Test Conditions	Min	Typ	Max	Units	
fMAX	Oscillator Frequency	See Test Circuits (Note 7)	24			MHz	
trC	ZCK Rise Time	ZCK $C_L = 80\text{pF}$ (Note 8)		9	14	ns	
tfC	ZCK Fall Time			7.6	11	ns	
trC	ZCK Rise Time	ZCK $C_L = 200\text{pF}$ (Note 8)		15.4	20	ns	
tfC	ZCK Fall time			14.0	20	ns	
tPLH	READY to WAIT	See Test Circuits		8	14	ns	
tPHL				11.5	16	ns	
tPLH	Status ST_i to WAIT			13	17	ns	
tPHL				17.2	21	ns	
ts	CLR to OSC () Setup Time				15	18	ns
th	CLR to OSC () Hold Time				-11	-6	ns

Notes: 7. Specification is based on fundamental mode crystal. See application section.
8. ZCK rise and fall times are based on a bootstrap capacitor value of 27pF.

SWITCHING CHARACTERISTICS — $4/3 = \text{HIGH}$ (AmZ8000 Mode) $(T_A = +25^\circ\text{C}, V_{CC} = 5.0\text{V})$

Parameters	Description	Test Conditions	Min	Typ	Max	Units	
t_s	READY to ZCK Set-up Time	See Test Circuits ZCK $C_L = 80\text{pF}$	T/4 + 10	T/4 + 4.5		ns	
t_H	READY to ZCK Hold Time		T/4 + 2	T/4		ns	
t_s	Status ST_i to ZCK Set-up Time		T/4 + 12	T/4 + 9.5		ns	
t_H	Status ST_i to ZCK Hold Time		T/4 - 3	T/4 - 7.5		ns	
t_s	$\overline{\text{TOEN}}$ to ZCK Set-up Time		30	22		ns	
t_H	$\overline{\text{TOEN}}$ to ZCK Hold Time		-10	-16		ns	
t_{SKEW}	ZCK to OSC		3	6	10	ns	
t_{SKEW}	ZCK to TCK		0	4.0	7	ns	
t_{PLH}	ZCK to $\overline{\text{RESET OUT}}$ Propagation Delay				9.0	13	ns
t_{PHL}					4	8	ns

Note: 9. T = ZCK period.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE —
OSCILLATOR, WAIT AND ZCK OUTPUTS***

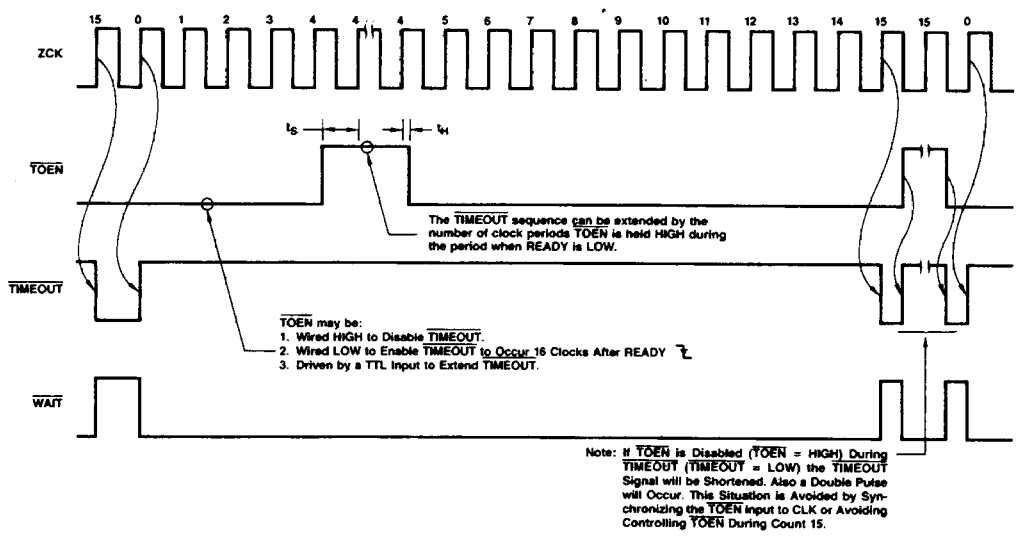
Parameters	Description	Test Conditions	COMMERCIAL			MILITARY			Units
			Min	Max 0°C	70°C	Min	Max -55°C	125°C	
f_{MAX}	Oscillator Frequency	(Note 7)	24			24			MHz
t_{rC}	ZCK Rise Time	$C_L = 80\text{pF}$ (Note 8)		15	15		20	15	ns
t_{fC}	ZCK Fall Time			14	14		20	14	ns
t_{rC}	ZCK Rise Time	$C_L = 200\text{pF}$ (Note 8)		25	20		32	20	ns
t_{fC}	ZCK Fall time			25	20		32	20	ns
t_{PLH}	READY to WAIT Propagation Delay	See Test Circuits		17	17		19	19	ns
t_{PHL}				19	19		19	19	ns
t_{PLH}	Status ST_i to WAIT Propagation Delay			20	20		22	22	ns
t_{PHL}				25	25		25	25	ns
t_s	$\overline{\text{CLR}}$ to OSC (\downarrow) Setup Time			21			30		ns
t_H	$\overline{\text{CLR}}$ to OSC (\downarrow) Hold Time			-3			0		ns

*AC performance over the operating temperature range is guaranteed by testing defined in Group A, Subgroup 9.

**SWITCHING CHARACTERISTICS OVER OPERATING RANGE —
 $4/3 = \text{HIGH}$ (AmZ8000 Mode)**

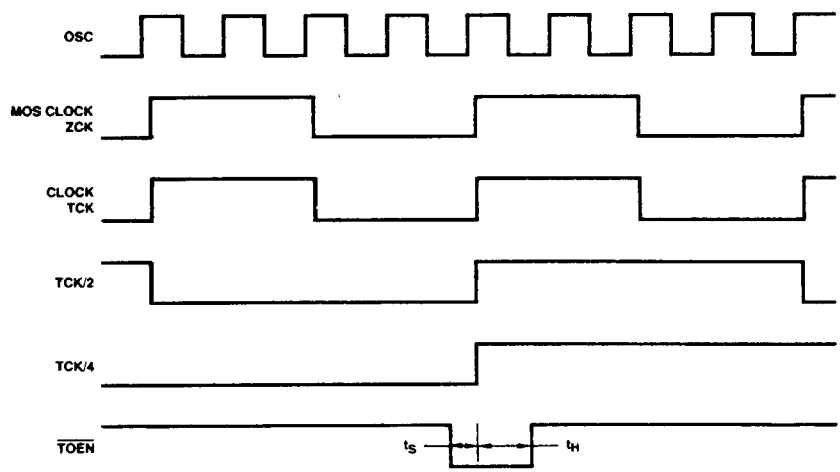
Parameters	Description	Test Conditions	COMMERCIAL		MILITARY		Units
			Min	Max	Min	Max	
t_s	READY to ZCK Setup Time	See Test Circuits ZCK, $C_L = 80\text{pF}$	T/4 + 14		T/4 + 17		ns
t_H	READY to ZCK Hold Time		T/4 + 5		T/4 + 5		ns
t_s	Status ST_i to ZCK Setup Time		T/4 + 15		T/4 + 20		ns
t_H	Status ST_i to ZCK Hold Time		T/4		T/4 + 5		ns
t_s	$\overline{\text{TOEN}}$ to ZCK Setup Time		35		40		ns
t_H	$\overline{\text{TOEN}}$ to ZCK Hold Time		-5		0		ns
t_{SKEW}	ZCK to OSC Skew		2	14	2	17	ns
t_{SKEW}	ZCK to TCK Skew		-2	10	-2	14	ns
t_{PLH}	ZCK to $\overline{\text{RESETOUT}}$ Propagation Delay				16	20	ns
t_{PHL}					16	20	ns

TIMEOUT COUNTER TIMING



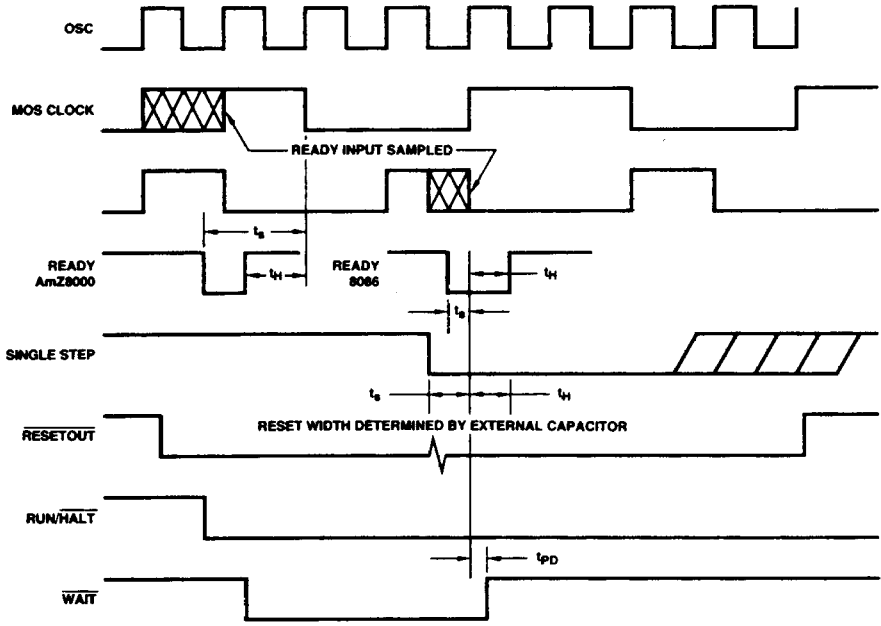
WF002020

Am8127 CLOCK OUTPUTS DIVIDE BY 4 MODE (AmZ8000)



WF002030

Am8127 READY, WAIT, RESET, AND SINGLE STEP



WF002010