

High Voltage Power Factor Controller

FEATURES

- Lossless Off-Line Startup
- Output Overvoltage Comparator
- Leading Edge Blanking (LEB) for Noise Immunity
- Watchdog Timer to Initiate Switching
- Restart Delay Timer

APPLICATIONS

- Industrial Lighting
- AC Motors
- Display Systems
- Personal Computers
- Peripherals

ORDERING INFORMATION

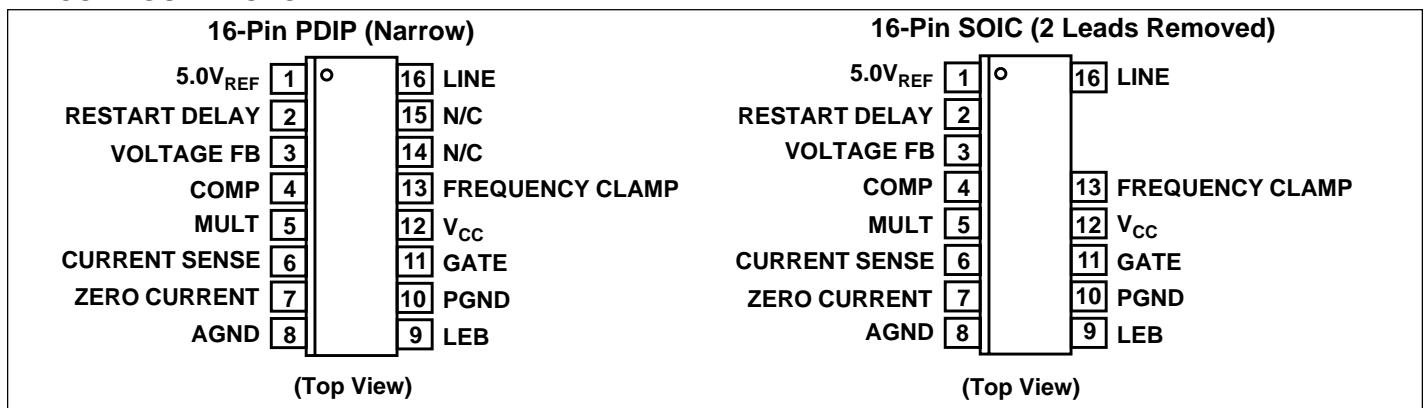
Part No.	Package	Operating Temp. Range
TC33368VOM	16-Pin SOIC (2 Leads Removed)	-25° to +125°C
TC33368VPE	16-Pin PDIP (Narrow)	-25° to +125°C

GENERAL DESCRIPTION

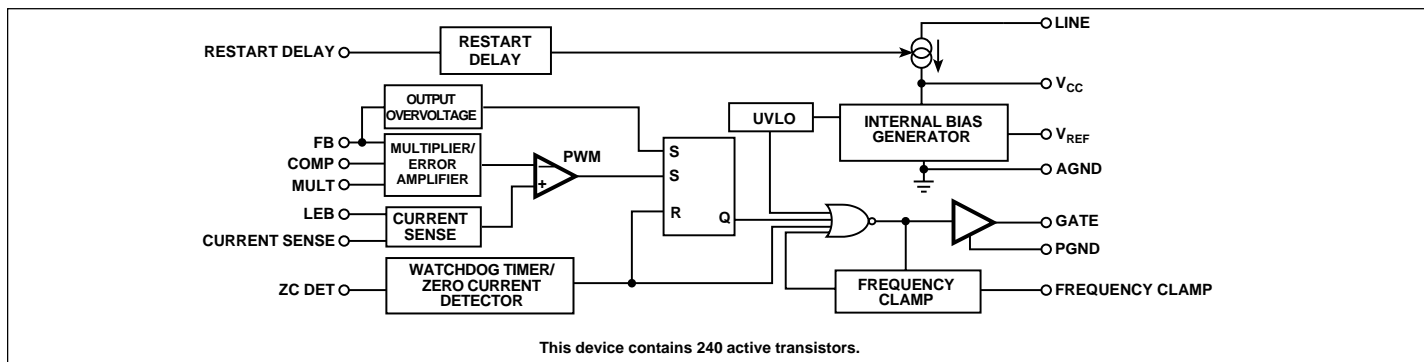
The TC33368 is an active power factor controller that functions as a boost preconverter in off-line power supply applications. TC33368 is optimized for low power, high density power supplies requiring a minimum board area, reduced component count and low power dissipation. The narrow body SOIC package provides a small footprint. Integration of the high voltage startup saves approximately 0.7W of power compared to resistor bootstrapped circuits.

The TC33368 features a watchdog timer to initiate output switching, a one quadrant multiplier to force the line current to follow the instantaneous line voltage a zero current detector to ensure critical conduction operation, a transconductance error amplifier, a current sensing comparator, a 5.0V reference, an undervoltage lockout (UVLO) circuit which monitors the V_{CC} supply voltage and a CMOS driver for driving MOSFETs. The TC33368 also includes a programmable output switching frequency clamp. Protection features include an output overvoltage comparator to minimize overshoot, a restart delay timer and cycle-by-cycle current limiting.

PIN CONFIGURATIONS



REPRESENTATIVE BLOCK DIAGRAM



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MAXIMUM RATINGS: $T_A = 25^\circ\text{C}$, unless otherwise noted

Power Supply Voltage (Transient)	$V_{CC} = 20\text{V}$
Power Supply Voltage (Operating)	$V_{CC} = 16\text{V}$
Line Voltage	$V_{LINE} = 500\text{V}$
Current Sense, Multiplier, Compensation, Voltage Feed Back, Restart Delay and Zero Current Input Voltage	$V_{IN2} = -1.0$ to $+10\text{V}$
LEB Unput, Frequency Clamp Input	$V_{IN2} = -1.0$ to $+20\text{V}$
Zero Current Detect Input	$I_{IN} = \pm 5.0\text{mA}$
Restart Diode Current	$I_{IN} = 5.0\text{mA}$

Power Dissipation and Thermal Characteristics

16-Pin PDIP (Narrow):

Max Power Dissipation @ $T_A = 70^\circ\text{C}$ $P_D = 1.25\text{mW}$

Thermal Resistance, Junction-to-Air $R_{\theta JA} = 100^\circ\text{C/W}$

16-Pin SOIC (2 Leads Removed):

Max Power Dissipation @ $T_A = 70^\circ\text{C}$ $P_D = 450\text{mW}$

Thermal Resistance, Junction-to-Air $R_{\theta JA} = 178^\circ\text{C/W}$

Operating Junction Temperature $T_J = 150^\circ\text{C}$

Operating Ambient Temperature (Note 3) ... $T_A = -25^\circ\text{C}$ to $+125^\circ\text{C}$

Storage Temperature Range $T_{STG} = -55^\circ\text{C}$ to $+150^\circ\text{C}$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS: $V_{CC} = 14.5\text{V}$, for typical values $T_A = 25^\circ\text{C}$, for min/max values $T_J = -25^\circ\text{C}$ to $+125^\circ\text{C}$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Error Amplifier						
I_{IB}	Input Bias Current	$V_{FB} = 5.0\text{V}$	—	0	1.0	μA
V_{IO}	Input Offset Voltage	$V_{COMP} = 3.0\text{V}$	—	2.0	50	mV
g_M	Transconductance	$V_{COMP} = 3.0\text{V}$	30	51	80	μmho
I_O	Output Source	$V_{FB} = 4.6\text{V}$, $V_{COMP} = 3.0\text{V}$	9.0	17.5	30	μA
I_{OUT}	Output Sink	$V_{FB} = 5.4\text{V}$, $V_{COMP} = 3.0\text{V}$	9.0	17.5	30	
Overvoltage Comparator						
$V_{FB(OV)}$	Voltage Feedback Input Threshold		$1.07V_{FB}$	$1.084V_{FB}$	$1.1V_{FB}$	V
T_P	Propagation Time to Output		—	705	—	nsec
Multiplier						
I_{IB}	Input Bias Current	$V_{MULT} (V_{FB} = 0\text{V})$	—	-0.2	-1.0	μA
$V_{TH(M)}$	Input Threshold	V_{COMP}	1.8	2.1	2.4	V
	Dynamic Input Voltage Range					V
V_{MULT} V_{COMP}	Multiplier Input Compensation		0 to 2.5 $V_{TH(M)}$ to $(V_{TH(M)} + 1.0)$	0 to 3.5 $V_{TH(M)}$ to $(V_{TH(M)} + 2.0)$	— —	
K	Multiplier Gain $\left[K = \frac{V_{CS\text{Threshold}}}{V_{MULT}(V_{COMP} - V_{TH(M)})} \right]$	$(V_{MULT} = 0.5\text{V}, V_{COMP} = V_{TH(M)} + 1.0\text{V})$	0.25	0.51	0.75	1/V
Voltage Reference						
V_{REF}	Voltage Reference	$I_O = 0\text{mA}$, $T_J = 25^\circ\text{C}$	4.95	5.0	5.05	V
Reg_{LINE}	Line Regulation	$V_{CC} = 10\text{V}$ to 16V	—	5.0	100	mV
Reg_{LOAD}	Load Regulation	$I_O = 0 - 5.0\text{mA}$	—	5.0	100	mV
V_{REF}	Total Output Variation Over Line, Load and Temperature		4.8	—	5.2	V
I_{OUT}	Maximum Output Current		5.0	10	—	mA
V_{TH}	Reference Undervoltage Lockout Threshold		—	4.5	—	V
Zero Current Detector						
V_{TH}	Input Threshold Voltage	V_{IN} Increasing	1.0	1.2	1.4	V
V_H	Hysteresis	V_{IN} Decreasing	100	200	300	mV
T_{PD}	Delay to Output		—	127	—	nsec

High Voltage Power Factor Controller

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ELECTRICAL CHARACTERISTICS: $V_{CC} = 14.5V$, for typical values $T_A = 25^\circ C$, for min/max values $T_J = -25^\circ C$ to $+125^\circ C$.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Current Sense Comparator						
I_{IB}	Input Bias Current	$V_{CS} = 0$ to $2.0V$	—	0.2	1.0	μA
V_{IO}	Input Offset Voltage	$V_{MULT} = -0.2V$	—	4.0	50	mV
$V_{TH(MAX)}$	Max Current Sense Input Threshold	$V_{COMP} = 5.0V$, $V_{MULT} = 5.0V$	1.3	1.5	1.8	V
$t_{PHL(IN/OUT)}$	Delay to Output	$V_{LEB} = 12V$, $V_{COMP} = 5.0V$, $V_{MULT} = 5.0V$, $V_{CS} = 0$ to $5.0V$ Step $C_L = 1.0nF$	50	270	425	nsec
Frequency Clamp						
$V_{TH(FC)}$	Frequency Clamp Input Threshold		1.9	2.0	2.1	V
I_{RESET}	Frequency Clamp Capacitor Reset Current	$V_{FC} = 0.5V$	0.5	1.7	4.0	mA
V_{DFC}	Frequency Clamp Disable Voltage		—	7.3	8.0	V
Drive Output						
R_{OH}	Source Resistance	Current Sense = $0V$, $V_{GATE} = V_{CC} - 1.0V$	4.0	8.6	20	Ω
R_{OL}	Sink Resistance	Current Sense = $3.0V$, $V_{GATE} = 1.0V$	4.0	7.2	20	
t_R	Output Voltage Rise Time	25% – 75%, $C_L = 1.0nF$	—	55	200	nsec
t_F	Output Voltage Fall Time	75% – 25%, $C_L = 1.0nF$	—	70	200	nsec
$V_{OUT(UV)}$	Output Voltage in Undervoltage	$V_{CC} = 7.0V$, $I_{SINK} = 1.0mA$	—	0.01	0.25	V
Leading Edge Blanking						
I_{BIAS}	Input Bias Current		—	0.1	0.5	μA
V_{LEB}	Threshold (as Offset from V_{CC})	V_{LEB} Increasing	1.0	2.25	2.75	V
V_H	Hysteresis	V_{LEB} Decreasing	100	270	500	mV
Undervoltage Lockout						
$V_{TH(ON)}$	Startup Threshold	V_{CC} Increasing	11.5	13	14.5	V
$V_{SHUTDOWN}$	Min. Operating Voltage After Turn-On	V_{CC} Decreasing	7.0	8.5	10	V
V_H	Hysteresis		—	4.5	—	V
Timer						
t_{DLY}	Watchdog Timer		180	385	800	μsec
$V_{TH(RESTART)}$	Restart Timer Threshold		1.5	2.3	3.0	V
$I_{RESTART}$	Restart Pin Output Current	$V_{RESTART} = 0V$, $V_{REF} = 5.0V$	3.1	5.2	7.1	mA
Total Device						
I_{SU}	Line Startup Current	$V_{CC} = 0V$, $V_{LINE} = 50V$	5.0	16	25	mA
I_{OP}	Line Operating Current	$V_{CC} = V_{TH(ON)}$, $V_{LINE} = 50V$	3.0	12.9	20	mA
I_{CC}	V_{CC} Dynamic Operating Current	50kHz, $C_L = 1.0nF$	—	5.3	8.5	mA
	V_{CC} Static Operating Current	$I_{OUT} = 0$	—	3.0	—	
I_{LINE}	Line Pin Leakage	$V_{LINE} = 500V$	—	30	80	μA

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INTRODUCTION

With the goal of exceeding the requirements of legislation on line current harmonic content, there is an ever increasing demand for an economical method of obtaining a unity power factor. This data sheet describes a monolithic control IC that was specifically designed for power factor control with minimal external components. It offers the designer a simple cost effective solution to obtain the benefits of active power factor correction.

Most electronic ballasts and switching power supplies use a bridge rectifier and a bulk storage capacitor to derive raw DC voltage from the utility AC line, Figure 1.

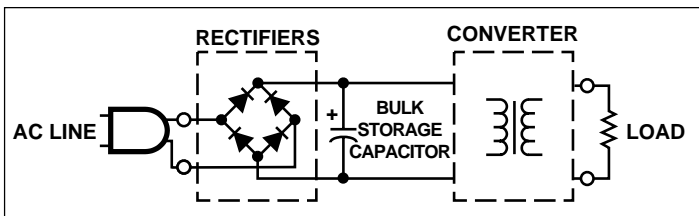


Figure 1. Uncorrected Power Factor Circuit

This simple rectifying circuit draws power from the line when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and results in a high charge current spike, Figure 2. Since power is only taken near the line voltage peaks, the resulting spikes of current are extremely nonsinusoidal with a high content of harmonics. This results in a poor power factor condition where the apparent input power is much higher than the real power. Power factor ratios of 0.5 to 0.7 are common.

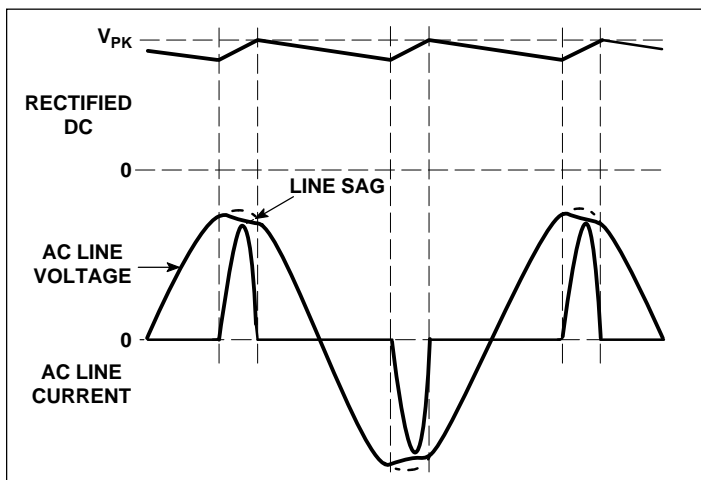


Figure 2. Uncorrected Power Factor Input Waveforms

Power factor correction can be achieved with the use of either a passive or active input circuit. Passive circuits usually contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits incorporate some form of a high frequency switching converter for the power processing with the boost converter being the most popular topology. Since active input circuits operate at a frequency much higher than that of the ac line, they are smaller, lighter in weight, and more efficient than a passive circuit that yields similar results. With proper control of the preconverter, almost any complex load can be made to appear resistive to the ac line, thus significantly reducing the harmonic current content.

Operating Description

The TC33368 contains many of the building blocks and protection features that are employed in modern high performance current mode power supply controllers. Referring to the block diagram in Figure 3, note that a multiplier has been added to the current sense loop and that this device does not contain an oscillator. A description of each of the functional blocks is given below.

Error Amplifier

An Error Amplifier with access to the inverting input and output is provided. The amplifier is a transconductance type, meaning that it has high output impedance with controlled voltage-to-current gain ($g_m \approx 50 \mu\text{mhos}$). The noninverting input is internally biased at $5.0\text{V} \pm 2.0\%$. The output voltage of the power factor converter is typically divided down and monitored by the inverting input. The maximum input bias current is $-1.0\mu\text{A}$ which can cause an output voltage error that is equal to the product of the input bias current and the value of the upper divider resistor R2. The Error Amplifier output is internally connected to the Multiplier and is pinned out (Pin 4) for external loop compensation. Typically, the bandwidth is set below 20Hz so that the amplifier's output voltage is relatively constant over a given ac line cycle. In effect, the error amplifier monitors the average output voltage of the converter over several line cycles resulting in a fixed Drive Output on-time. The amplifier output stage can sink and source $11.5\mu\text{A}$ of current and is capable of swinging from 1.7 to 5.0V, assuring that the Multiplier can be driven over its entire dynamic range.

Note that by using a transconductance type amplifier, the input is allowed to move independently with respect to the output, since the compensation capacitor is connected to ground. This allows dual usage of the Voltage Feedback pin by the Error Amplifier and Overvoltage Comparator.

Overvoltage Comparator

An Overvoltage Comparator is incorporated to eliminate the possibility of runaway output voltage. This condition can occur during initial startup, sudden load removal, or during output arcing and is the result of the low bandwidth that must be used in the Error Amplifier control loop. The Overvoltage Comparator monitors the peak output voltage of the converter, and when exceeded, immediately terminates MOSFET switching. The comparator threshold is internally set to $1.08V_{REF}$. In order to prevent false tripping during normal operation, the value of the output filter capacitor C3 must be large enough to keep the peak-to-peak ripple less than 16% of the average DC output.

Multiplier

A single quadrant, two input multiplier is the critical element that enables this device to control power factor. The ac haversines are monitored at Pin 5 with respect to ground while the Error Amplifier output at Pin 4 is monitored with respect to the Voltage Feedback Input threshold. A graph of the Multiplier transfer curve is shown in Figure 9. Note that both inputs are extremely linear over a wide dynamic range, 0 to 3.2V for Pin 5 and 2.5V to 4.0V for Pin 4. The Multiplier output controls the Current Sense Comparator threshold as the ac voltage traverses sinusoidally from zero to peak line. This has the effect of forcing the MOSFET on-time to track the input line voltage, thus making the preconverter load appear to be resistive.

$$\text{Pin 6 Threshold} \approx 0.55 (V_{\text{PIN 4}} - V_{\text{PIN 3}}) V_{\text{PIN 5}}$$

Zero Current Detector

The TC33368 operates as a critical conduction current mode controller, whereby output switch conduction is initiated by the Zero Current Detector and terminated when the peak inductor current reaches the threshold level established by the Multiplier output. The Zero Current Detector initiates the next on-time by setting the R_S Latch at the instant the inductor current reaches zero. This critical conduction mode of operation has two significant benefits. First, since the MOSFET cannot turn-on until the inductor current reaches zero, the output rectifier's reverse recovery time becomes less critical allowing the use of an inexpensive rectifier. Second, since there are no deadtime gaps between cycles, the ac line current is continuous thus limiting the peak switch to twice the average input current.

The Zero Current Detector indirectly senses the inductor current by monitoring when the auxiliary winding voltage falls below 1.2V. To prevent false tripping, 200mV of hysteresis is provided. The Zero Current Detector input is internally protected by two clamps. The upper 10V clamp prevents

input overvoltage breakdown while the lower $-0.7V$ clamp prevents substrate injection. An external resistor must be used in series with the auxiliary winding to limit the current through the clamps to 5.0mA or less.

Current Sense Comparator and R_S Latch

The Current Sense Comparator R_S Latch configuration used ensures that only a single pulse appears at the Drive Output during a given cycle. The inductor current is converted to a voltage by inserting a ground-referenced sense resistor R7 in series with the source of output switch. This voltage is monitored by the Current Sense Input and compared to a level derived from the Multiplier output. The peak inductor current under normal operating conditions is controlled by the threshold voltage of Pin 6 where:

$$I_{PK} = \frac{\text{Pin 6 Threshold}}{R7}$$

Abnormal operating conditions occur when the preconverter is running at extremely low line or if output voltage sensing is lost. Under these conditions, the Current Sense Comparator threshold will be internally clamped to 1.5V. Therefore, the maximum peak switch current is:

$$I_{PK} (\text{MAX}) = \frac{1.5V}{R7}$$

With the component values shown in Figure 3, the Current Sense Comparator threshold, at the peak of the haversine, varies from 110mV at 90V_{AC} to 100mV at 268V_{AC}. The Current Sense Input to Drive Output propagation delay is typically 200nsec.

Timer

A watchdog timer function was added to the IC to eliminate the need for an external oscillator when used in stand alone applications. The Timer provides a means to automatically start or restart the preconverter if the Drive Output has been off for more than 385μsec after the inductor current reaches zero.

Undervoltage Lockout and Quickstart

The TC33368 has a 5.0V internal reference brought out to Pin 1 and capable of sourcing 10mA typically. It also contains an Undervoltage Lockout (UVLO) circuit which suppresses the Gate output at Pin 11 if the V_{CC} supply voltage drops below 8.5V typical.

A Quickstart circuit has been incorporated to optimize converter startup. During initial startup, compensation capacitor C1 will be discharged, holding the Error Amplifier output below the Multiplier's threshold. This will prevent Drive Output switching and delay bootstrapping of capacitor C4 by diode D6. If Pin 4 does not reach the multiplier

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threshold before C4 discharges below the lower SMPS UVLO threshold, the converter will hiccup and experience a significant startup delay. The Quickstart circuit is designed to precharge C1 to 1.7V. This level is slightly below the Pin 4 Multiplier threshold, allowing immediate Drive Output switching.

Restart Delay

A restart delay pin is provided to allow hiccup mode fault protection in case of a short circuit condition and to prevent the SMPS from repeatedly trying to restart after the input line voltage has been removed. When power is first applied, there is no startup delay, but subsequent cycling of the V_{CC} voltage will result in delay times that are programmed by an external resistor and capacitor. The Restart Delay, Pin 2, is a high impedance, so that an external capacitor can provide delay times as long as several seconds.

If the SMPS output is short circuited, the transformer winding, which provides the V_{CC} voltage to the control IC and the TC33368, will be unable to sustain V_{CC} to the control circuits. The restart delay capacitor at Pin 2 of the TC33368 prevents the high voltage startup transistor within the IC from maintaining the voltage on C4. After V_{CC} drops below the UVLO threshold in the SMPS, the SMPS switching transistors are held off for the time programmed by the values of the restart capacitor (C9) and resistor (R8). In this manner, the SMPS switching transistors are operated at very low duty cycles, preventing their destruction. If the short circuit fault is removed, the power supply system will turn on by itself in a normal startup mode after the restart delay has timed out.

Output Switching Frequency Clamp

In normal operation, the TC33368 operates the boost inductor in the critical mode. That is, the inductor current ramps to a peak value, ramps down to zero, then immediately begins ramping positive again. The peak current is programmed by the multiplier output within the IC. As the input voltage haversine declines to near zero, the output switch on-time becomes constant, rather than going to zero because of the small integrated dc voltage at Pin 5 caused by C2, R3 and R5. Because of this, the average line current does not exactly follow the line voltage near the zero crossings. The Output Switching Frequency Clamp remedies this situation to improve power factor and minimize EMI generated in this operating region. The values of R10 and C7, as shown in Figure 3, program a minimum off-time in the frequency clamp which overrides the zero current detect signal, forcing a minimum off-time. This allows discontinuous conduction operation of the boost inductor in the zero crossing region, and the average line current more

nearly follows the voltage. The Output Switching Frequency Clamp function can be disabled by connecting the FC input, Pin 13, to the V_{CC} supply Pin 12.

For best results, the minimum off-time, determined by the values of R10 and C7, should be chosen so that $t_{S(MIN)} = t_{(ON)} + t_{(OFF)fc}$. Output drive is inhibited when the voltage at the frequency clamp input is less than 2.0V. When the output drive is high, C7 is discharged through an internal 100 μ A current source. When the output drive switches low, C7 is charged through R10. The drive output is inhibited until the voltage across C7 reaches 2.0V, establishing a minimum off-time where:

$$t_{(OFF)FC} = -R10 C7 \text{ Log}_E \left[1 - \left(\frac{2}{V_{CC}} \right) \right]$$

Output

The IC contains a CMOS output driver that was specifically designed for direct drive of power MOSFETs. The Gate Output is capable of up to ± 1500 mA peak current with a typical rise and fall time of 50nsec with a 1.0nF load. Additional internal circuitry has been added to keep the Gate Output in a sinking mode whenever the Undervoltage Lock-out is active. This characteristic eliminates the need for an external gate pull-down resistor. The totem-pole output has been optimized to minimize cross-conduction current during high speed operation.

Calculation	Formula	Notes
Converter Output Power	$P_{OUT} = V_{OUT} I_{OUT}$	Calculate the maximum required output power.
Peak Indicator Current	$I_{L(PK)} = \frac{2\sqrt{2} P_{OUT}}{\eta V_{AC(LL)}}$	Calculated at the minimum required ac line voltage for output regulation. Let the efficiency $\eta = 0.92$ for low line operation.
Inductance	$L_P = \frac{t \left(\frac{V_{OUT}}{\sqrt{2}} - V_{AC(LL)} \right) \eta V_{AC(LL)}^2}{\sqrt{2} V_{OUT} P_{OUT}}$	Let the switching cycle $t = 40$ sec for universal input (85 to 265 V _{AC}) operation and 20 sec for fixed input (92 to 138Vac, or 184 to 276 V _{AC}) operation.
Switch On-Time	$t_{(ON)} = \frac{2 P_{OUT} L_P}{\eta V_{AC}^2}$	In theory, the on-time $t_{(ON)}$ is constant. In practice, $t_{(ON)}$ tends to increase at the ac line zero crossings due to the charge on capacitor C5. Let $V_{AC} = V_{AC(LL)}$ for initial $t_{(ON)}$ and $t_{(OFF)}$ calculations.
Switch Off-Time	$t_{(OFF)} = \frac{t_{(ON)}}{\frac{V_{OUT}}{\sqrt{2} V_{AC} I \sin \theta} - 1}$	The off-time $t_{(OFF)}$ is greatest at the peak of the AC line voltage and approaches zero at the AC line zero crossings. Theta (θ) represents the angle of the ac line voltage.
Minimum Switch Off-Time	$t_{(OFF) MIN} = \frac{L_P I_{L(PK)}}{V_{OUT}}$	The off-time is at a minimum at AC line crossings. This equation is used to calculate $t_{(OFF)}$ as Theta approaches zero.
Delay Time	$t_D = -R10 C7 \ln\left(\frac{V_{CC} - 2}{V_{CC}}\right)$	The delay time is used to override the minimum off-time at the AC line zero crossings by programming the Frequency Clamp with C7 and R10.
Switching Frequency	$f = \frac{1}{t_{(ON)} + t_{(OFF)}}$	The minimum switching frequency occurs at the peak of the AC line voltage. As the AC line voltage traverses from peak to zero, $t_{(OFF)}$ approaches zero producing an increase in switching frequency.
Peak Switch Current	$R7 = \frac{V_{CS}}{I_{L(PK)}}$	Set the current sense threshold V_{CS} to 1.0V for universal input (85 to 265 V _{AC}) operation and to 0.5V for fixed input (92 to 138 V _{AC} , or 184 to 276 V _{AC}) operation. Note that V_{CS} must be less than 1.4V.
Multiplier Input Voltage	$V_M = \frac{V_{AC} \sqrt{2}}{\left(\frac{R5}{R3} + 1\right)}$	Set the multiplier input voltage V_M to 3.0V at high line. Empirically adjust V_M for the lowest distortion over the ac line voltage range while guaranteeing startup at minimum line.
Converter Output Voltage	$V_{OUT} = V_{REF} \left(\frac{R2}{R1} + 1\right) - I_B R1$	The $I_B R1$ error term can be minimized with a divider current in excess of 100 μ A.
Converter Output Peak-to-Peak Ripple Voltage	$\Delta V_{OUT(PP)} = I_{L(PK)} \sqrt{\left(\frac{1}{2 f_{AC} C3}\right)^2 + (ESR)^2}$	The calculated peak-to-peak ripple must be less than 16% of the average DC output voltage to prevent false tripping of the Overvoltage Comparator. Refer to the Overvoltage Comparator Text. ESR is the equivalent series resistance of C3.
Error Amplifier Bandwidth	$BW = \frac{g_M}{2, C1}$	The bandwidth is typically set to 20Hz. When operating at high AC line, the value of C1 may need to be increased.

Table 1. Design Equations

NOTE: The following converter characteristics must be chosen:

V_{OUT} = Desired output voltage.

I_{OUT} = Desired output current.

V_{AC} = AC RMS operating line voltage.

$V_{AC(LL)}$ = AC RMS minimum required operating line voltage for output regulation.

ΔV_{OUT} = Converter output peak-to-peak ripple voltage.

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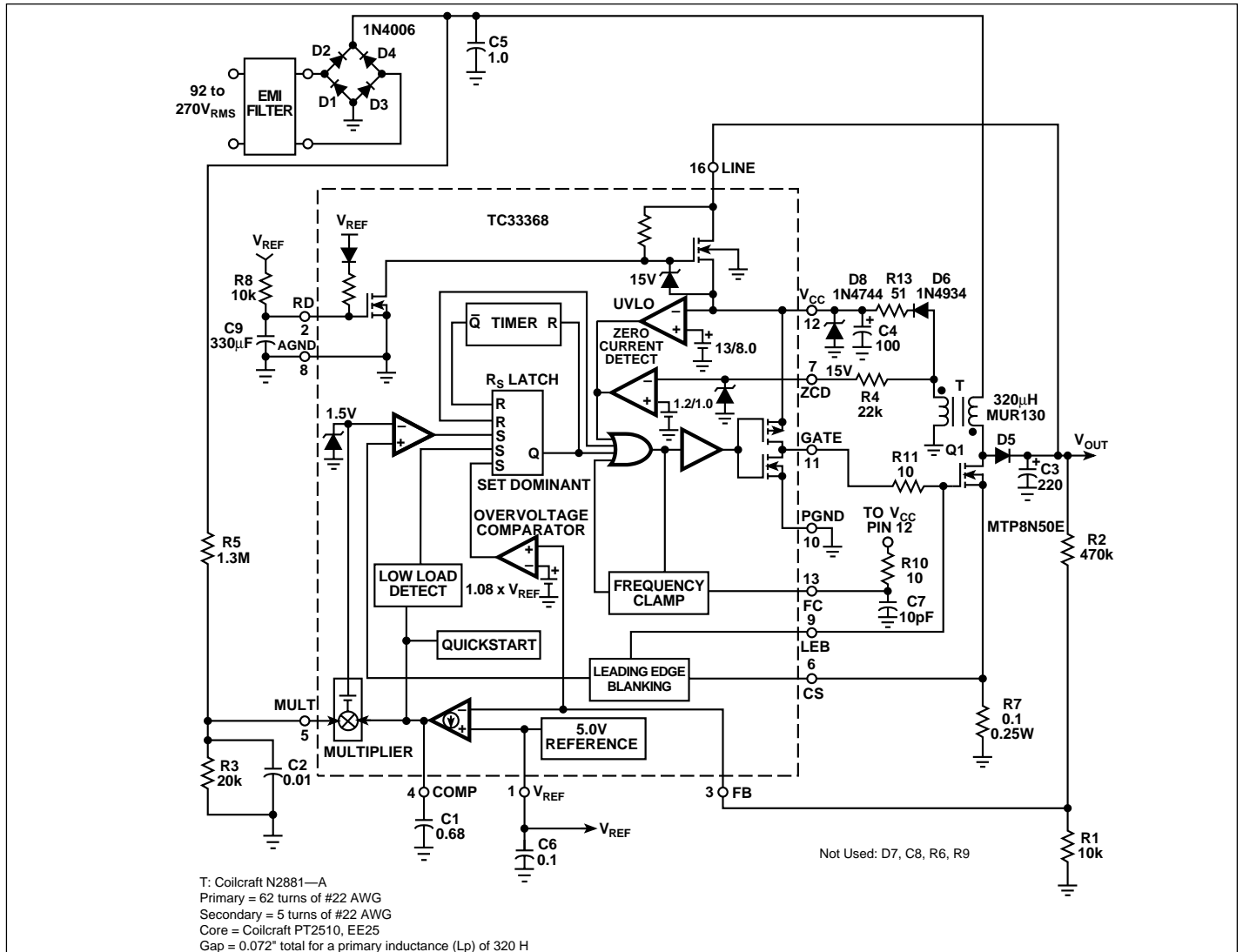


Figure 3. 80W Power Factor Controller

Power Factor Controller Test Data

AC Line Input					DC Output								
V _{RMS}	P _{IN}	PF	I _{FUND}	Current Harmonic Distortion (% I _{FUND})					V _{OUT(PP)}	V _{OUT}	I _{OUT}	P _{OUT}	η(%)
				THD	2	3	5	7					
90	79.7	0.999	0.89	0.5	0.15	0.09	0.06	0.09	3.0	244.4	0.31	76.01	95.4
100	79.3	0.998	0.79	0.5	0.14	0.09	0.08	0.10	3.0	242.9	0.31	75.54	95.3
110	78.9	0.997	0.72	0.5	0.16	0.13	0.08	0.10	3.0	242.9	0.31	75.3	95.4
120	78.5	0.996	0.66	0.5	0.15	0.12	0.08	0.13	3.0	243.0	0.31	75.57	96.3
130	78.1	0.994	0.60	0.5	0.14	0.12	0.07	0.14	3.0	243.0	0.31	75.57	96.7
138	77.8	0.991	0.57	0.5	0.15	0.08	0.08	0.14	3.0	243.0	0.31	75.57	97.1

Heatsink = Aavid Engineering Inc., 590302B03600, or 593002B03400

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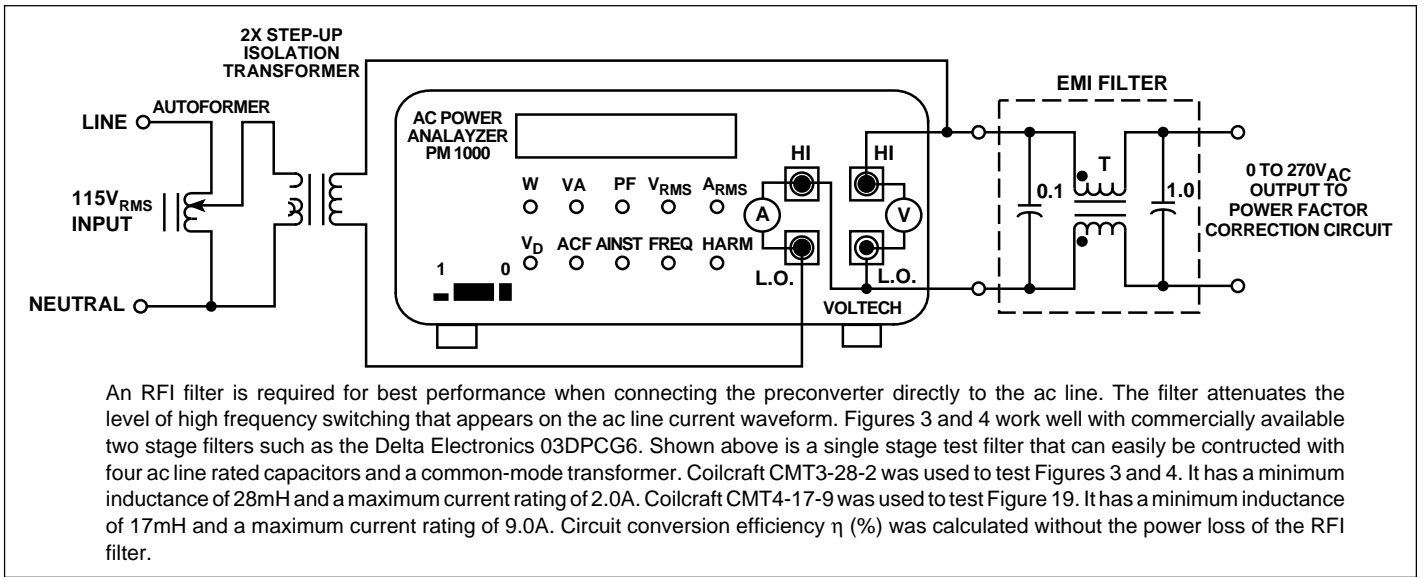


Figure 5. Power Factor Test Setup

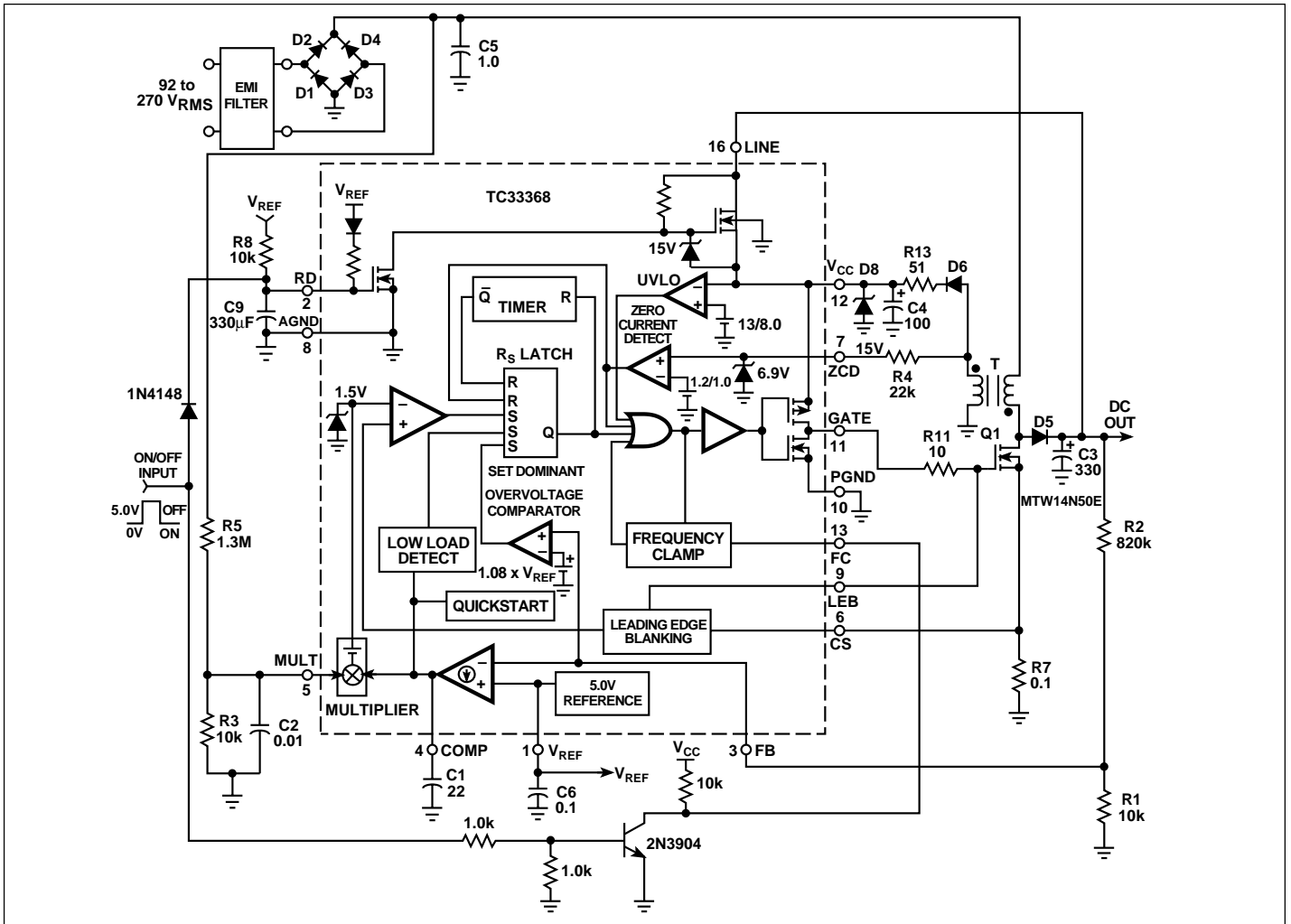


Figure 6. On/Off Control

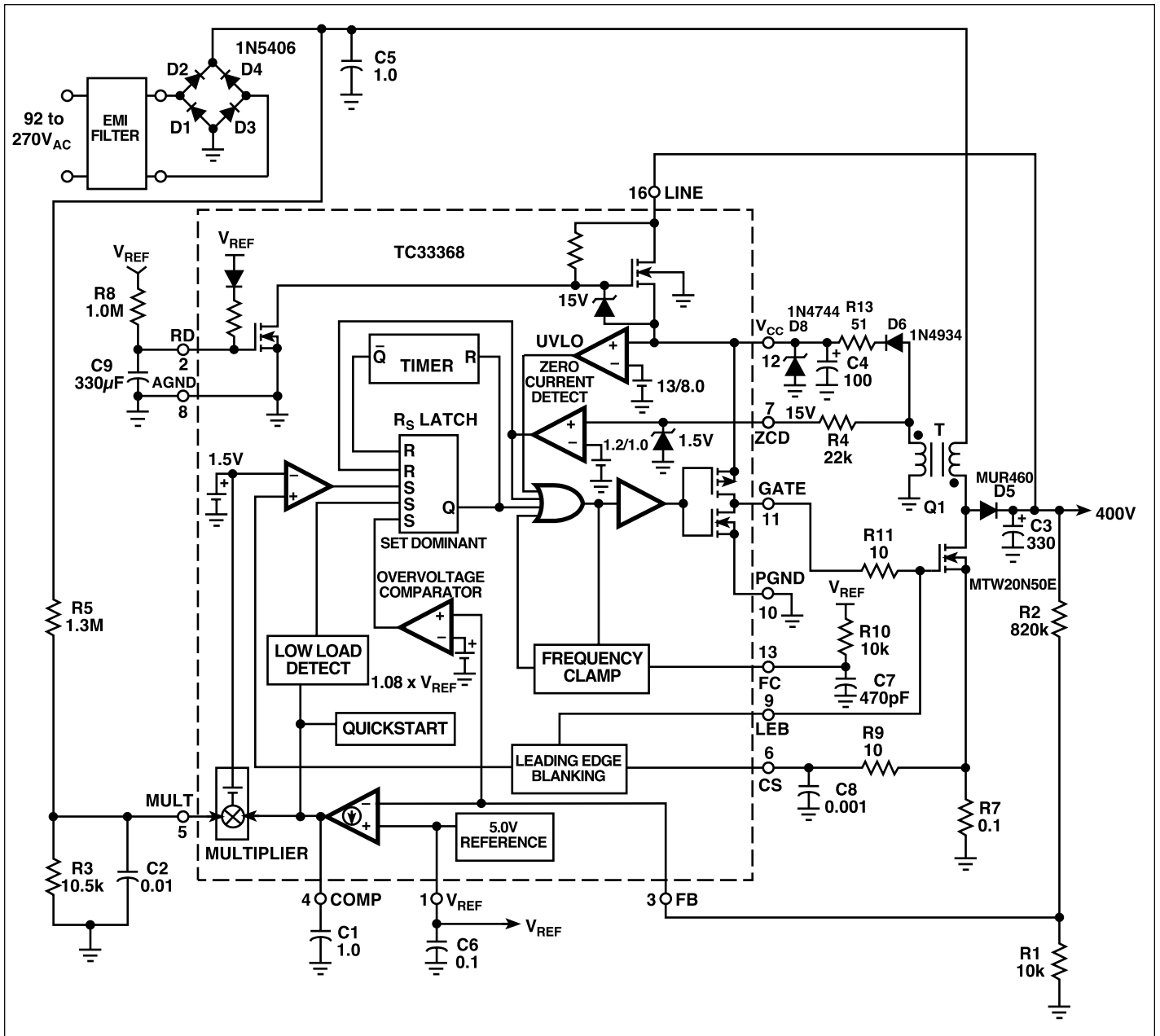
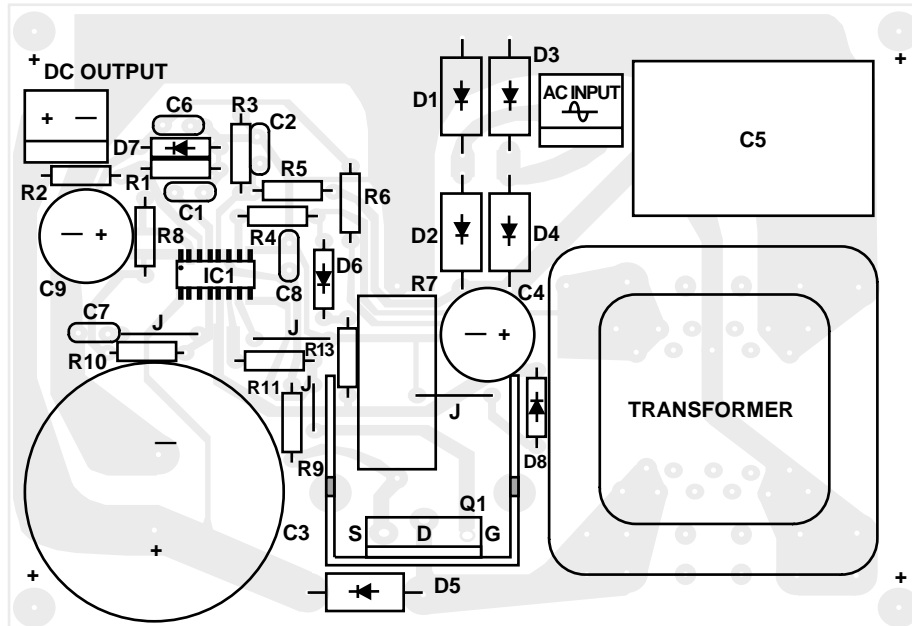


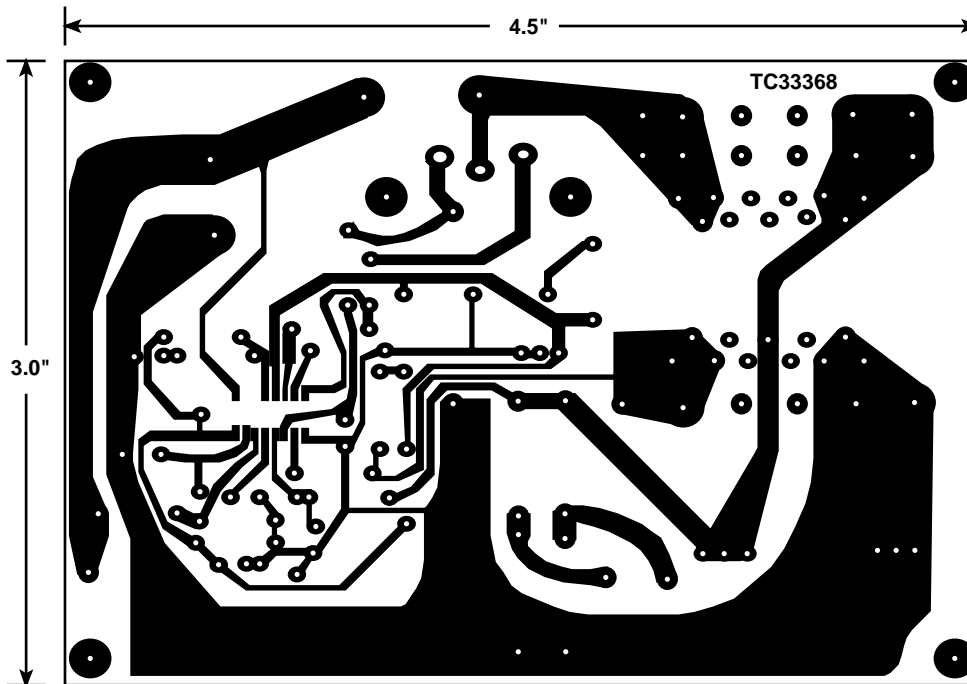
Figure 7. 400W Power Factor Controller

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J = JUMPER

(Top View)



(Bottom View)

Figure 8. Printed Circuit Board and Component Layout (Circuits of Figures 3 and 4)

TYPICAL CHARACTERISTICS

Figure 9. Current Sense Input Threshold versus Multiplier Input

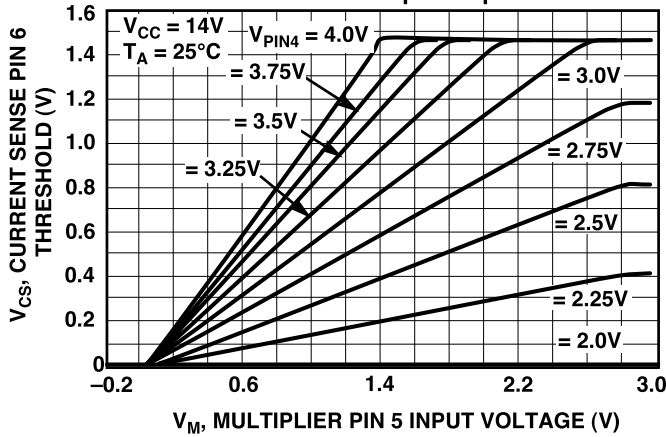


Figure 10. Current Sense Input Threshold versus Multiplier Input, Expanded View

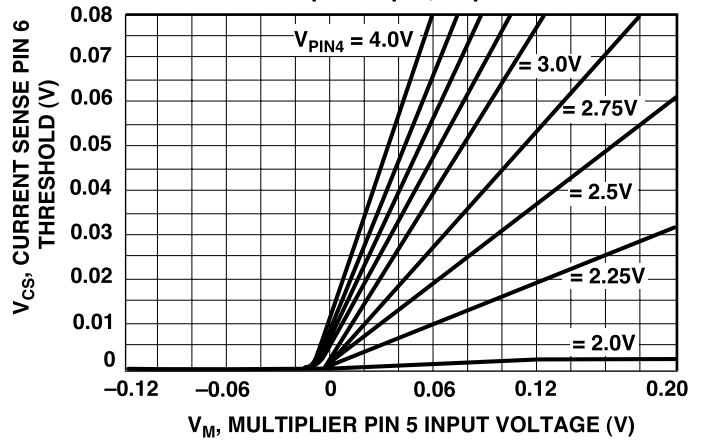


Figure 11. Reference Voltage versus Temperature

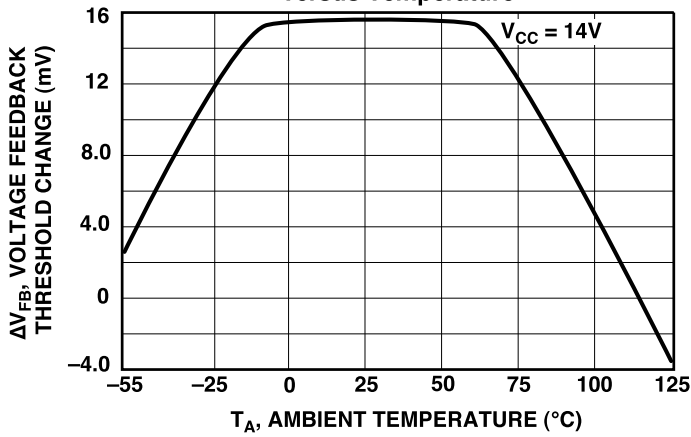


Figure 12. Overvoltage Comparator Input Threshold versus Temperature

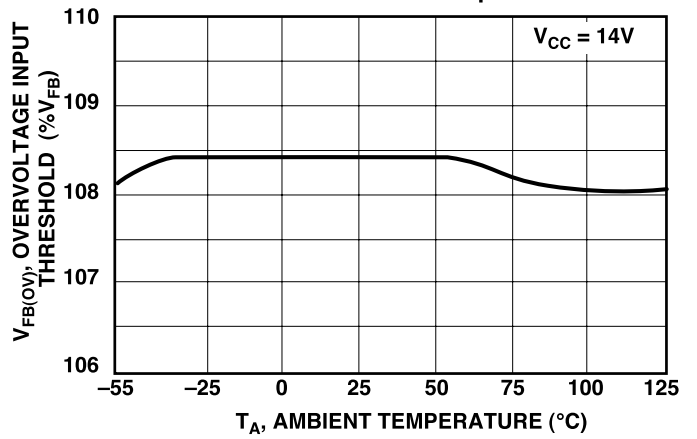


Figure 13. Error Amplifier Transconductance and Phase versus Frequency

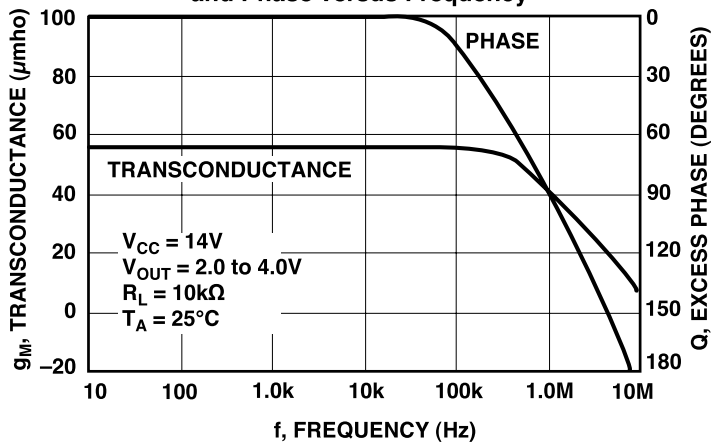
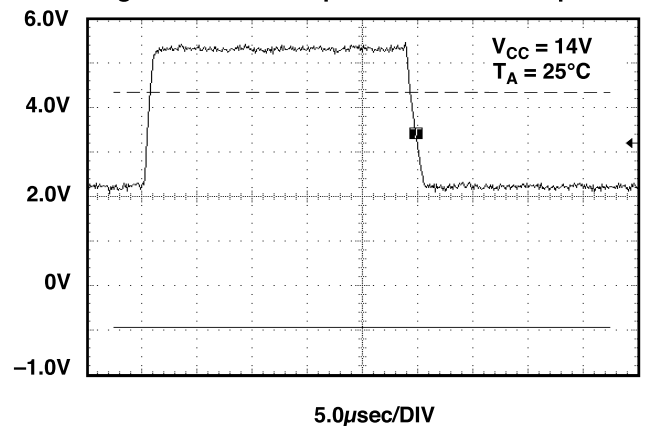


Figure 14. Error Amplifier Transient Response



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TYPICAL CHARACTERISTICS

Figure 15. Quickstart Charge Current versus Temperature

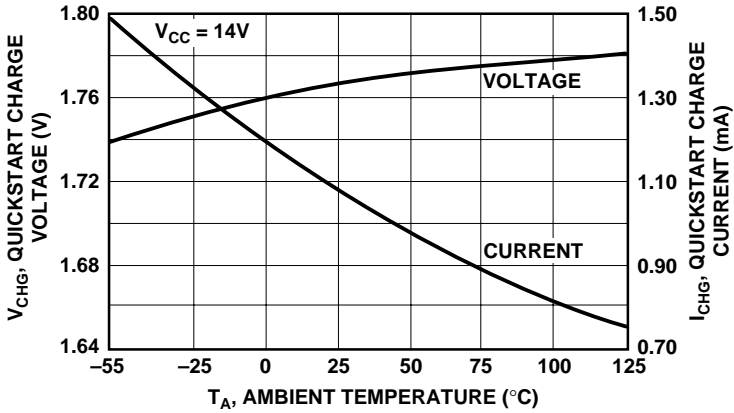


Figure 16. Watchdog Timer Delay versus Temperature

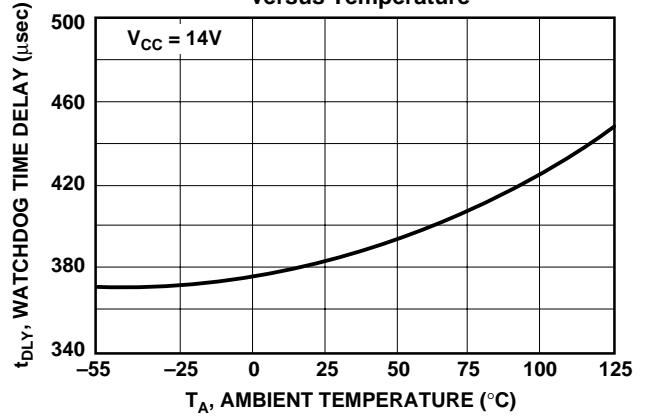


Figure 17. Drive Output Waveform

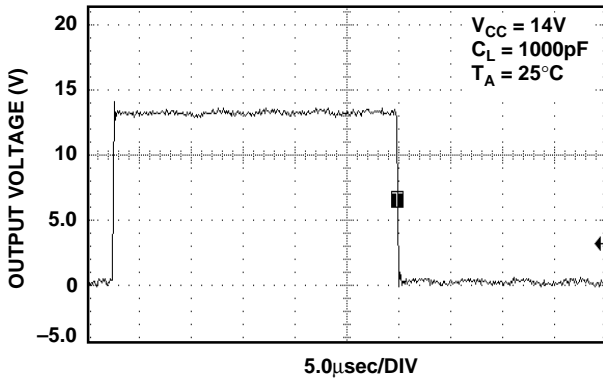


Figure 18. Supply Current versus Supply Voltage

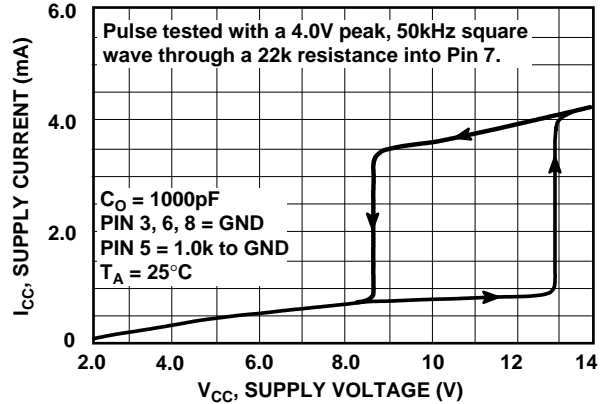


Figure 19. Transient Thermal Resistance

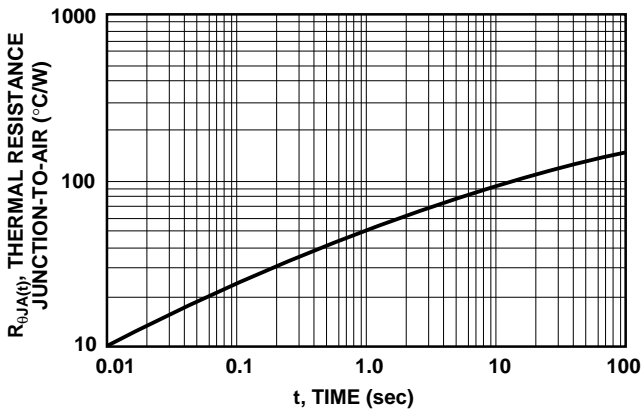
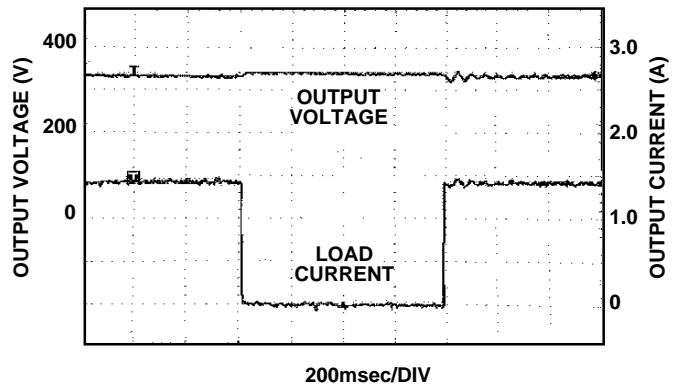
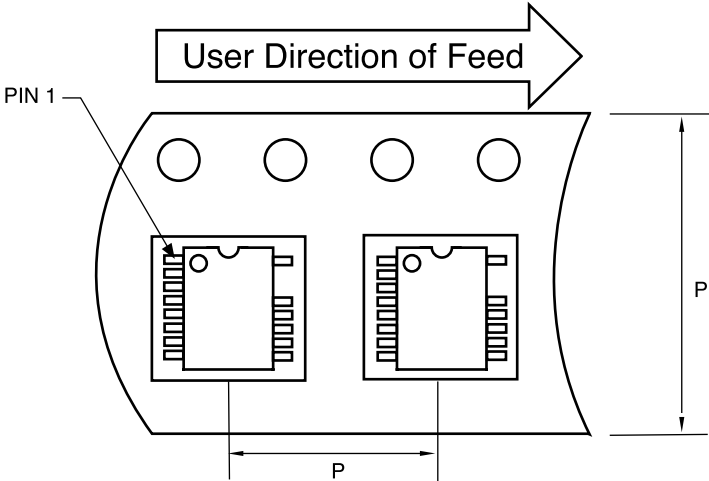


Figure 20. Low Load Detection Response Waveform



TAPE AND REEL INFORMATION

Component Taping Orientation for 16-Pin SOIC (2 Leads Removed) Devices



Standard Reel Component Orientation for TR Suffix Device

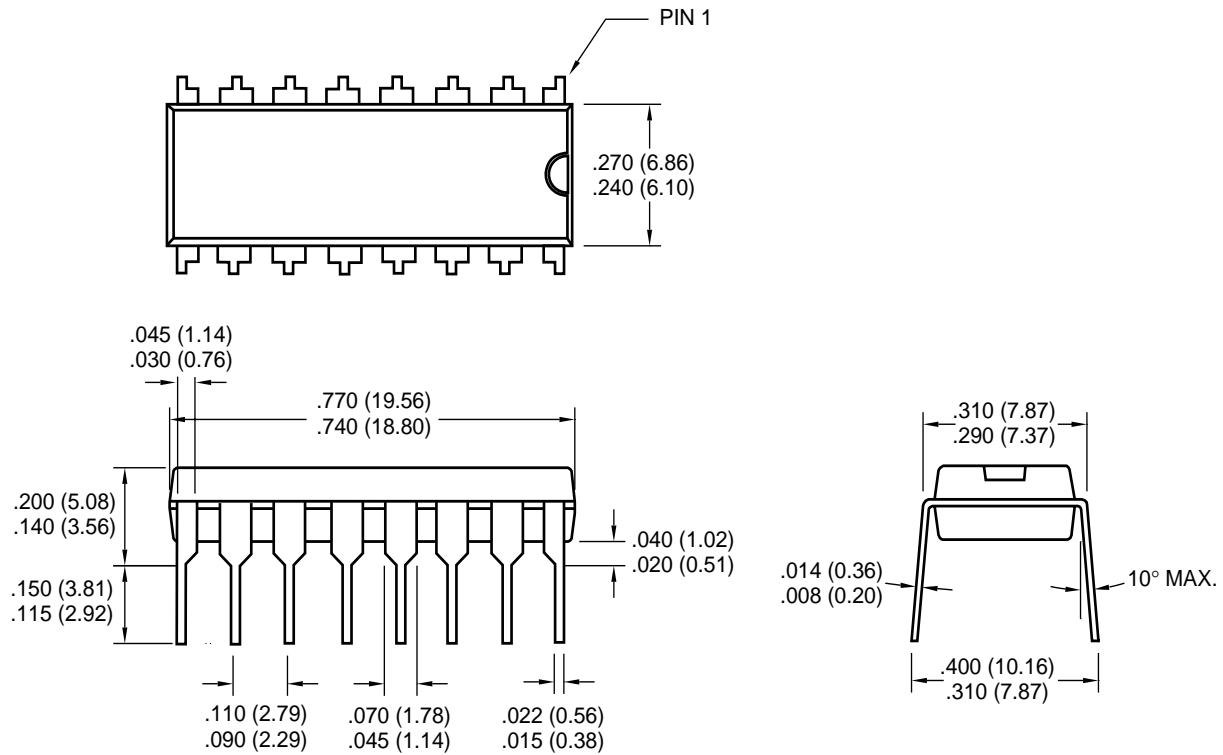
Carrier Tape, Reel Size, and Number of Components Per Reel

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
16-Pin SOIC (2 Leads Removed)	16 mm	8 mm	2500	13 in

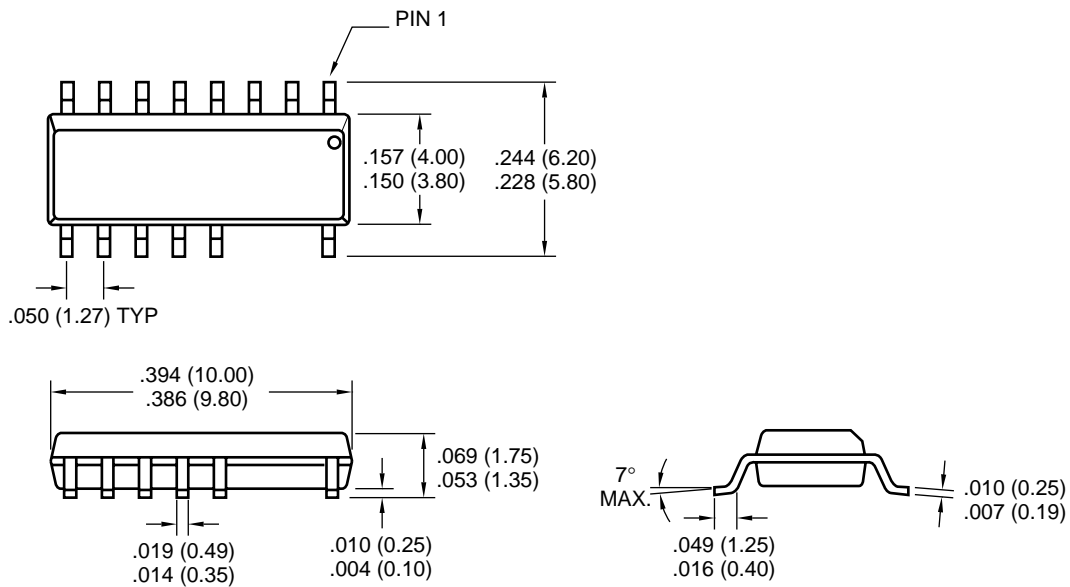
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PACKAGE DIMENSIONS

16-Pin PDIP (Narrow)



16-Pin SOIC (2 Leads Removed)



Dimensions: inches (mm)

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