



### **Trusted Platform Module LPC Interface**

#### SUMMARY DATASHEET

### **Features**

- Fully compliant to the Trusted Computing Group (TCG) Trusted Platform Module (TPM) version 1.2 specification
- Compliant with TCG PC client-specific TPM Interface Specification (TIS) version 1.2
- Single-chip, turnkey solution
- Hardware asymmetric crypto engine
- 2048-bit RSA<sup>®</sup> sign in 200ms
- Atmel<sup>®</sup> AVR<sup>®</sup> RISC microprocessor
- Internal EEPROM storage for RSA keys
- 33MHz Low Pin Count (LPC) bus for easy PC interface
- Secure hardware and firmware design and chip layout
- Internal, high-quality Random Number Generator (RNG) FIPS 140-2 compliant
- NV storage space for 1756 bytes of user defined data
- 3.3V supply voltage
- 28-lead thin TSSOP, 28-lead wide TSSOP, or 40-pad QFN packages
- Offered in both commercial (0 to 70°C) and industrial (-40 to +85°C) temperature ranges

### **Description**

The Atmel AT97SC3204 is a fully integrated security module designed to be integrated into personal computers and other embedded systems. It implements version 1.2 of the Trusted Computing Group (TCG) specification for Trusted Platform Modules (TPM).

The TPM includes a cryptographic accelerator capable of computing a 2048-bit RSA signature in 200ms and a 1024-bit RSA signature in 40ms. Performance of the SHA-1 accelerator is 20µs per 64-byte block.

The chip communicates with the PC through the LPC interface. The TPM supports SIRQ (for interrupts) and CLKRUN to permit clock stopping for power savings in mobile computers.

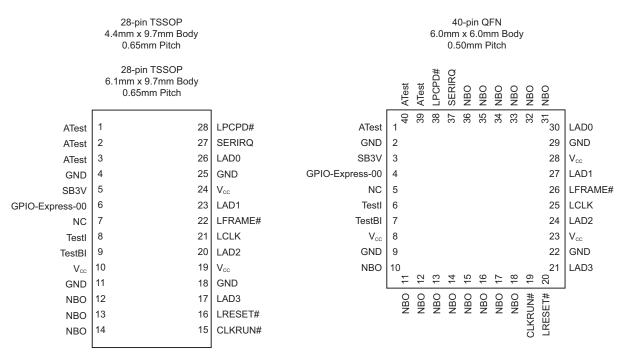
This is a summary document. The complete document is available under NDA. For more information, please contact your local Atmel sales office. This is a summary document.

## 1. Pin Configurations and Pinouts

Table 1-1. Pin Configurations

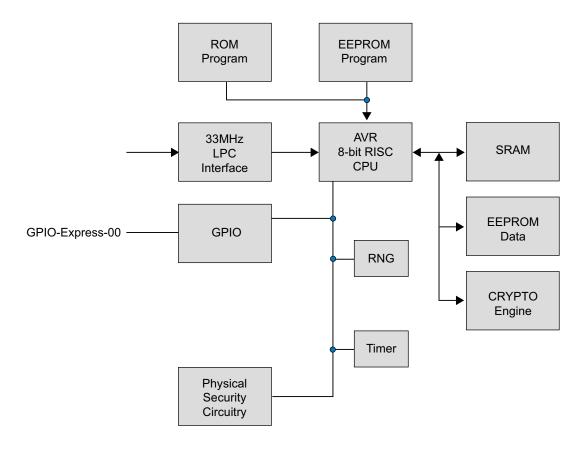
Pin name	Function		
V <sub>CC</sub>	3.3V Supply Voltage		
SB3V	Standby 3.3V Supply Voltage		
GND	Ground		
LRESET#	PCI Reset Input Active Low		
LAD0	LPC Command, Address, Data Line Input/Output		
LAD1	LPC Command, Address, Data Line Input/Output		
LAD2	LPC Command, Address, Data Line Input/Output		
LAD3	LPC Command, Address, Data Line Input/Output		
LCLK	33MHz PCI Clock Input		
LFRAME#	LPC FRAME Input		
CLKRUN#	PCI Clock Run Input/Output		
LPCPD#	LPC Power-Down Input		
SERIRQ	Serialized Interrupt Request Input/Output		
GPIO-Express-00	GPIO assigned to TPM_NV_INDEX_GPIO_00		
Testl	Test Input (Disabled)		
TestBI	Test Input (Disabled)		
ATest	Atmel Test Pin		
NC	No Connect		
NBO Not Bounded Out			

Table 1-2. Pinouts





## 2. Block Diagram



The TPM includes a hardware random number generator, including a FIPS-approved Pseudo Random Number Generator that is used for key generation and TCG protocol functions. The RNG is also available to the system to generate random numbers that may be needed during normal operation.

The chip uses a dynamic internal memory management scheme to store multiple RSA keys. Other than the standard TCG commands (TPM\_FlushSpecific, TPM\_Loadkey2), no system intervention is required to manage this internal key cache.

The TPM is offered to OEM and ODM manufacturers as a turnkey solution, including the firmware integrated on the chip. In addition, Atmel provides the necessary device driver software for integration into certain operating systems, along with BIOS drivers. Atmel will also provide manufacturing support software for use by OEMs and ODMs during initialization and verification of the TPM during board assembly.

Full documentation for TCG primitives can be found in the TCG TPM Main Specification, Parts 1 to 3, on the TCG Web site located at <a href="https://www.trustedcomputinggroup.org">https://www.trustedcomputinggroup.org</a>. TPM features specific to PC Client platforms are specified in the "TCG PC Client Specific TPM Interface Specification, Version 1.2", also available on the TCG web site. Implementation guidance for 32-bit PC platforms is outlined in the "TCG PC Client Specific Implementation Specification for Conventional BIOS for TCG Version 1.2", also available on the TCG website.



# 3. Ordering Information

Atmel Ordering Code	Package		Operating Range
AT97SC3204 <sup>(1)</sup>	28X1 (28-pin thin TSSOP)	Lead-free, RoHS	Commercial (0°C to 70°C)
AT97SC3204 <sup>(1)</sup>	40ML1 (40-pin QFN)	Leau-liee, Rons	Industrial (-40°C to 85°C)

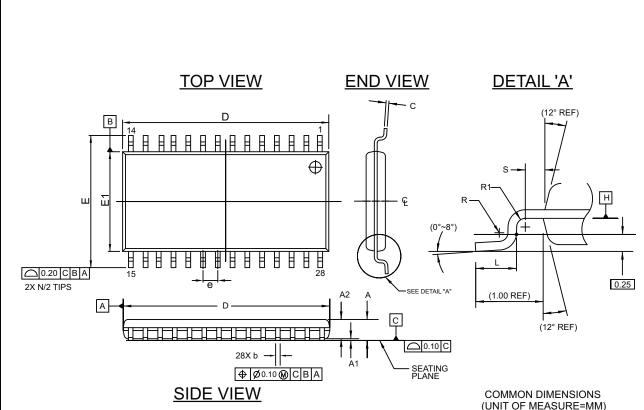
Note: 1. Please see the AT97SC3204 datasheet addendum for the complete catalog number ordering code.

	Package Type
28X1	28-lead, 4.4mm body width, Plastic Thin Shrink Small Outline (thin TSSOP)
40-pad 6.0 x 6.0x0.9mm body, 0.50mm pitch, Very-thin Quad Flat No Lead (VQFN)	



## 4. Package Drawings

### 4.1 28X1 — 28-lead Thin TSSOP

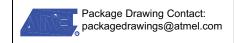


#### Note:

- 1. Refer to JEDEC drawing MO-153, variation AE
- Dimension D does not include mold flash, protrusions or gate burrs. Mold flash,protrusions or gate burrs shall not exceed 0.15mm per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side.
- 3. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.

(UNIT OF MEASURE=MM)				
SYMBOL	MIN	NOM	MAX	NOTE
А	-	-	1.10	
A1	0.05	-	0.15	
A2	0.85	0.90	0.95	
b	0.19	-	0.30	2
С	0.09	-	0.20	
D	9.60	9.70	9.80	1
Е		6.40BSC		
E1	4.30	4.40	4.50	1
е		0.65 BSC		
L	0.45	0.60	0.75	
R	0.09	-	-	
R1	0.09	-	-	
Q	0.20	_	_	

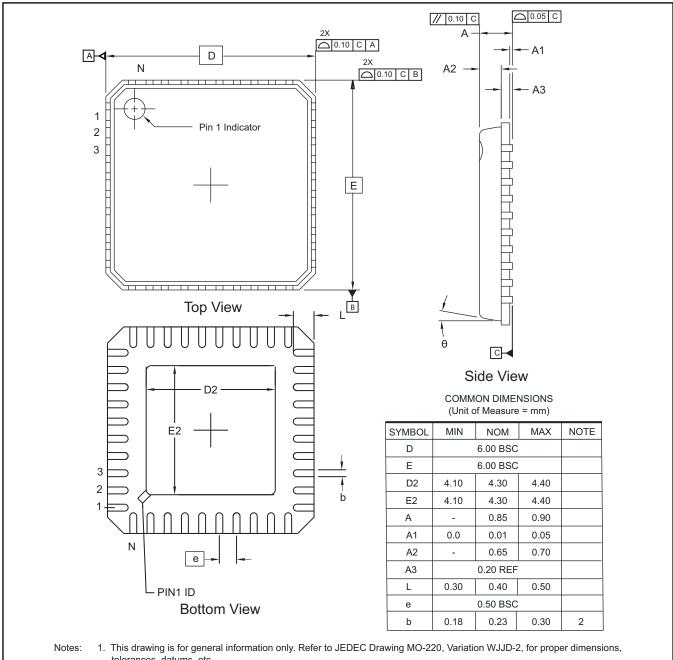
7/8/2011



TITLE	GPC	DRAWING NO.	REV.
28X1, 28-lead, 4.4mm Body Width, Plastic Thin Shrink Small Outline Package (TSSOP)	TFL	28X1	Α



#### 4.2 40ML1 — 40-pad VQFN



- tolerances, datums, etc.
- 2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area. 09/23/11



Package Drawing Contact: packagedrawings@atmel.com 40ML1, 40-pad 6.0 x 6.0x0.9 mm Body, 0.50 mm pitch, Very-Thin Quad Flat No Lead Package (VQFN) Punched

GPC	DRAWING NO.	REV.
ZJI	40ML1	D



# 5. Revision History

Doc. Rev.	Date	Comments		
5295DS	12/2012	Changed GPIO6 to GPIO-Express-00.  Updated package drawings 28A3 and 40ML1.  Updated package drawing 28A1 to 28X1.  Updated template and Atmel logos.		
5295CS	03/2011 Corrected header and footers.			
5295BS	10/2010	Added Industrial Grade support detail.		
5295AS	01/2008	Initial document release.		





#### **Atmel Corporation**

1600 Technology Drive San Jose, CA 95110 USA

**Tel:** (+1) (408) 441-0311 **Fax:** (+1) (408) 487-2600

www.atmel.com

#### **Atmel Asia Limited**

Unit 01-5 & 16, 19F BEA Tower, Millennium City 5 418 Kwun Tong Roa Kwun Tong, Kowloon

**Tel:** (+852) 2245-6100 **Fax:** (+852) 2722-1369

HONG KONG

## Atmel Munich GmbH

Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY

**Tel:** (+49) 89-31970-0 **Fax:** (+49) 89-3194621

## Atmel Japan G.K.

16F Shin-Osaki Kangyo Bldg 1-6-4 Osaki, Shinagawa-ku

Tokyo 141-0032

**JAPAN** 

**Tel:** (+81) (3) 6417-0300 **Fax:** (+81) (3) 6417-0370

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## Atmel AT97SC3204 and AT97SC3204T

## **Trusted Platform Module**

## ORDERING CODE ADDENDUM

## 1. Atmel AT97SC3204 Ordering Code Information

Ordering Code	Package	Description	Operation Range
AT97SC3204-X2A1A-10	(28-pin 4.4mm TSSOP)	Lead-free, RoHS v1.2 rev 116 LPC TPM with EK	Commercial (0°C to 70°C)
AT97SC3204-U2A1A-10	(28-pin 4.4mm TSSOP)	Lead-free, RoHS v1.2 rev 116 LPC TPM with EK	Industrial (-40°C to 85°C)
AT97SC3204-X2A1A-20	(28-pin 4.4mm TSSOP)	Lead-free, RoHS v1.2 rev 116 LPC TPM with signed EK	Commercial (0°C to 70°C)
AT97SC3204-U2A1A-20	(28-pin 4.4mm TSSOP)	Lead-free, RoHS v1.2 rev 116 LPC TPM with signed EK	Industrial (-40°C to 85°C)
AT97SC3204-X2MA-10	40ML1 (40-pin QFN)	Lead-free, RoHS v1.2 rev 116 LPC TPM with EK	Commercial (0°C to 70°C)
AT97SC3204-U2MA-10	40ML1 (40-pin QFN)	Lead-free, RoHS v1.2 rev 116 LPC TPM with EK	Industrial (-40°C to 85°C)
AT97SC3204-X2MA-20	40ML1 (40-pin QFN)	Lead-free, RoHS v1.2 rev 116 LPC TPM with signed EK	Commercial (0°C to 70°C)
AT97SC3204-U2MA-20	40ML1 (40-pin QFN)	Lead-free, RoHS v1.2 rev 116 LPC TPM with signed EK	Industrial (-40°C to 85°C)
AT97SC3204T-X2A1B-10	(28-pin 4.4mm TSSOP)	Lead-free, RoHS v1.2 rev 116 TWI (I <sup>2</sup> C) TPM with EK	Commercial (0°C to 70°C)
AT97SC3204T-U2A1B-10	(28-pin 4.4mm TSSOP)	Lead-free, RoHS v1.2 rev 116 TWI (I <sup>2</sup> C) TPM with EK	Industrial (-40°C to 85°C)
AT97SC3204T-X2MB-10	40ML1 (40-pin QFN)	Lead-free, RoHS v1.2 rev 116 TWI (I <sup>2</sup> C) TPM with EK	Commercial (0°C to 70°C)
AT97SC3204T-U2MB-10	40ML1 (40-pin QFN)	Lead-free, RoHS v1.2 rev 116 TWI (I <sup>2</sup> C) TPM with EK	Industrial (-40°C to 85°C)

## 2. Revision History

Doc. Rev.	Date	Comments	
8728B	07/2012	Update ordering codes and template.	
8728A	08/2010	Initial document release.	



#### **Atmel Corporation**

1600 Technology Drive San Jose, CA 95110 USA

**Tel:** (+1) (408) 441-0311 **Fax:** (+1) (408) 487-2600

www.atmel.com

#### **Atmel Asia Limited**

Unit 01-5 & 16, 19F BEA Tower, Millennium City 5 418 Kwun Tong Roa Kwun Tong, Kowloon

**Tel:** (+852) 2245-6100 **Fax:** (+852) 2722-1369

HONG KONG

## Atmel Munich GmbH

Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY

**Tel:** (+49) 89-31970-0 **Fax:** (+49) 89-3194621

## Atmel Japan G.K.

16F Shin-Osaki Kangyo Bldg 1-6-4 Osaki, Shinagawa-ku

Tokyo 141-0032

**JAPAN** 

**Tel:** (+81) (3) 6417-0300 **Fax:** (+81) (3) 6417-0370

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