HARRIS

IRFD120/121/122/123
IRFD120R/121R/122R/123R

N-Channel Power MOSFETs
Avalanche Energy Rated*

August 1991

Features

- 1.3A and 1.1A, 80V - 100V
- $r_{DS(on)}$ = 0.30Ω and 0.40Ω
- Single Pulse Avalanche Energy Rated*
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance

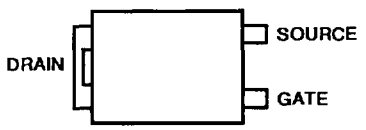
Description

The IRFD120, IRFD121, IRFD122, and IRFD123 are n-channel enhancement-mode silicon-gate power field-effect transistors. IRFD120R, IRFD121R, IRFD122R, and IRFD123R types are advanced power MOSFETs designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

The IRFD types are supplied in the 4-pin dual-in-line plastic package.

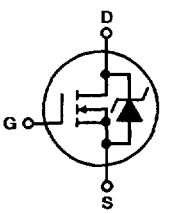
Package

4-PIN DIP
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

	IRFD120 IRFD120R	IRFD121 IRFD121R	IRFD122 IRFD122R	IRFD123 IRFD123R	UNITS
Drain-Source Voltage (1) ..... V_{DS}	100	80	100	80	V
Drain-Gate Voltage (R_{GS} = 20kΩ) (1) ..... V_{DGR}	100	80	100	80	V
Continuous Drain Current T_C = +25°C ..... I_D	1.3	1.3	1.1	1.1	A
Pulsed Drain Current ..... I_{DM}	5.2	5.2	4.4	4.4	A
Gate-Source Voltage ..... V_{GS}	±20	±20	±20	±20	V
Maximum Power Dissipation T_C = +25°C (See Figure 13) ..... P_D	1.0	1.0	1.0	1.0	W
Linear Derating Factor (See Figure 13)	0.008	0.008	0.008	0.008	W/°C
Inductive Current, Clamped ..... I_{LM} (See Figure 14, L = 100μH)	5.2	5.2	4.4	4.4	A
Single Pulse Avalanche Energy Rating (3) ..... E_{as}*	36	36	36	36	mJ
Operating and Storage Junction ..... T_J, T_{STG} Temperature Range	-55 to +150	-55 to +150	-55 to +150	-55 to +150	°C
Maximum Lead Temperature for Soldering ..... T_L (0.063" (1.6mm) from case for 10s)	300	300	300	300	°C

NOTES:

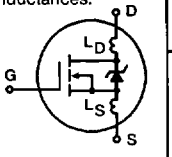
1. T_J = +25°C to +150°C.
2. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%.
3. V_{DD} = 25V, starting T_J = +25°C, L = 32mH, R_{GS} = 25Ω, I_{PEAK} = 1.3A. See Figure 15.

* R Suffix Types Only

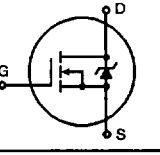
CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2315.1**

Electrical Characteristics T_C = +25°C, Unless Otherwise Specified

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage IRFD120/122, IRFD120R/122R	BV_{DSS}	V_{GS} = 0V, I_D = 250µA	100	-	-	V
IRFD121/123, IRFD121R/123R			80	-	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS} = V_{GS}, I_D = 250µA	2.0	-	4.0	V
Gate-Source Leakage Forward	I_{GSS}	V_{GS} = 20V	-	-	500	nA
Gate-Source Leakage Reverse	I_{GSS}	V_{GS} = -20V	-	-	-500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = Max Rating, V_{GS} = 0V	-	-	250	µA
		V_{DS} = Max Rating x 0.8, V_{GS} = 0V, T_C = +125°C	-	-	1000	µA
On-State Drain Current (Note 2) IRFD120/121, IRFD120R/121R	$I_{D(ON)}$	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, V_{GS} = 10V	1.3	-	-	A
IRFD122/123, IRFD122R/123R			1.1	-	-	A
Static Drain-Source On-State Resistance (Note 2) IRFD120/121, IRFD120R/121R	$r_{DS(ON)}$	V_{GS} = 10V, I_D = 0.6A	-	0.25	0.30	Ω
IRFD122/123, IRFD122R/123R			-	0.30	0.40	Ω
Forward Transconductance (Note 2)	g_{fs}	V_{DS} > $I_{D(ON)}$ x $r_{DS(ON)}$ Max, I_D = 0.6A	0.9	1.0	-	S(℧)
Input Capacitance	C_{ISS}	V_{GS} = 0V, V_{DS} = 25V, f = 1.0MHz See Figure 9	-	450	-	pF
Output Capacitance	C_{OSS}		-	200	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	50	-	pF
Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} \simeq 0.5BV_{DSS}$, I_D = 1.3A, R_G = 9.1Ω See Figure 16. (MOSFET switching times are essentially independent of operating temperature)	-	20	40	ns
Rise Time	t_r		-	35	70	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	50	100	ns
Fall Time	t_f		-	35	70	ns
Total Gate Charge (Gate-Source + Gate-Drain)	Q_g	V_{GS} = 10V, I_D = 1.3A, V_{DS} = 0.8 Max Rating. See Figure 17 for test circuit. (Gate charge is essentially independent of operating temperature.)	-	11	15	nC
Gate-Source Charge	Q_{gs}		-	6.0	-	nC
Gate-Drain ("Miller") Charge	Q_{gd}		-	5.0	-	nC
Internal Drain Inductance	L_D	Measured from the drain lead, 2.0mm (0.08 in.) from package to center of die. Modified MOSFET symbol showing the internal device inductances. 	-	4.0	-	nH
Internal Source Inductance	L_S	Measured from the source lead, 2.0mm (0.08") from package to source bonding pad.	-	6.0	-	nH
Junction-to-Ambient	$R_{\theta JA}$	Free air operation	-	-	120	°C/W

Source Drain Diode Ratings and Characteristics

Continuous Source Current (Body Diode)	I_S	Modified MOSFET symbol showing the integral reverse P-N junc. rectifier. 	-	-	1.3	A
Pulse Source Current (Body Diode) (Note 3)	I_{SM}		-	-	5.2	A
Diode Forward Voltage (Note 2)	V_{SD}	T_J = +25°C, I_S = 1.3A, V_{GS} = 0V	-	-	2.5	V
Reverse Recovery Time	t_{rr}	T_J = +150°C, I_F = 1.3A, dI_F/dt = 100A/µs	-	280	-	ns
Reverse Recovered Charge	Q_{RR}	T_J = +150°C, I_F = 1.3A, dI_F/dt = 100A/µs	-	1.6	-	µC
Forward Turn-on Time	t_{ON}	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.	-	-	-	-

NOTES:

1. T_J = +25°C to +150°C
2. Pulse Test: Pulse width ≤ 300µs, Duty Cycle ≤ 2%
3. V_{DD} = 25V, starting T_J = +25°C, L = 32mH, R_{GS} = 25Ω, I_{PEAK} = 1.3A. (See Figure 15.)

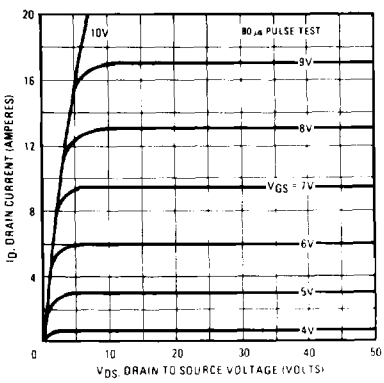


Fig. 1 – Typical Output Characteristics

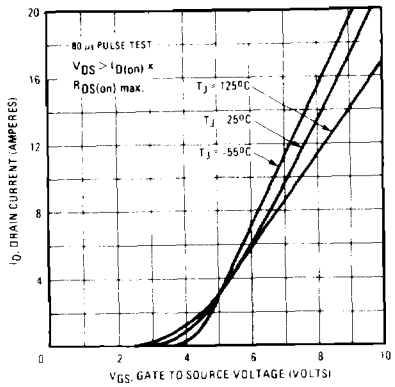


Fig. 2 – Typical Transfer Characteristics

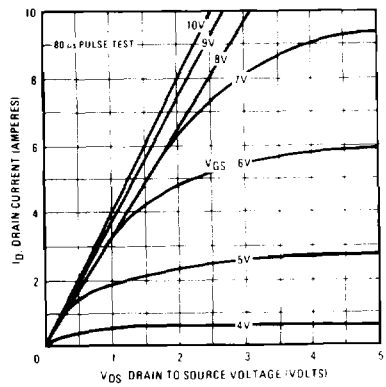


Fig. 3 – Typical Saturation Characteristics

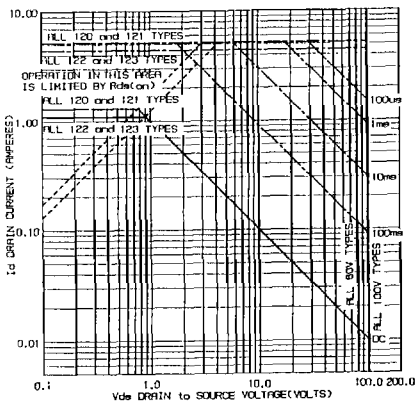


Fig. 4 – Maximum Safe Operating Area

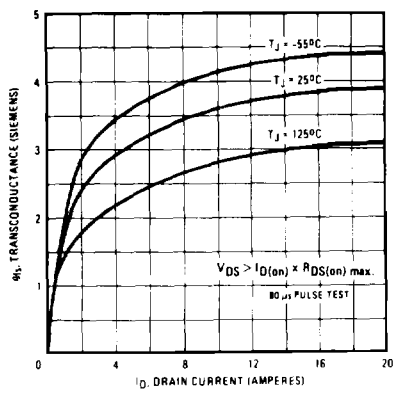


Fig. 5 – Typical Transconductance Vs. Drain Current

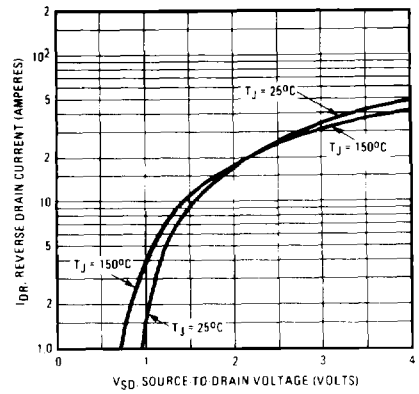


Fig. 6 – Typical Source-Drain Diode Forward Voltage

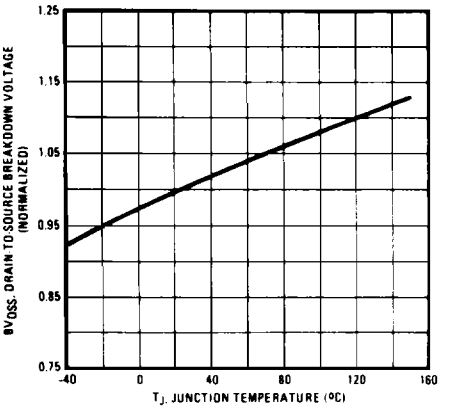


Fig. 7 – Breakdown Voltage Vs. Temperature

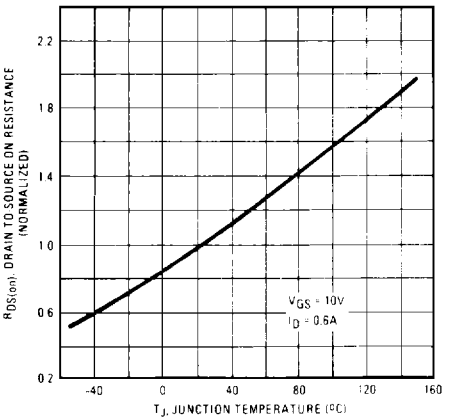


Fig. 8 – Normalized On-Resistance Vs. Temperature

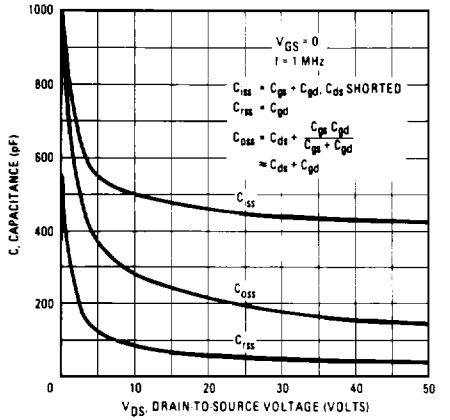


Fig. 9 – Typical Capacitance Vs. Drain-to-Source Voltage

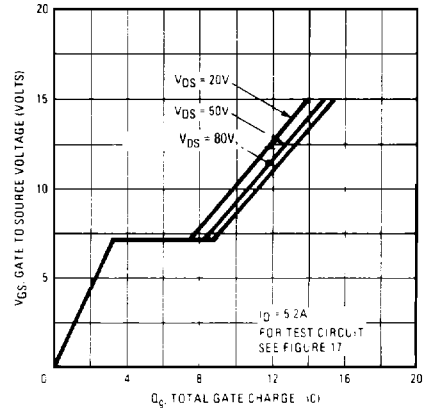


Fig. 10 – Typical Gate Charge Vs. Gate-to-Source Voltage

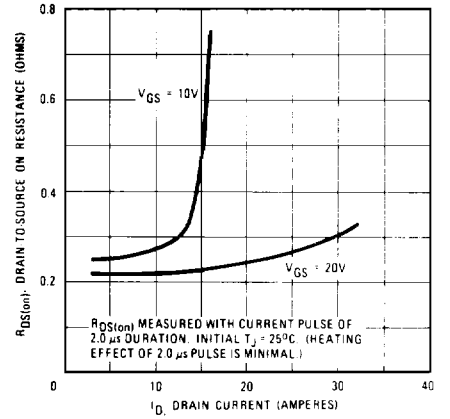


Fig. 11 – Typical On-Resistance Vs. Drain Current

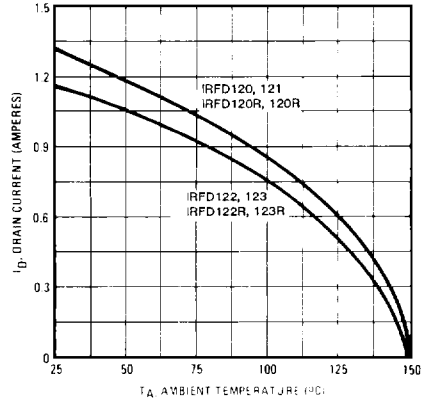


Fig. 12 – Maximum Drain Current Vs. Case Temperature

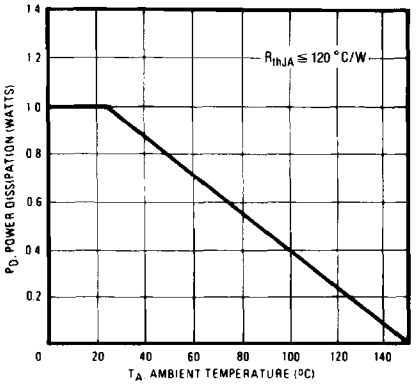


Fig. 13 - Power Vs. Temperature Derating Curve

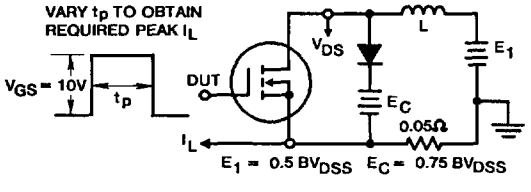


Fig. 14a - Clamped Inductive Test Circuit

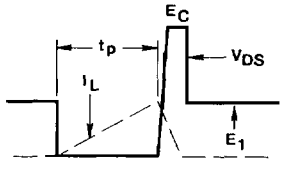


Fig. 14b - Clamped Inductive Waveforms

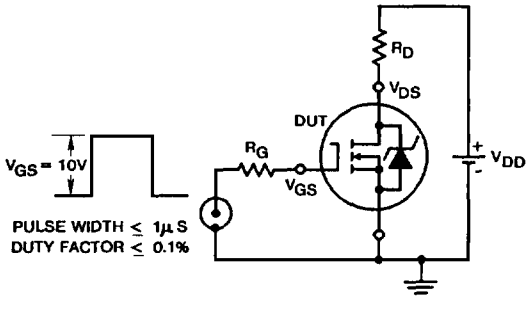


Fig. 16 - Switching Time Test Circuit

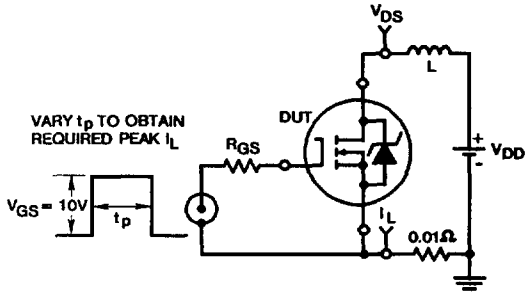


Fig. 15a - Unclamped Energy Test Circuit

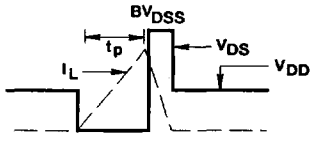


Fig. 15b - Unclamped Energy Waveforms

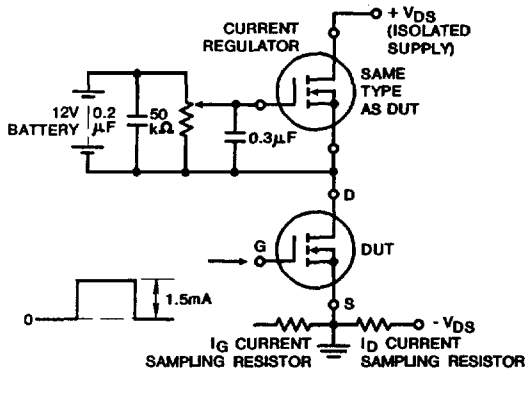


Fig. 17 - Gate Charge Test Circuit