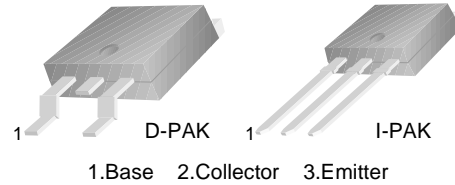


MJD127

D-PAK for Surface Mount Applications

- High DC Current Gain
- Built-in a Damper Diode at E-C
- Lead Formed for Surface Mount Applications (No Suffix)
- Straight Lead (I-PAK, "- I" Suffix)
- Electrically Similar to Popular TIP127
- Complement to MJD122

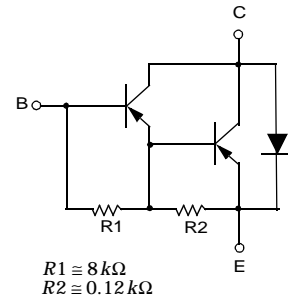


PNP Silicon Darlington Transistor

Absolute Maximum Ratings $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector-Base Voltage	- 100	V
V_{CEO}	Collector-Emitter Voltage	- 100	V
V_{EBO}	Emitter-Base Voltage	- 5	V
I_C	Collector Current (DC)	- 8	A
I_{CP}	Collector Current (Pulse)	- 16	A
I_B	Base Current	- 120	mA
P_C	Collector Dissipation ($T_C=25^\circ\text{C}$)	20	W
	Collector Dissipation ($T_a=25^\circ\text{C}$)	1.75	W
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{STG}	Storage Temperature	- 65 ~ 150	$^\circ\text{C}$

Equivalent Circuit



Electrical Characteristics $T_C=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
$V_{CEO(sus)}$	*Collector-Emitter Sustaining Voltage	$I_C = -30\text{mA}, I_B = 0$	- 100		V
I_{CEO}	Collector Cut-off Current	$V_{CE} = -50\text{V}, I_B = 0$		- 10	μA
I_{CBO}	Collector Cut-off Current	$V_{CB} = -100\text{V}, I_E = 0$		- 10	μA
I_{EBO}	Emitter Cut-off Current	$V_{EB} = -5\text{V}, I_C = 0$		- 2	mA
h_{FE}	*DC Current Gain	$V_{CE} = -4\text{V}, I_C = -4\text{A}$ $V_{CE} = -4\text{V}, V_{EB} = -8\text{A}$	1000 100	12K	
$V_{CE(sat)}$	*Collector-Emitter Saturation Voltage	$I_C = -4\text{A}, I_B = -16\text{mA}$		- 2	V
		$I_C = -8\text{A}, I_B = -80\text{mA}$		- 4	V
$V_{BE(sat)}$	*Base-Emitter Saturation Voltage	$I_C = -8\text{A}, I_B = -80\text{mA}$		- 4.5	V
$V_{BE(on)}$	*Base-Emitter ON Voltage	$V_{CE} = -4\text{V}, I_C = -4\text{A}$		- 2.8	V
C_{ob}	Output Capacitance	$V_{CB} = -10\text{V}, I_E = 0$ $f = 0.1\text{MHz}$		300	pF

* Pulse Test: $PW \leq 300\mu\text{s}$, Duty Cycles $\leq 2\%$

Typical Characteristics

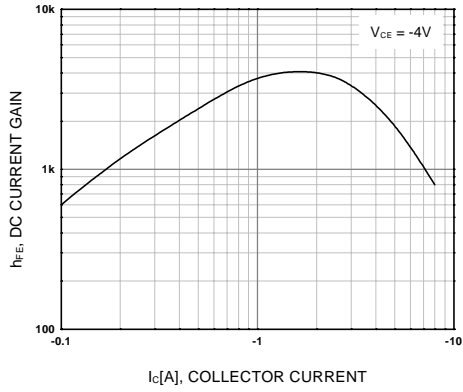


Figure 1. DC current Gain

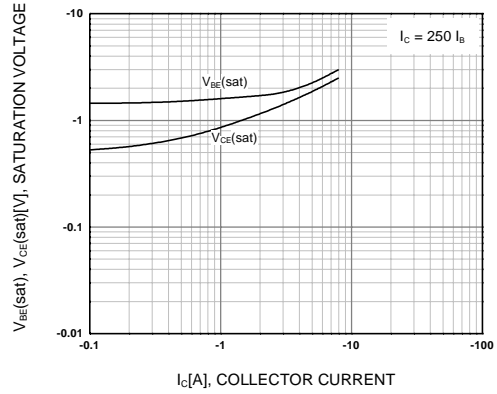


Figure 2. Base-Emitter Saturation Voltage
Collector-Emitter Saturation Voltage

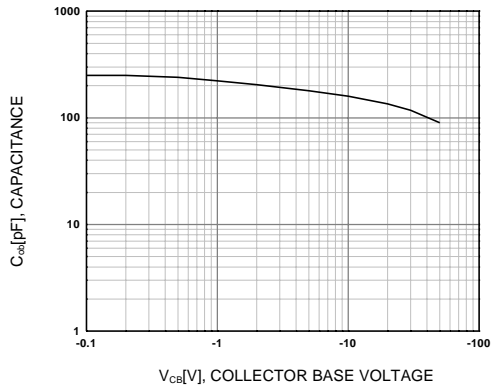


Figure 3. Collector Output Capacitance

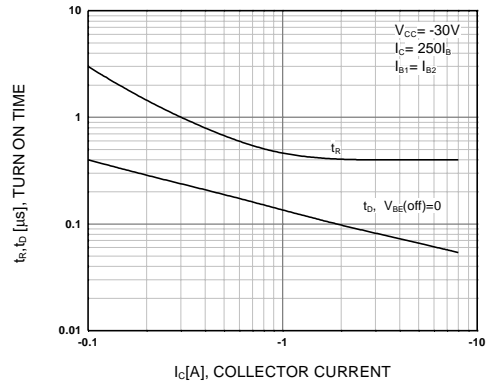


Figure 4. Turn On Time

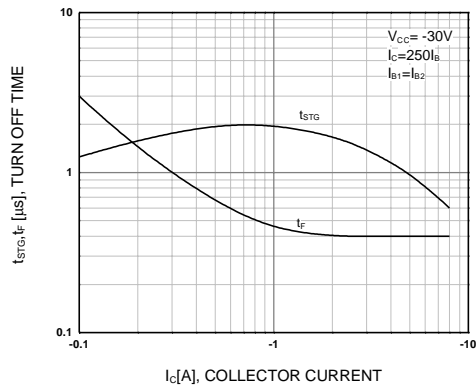


Figure 5. Turn Off Time

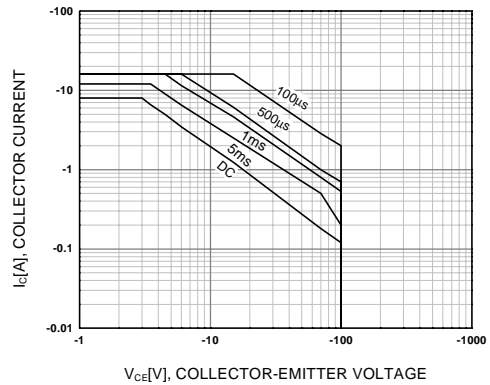


Figure 6. Safe Operating Area

Typical Characteristic (Continued)

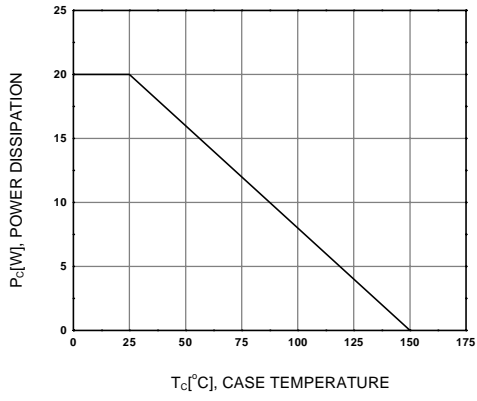
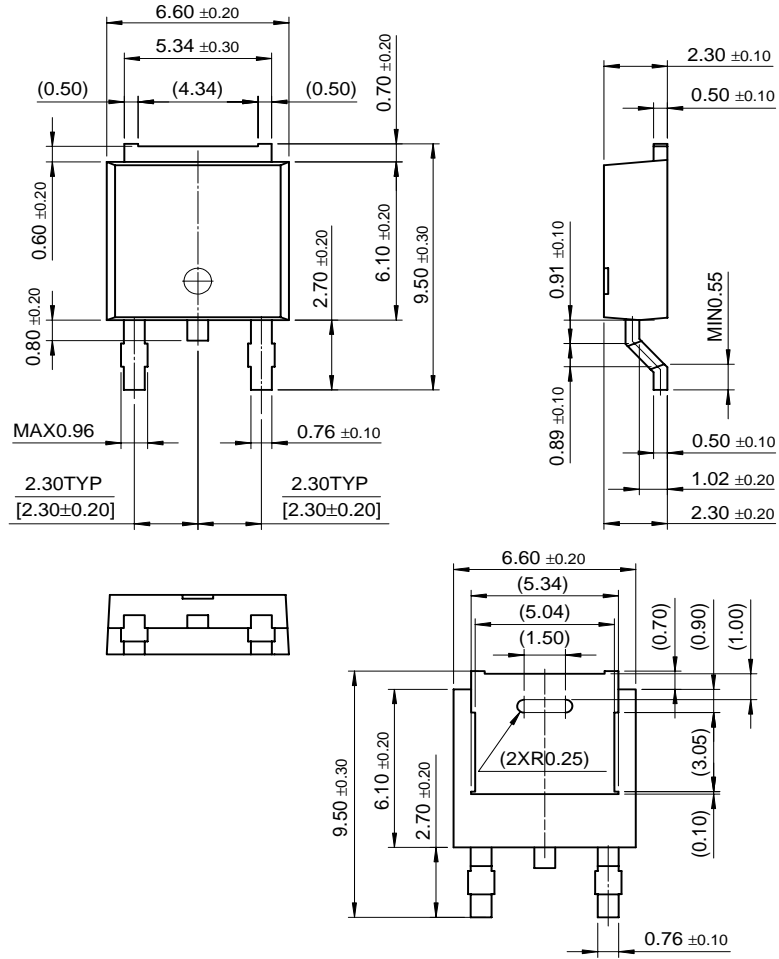


Figure 7. Power Derating

Package Dimensions

D-PAK



Dimensions in Millimeters

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MJD127

PNP Silicon Darlington Transistor

Contents

[Features](#) | [Applications](#) | [Product status/pricing/packaging](#)

Features

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Applications

D-PAK for Surface Mount

[back to top](#)

Product status/pricing/packaging

Product	Product status	Package type	Leads	Packing method
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