60V Synchronous Switching Regulator Controller

FEATURES

- **High Voltage Operation: Up to 60V**
- **Large 1Ω Gate Drivers (with 5V Supply)**
- **No Current Sense Resistor Required**
- **Step-Up or Step-Down DC/DC Converter**
- Dual N-Channel MOSFET Synchronous Drive
- Excellent Line and Load Transient Response
- Programmable Constant Frequency: 100kHz to 600kHz
- ±1% Reference Accuracy
- Synchronizable up to 600kHz
- Selectable Pulse Skip Mode Operation
- Low Shutdown Current: 25µA Typ
- Programmable Current Limit
- Undervoltage Lockout
- Programmable Soft-Start
- 16-Pin Narrow SSOP and 28-Pin SSOP Packages

APPLICATIONS

- 48V Telecom and Base Station Power Supplies
- Networking Equipment, Servers
- Automotive and Industrial Control

DESCRIPTION

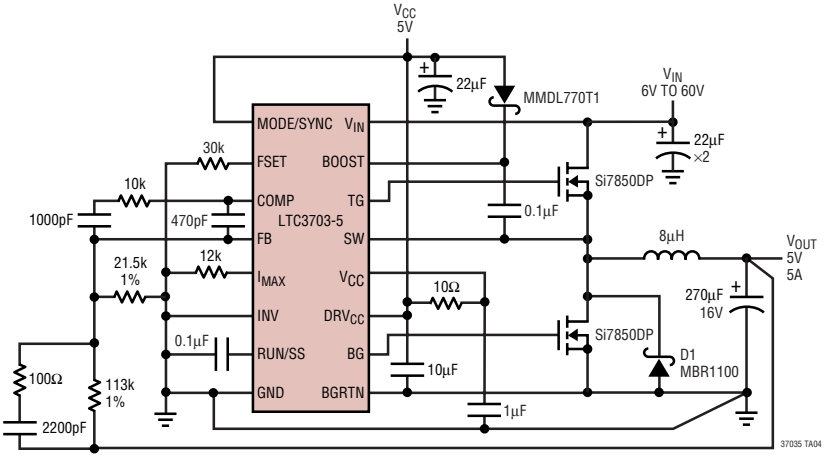
The LTC®3703-5 is a synchronous step-down switching regulator controller that can directly step-down voltages from up to 60V input, making it ideal for telecom and automotive applications. The LTC3703-5 drives external logic level N-channel MOSFETs using a constant frequency (up to 600kHz), voltage mode architecture.

A precise internal reference provides 1% DC accuracy. A high bandwidth error amplifier and patented* line feed forward compensation provide very fast line and load transient response. Strong 1Ω gate drivers allow the LTC3703-5 to drive multiple MOSFETs for higher current applications. The operating frequency is user programmable from 100kHz to 600kHz and can also be synchronized to an external clock for noise-sensitive applications. Current limit is programmable with an external resistor and utilizes the voltage drop across the synchronous MOSFET to eliminate the need for a current sense resistor. For applications requiring up to 100V operation, refer to the LTC3703 data sheet.

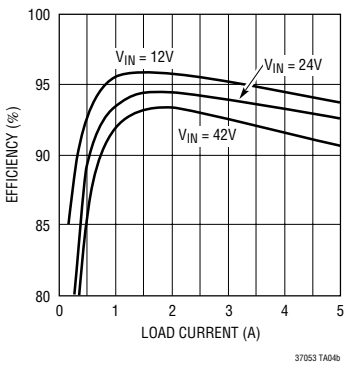
PARAMETER	LTC3703-5	LTC3703
Maximum V_{IN}	60V	100V
MOSFET Gate Drive	4.5V to 15V	9.3V to 15V
V_{CC} UV^+	3.7V	8.7V
V_{CC} UV^-	3.1V	6.2V

TYPICAL APPLICATION

High Efficiency High Voltage Step-Down Converter



Efficiency vs Load Current



ABSOLUTE MAXIMUM RATINGS (Note 1)

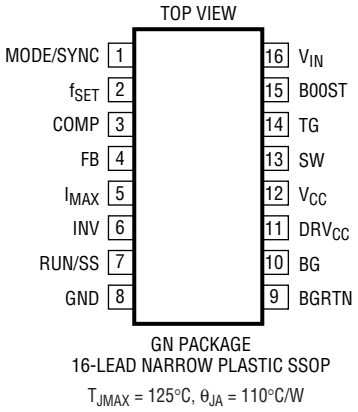
Supply Voltages
- V_{CC}, DRV_{CC} ..... –0.3V to 15V
- (DRV_{CC} – BGRTN), (BOOST – SW) ..... –0.3V to 15V
- BOOST (Continuous) ..... –0.3V to 85V
- BOOST (400ms) ..... –0.3V to 95V
- BGRTN ..... –5V to 0V

V_{IN} Voltage (Continuous) ..... –0.3V to 70V
V_{IN} Voltage (400ms) ..... –0.3V to 80V
SW Voltage (Continuous) ..... –1V to 70V
SW Voltage (400ms) ..... –1V to 80V
Run/SS Voltage ..... –0.3V to 5V
MODE/SYNC, INV Voltages ..... –0.3V to 15V
f_{SET}, FB, I_{MAX}, COMP Voltages ..... –0.3V to 3V
Driver Outputs
- TG ..... SW – 0.3V to BOOST + 0.3V
- BG ..... BGRTN – 0.3V to DRV_{CC} + 0.3V

Peak Output Current <10µs BG,TG 5A
Operating Temperature Range (Note 2)
- LTC3703E-5 ..... –40°C to 85°C
- LTC3703I-5 ..... –40°C to 125°C

Junction Temperature (Notes 3, 7) ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



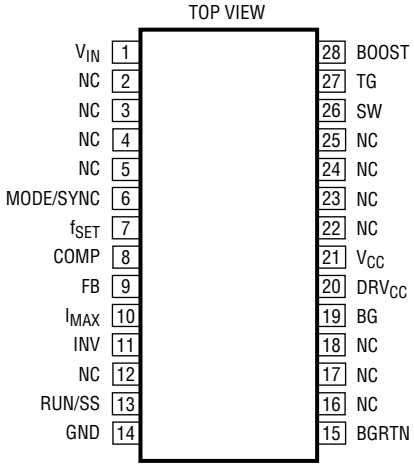
GN PACKAGE
16-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 110°C/W

ORDER PART NUMBER

LTC3703EGN-5
LTC3703IGN-5

GN PART MARKING

37035
3703I5



G PACKAGE
28-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER PART NUMBER

LTC3703EG-5
LTC3703IG-5

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = DRV_{CC} = V_{BOOST} = V_{IN} = 5V, $V_{MODE/SYNC}$ = V_{INV} = V_{SW} = BGRTN = 0V, RUN/SS = I_{MAX} = open, R_{SET} = 25k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}, DRV_{CC}	V_{CC}, DRV_{CC} Supply Voltage		●	4.1		15	V
V_{IN}	V_{IN} Pin Voltage		●			60	V
I_{CC}	V_{CC} Supply Current	V_{FB} = 0V	●		1.7	2.5	mA
		RUN/SS = 0V			25	40	µA
I_{DRVCC}	DRV_{CC} Supply Current	(Note 5)			0	5	µA
		RUN/SS = 0V			0	5	µA
I_{BOOST}	BOOST Supply Current	(Note 5) RUN/SS = 0V	●		360 0	500 5	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = DRV_{CC} = V_{BOOST} = V_{IN} = 5V, $V_{MODE/SYNC}$ = V_{INV} = V_{SW} = BGRTN = 0V, RUN/SS = I_{MAX} = open, R_{SET} = 25k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{FB}	Feedback Voltage	(Note 4)	 ●	0.792 0.788	0.800	0.808 0.812	V V
$\Delta V_{FB, LINE}$	Feedback Voltage Line Regulation	5V < V_{CC} < 15V (Note 4)	●		0.007	0.05	%/V
$\Delta V_{FB, LOAD}$	Feedback Voltage Load Regulation	1V < V_{COMP} < 2V (Note 4)	●		0.01	0.1	%
$V_{MODE/SYNC}$	MODE/SYNC Threshold	MODE/SYNC Rising		0.75	0.8	0.87	V
$\Delta V_{MODE/SYNC}$	MODE/SYNC Hysteresis				20		mV
$I_{MODE/SYNC}$	MODE/SYNC Current	0 ≤ $V_{MODE/SYNC}$ ≤ 15V			0	1	µA
V_{INV}	Invert Threshold			1	1.5	2	V
I_{INV}	Invert Current	0 ≤ V_{INV} ≤ 15V			0	1	µA
I_{VIN}	V_{IN} Sense Input Current	V_{IN} = 60V RUN/SS = 0V, V_{IN} = 10V			80 0	130 1	µA µA
I_{MAX}	I_{MAX} Source Current	V_{IMAX} = 0V		10.5	12	13.5	µA
$V_{OS, IMAX}$	V_{IMAX} Offset Voltage	$\|V_{SW}\| - V_{IMAX}$ at $I_{RUN/SS}$ = 0µA		–25	10	55	mV
$V_{RUN/SS}$	Shutdown Threshold			0.7	0.9	1.2	V
$I_{RUN/SS}$	RUN/SS Source Current	RUN/SS = 0V		2.3	3.8	5.3	µA
	Maximum RUN/SS Sink Current	$\|V_{SW}\| - V_{IMAX}$ > 100mV		9	17	25	µA
V_{UV}	Undervoltage Lockout	V_{CC} Rising V_{CC} Falling Hysteresis	● ● ●	3.4 2.8 0.45	3.7 3.1 0.65	4.1 3.4 0.85	V V V
Oscillator							
f_{OSC}	Oscillator Frequency	R_{SET} = 25kΩ		270	300	330	kHz
f_{SYNC}	External Sync Frequency Range			100		600	kHz
$t_{ON, MIN}$	Minimum On-Time				200		ns
DC_{MAX}	Maximum Duty Cycle	f < 200kHz		89	93	96	%
Driver							
$I_{BG, PEAK}$	BG Driver Peak Source Current			0.75	1		A
$R_{BG, SINK}$	BG Driver Pull-Down $R_{DS, ON}$	(Note 8)			1.2	1.8	Ω
$I_{TG, PEAK}$	TG Driver Peak Source Current			0.75	1		A
$R_{TG, SINK}$	TG Driver Pull-Down $R_{DS, ON}$	(Note 8)			1.2	1.8	Ω
Feedback Amplifier							
A_{VOL}	Op Amp DC Open Loop Gain	(Note 4)		74	85		dB
f_U	Op Amp Unity Gain Crossover Frequency	(Note 6)			25		MHz
I_{FB}	FB Input Current	0 ≤ V_{FB} ≤ 3V			0	1	µA
I_{COMP}	COMP Sink/Source Current			±5	±10		mA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LTC3703-5 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3703I-5 is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

LTC3703-5: $T_J = T_A + (P_D \bullet 100\ °C/W)$ G Package

Note 4: The LTC3703-5 is tested in a feedback loop that servos V_{FB} to the reference voltage with the COMP pin forced to a voltage between 1V and 2V.

Note 5: The dynamic input supply current is higher due to the power MOSFET gate charging being delivered at the switching frequency ($Q_G \bullet f_{OSC}$).

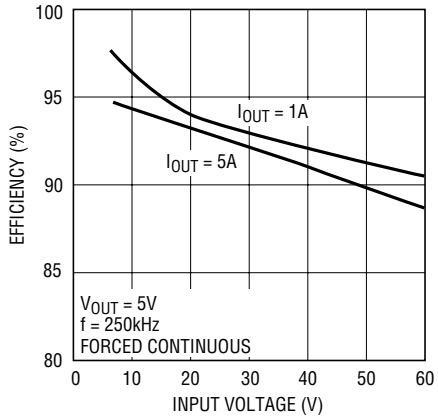
Note 6: Guaranteed by design. Not subject to test.

Note 7: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

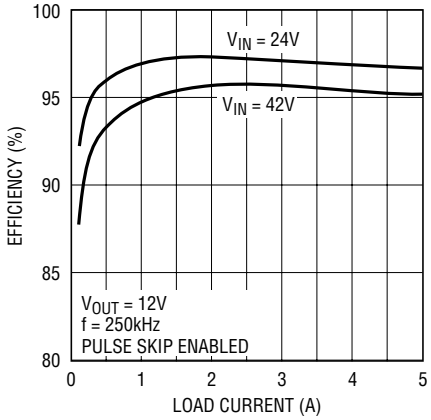
Note 8: $R_{DS(ON)}$ guaranteed by correlation to wafer level measurement.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C (unless otherwise noted).

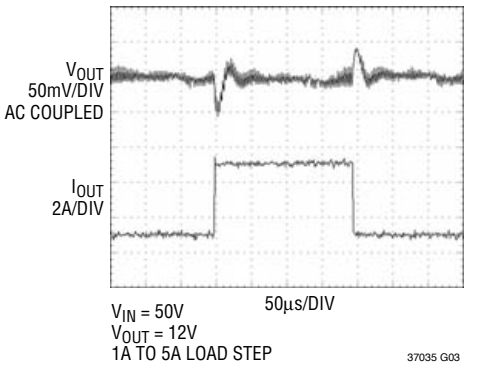
Efficiency vs Input Voltage



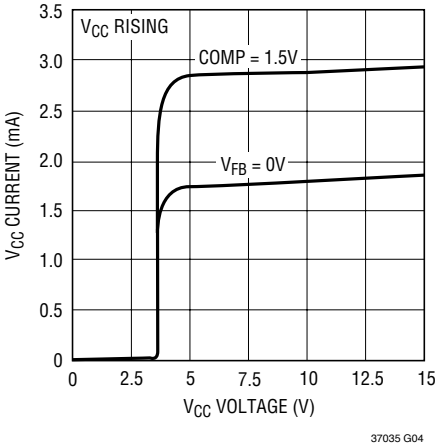
Efficiency vs Load Current



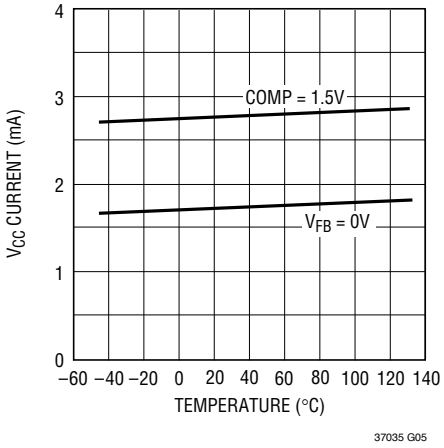
Load Transient Response



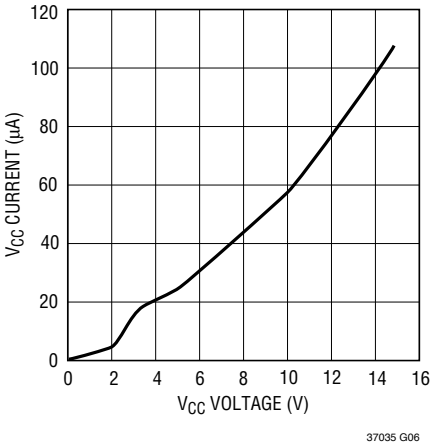
V_{CC} Current vs V_{CC} Voltage



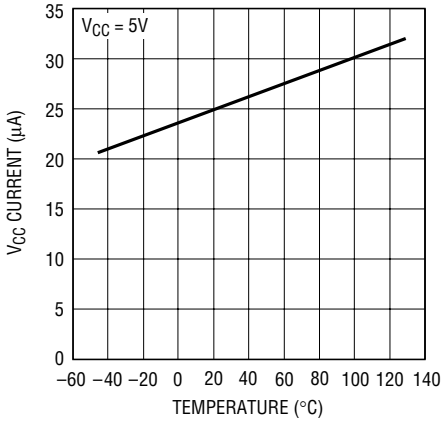
V_{CC} Current vs Temperature



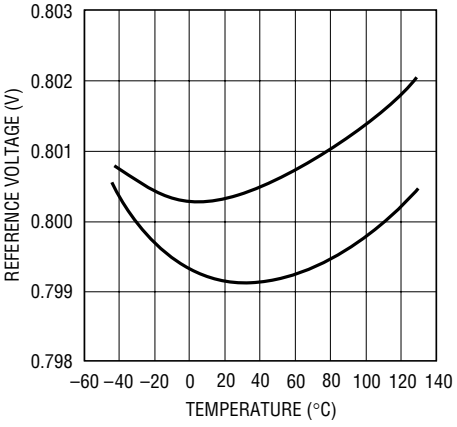
V_{CC} Shutdown Current vs V_{CC} Voltage



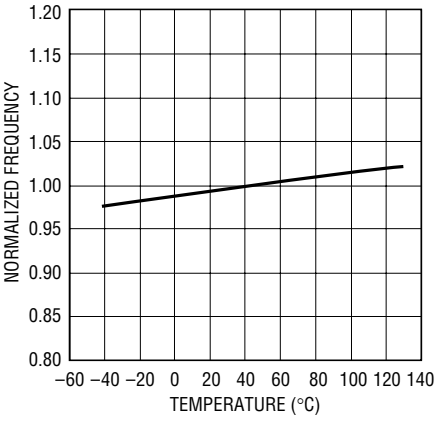
V_{CC} Shutdown Current vs Temperature



Reference Voltage vs Temperature

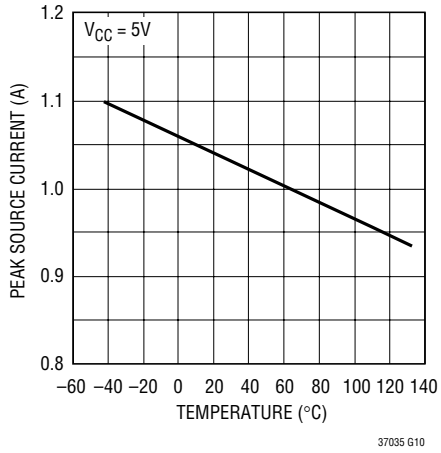


Normalized Frequency vs Temperature

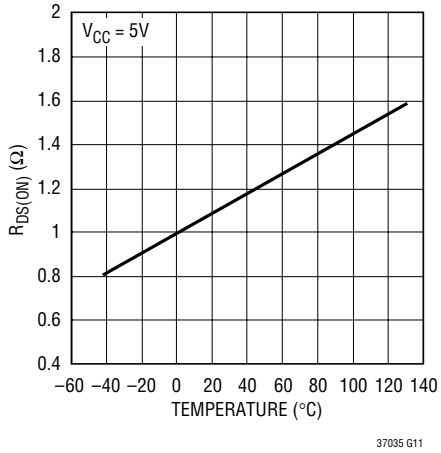


TYPICAL PERFORMANCE CHARACTERISTICS

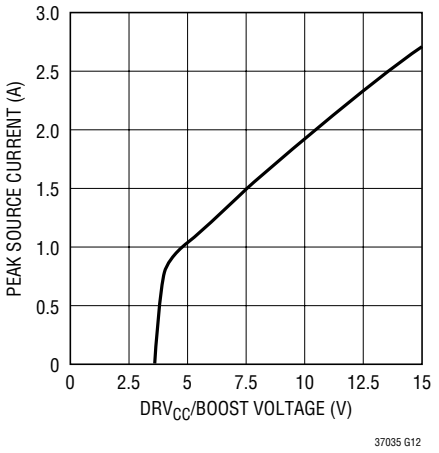
Driver Peak Source Current vs Temperature



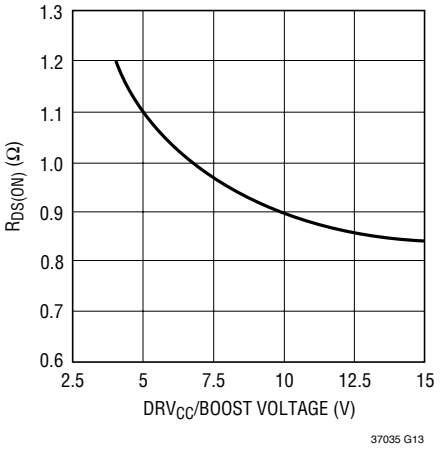
Driver Pull-Down $R_{DS(ON)}$ vs Temperature



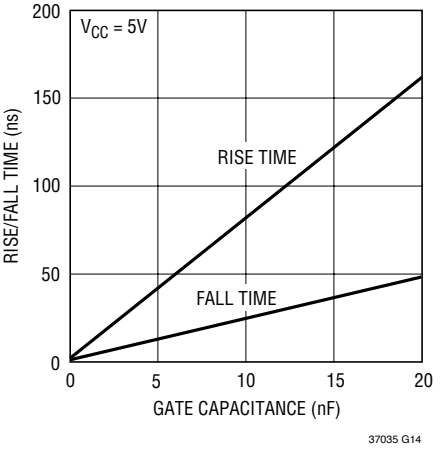
Driver Peak Source Current vs Supply Voltage



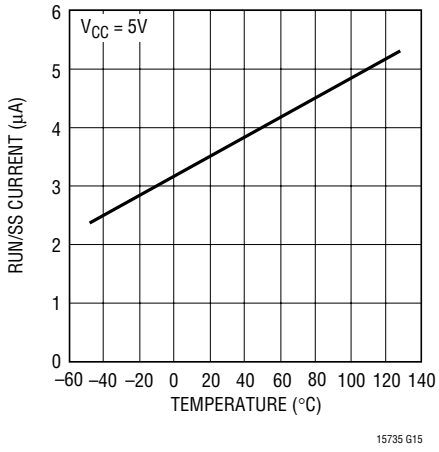
Driver Pull-Down $R_{DS(ON)}$ vs Supply Voltage



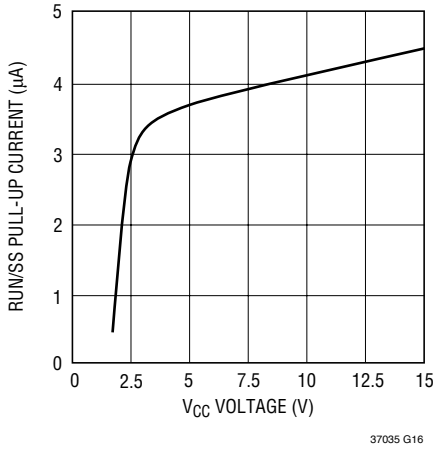
Rise/Fall Time vs Gate Capacitance



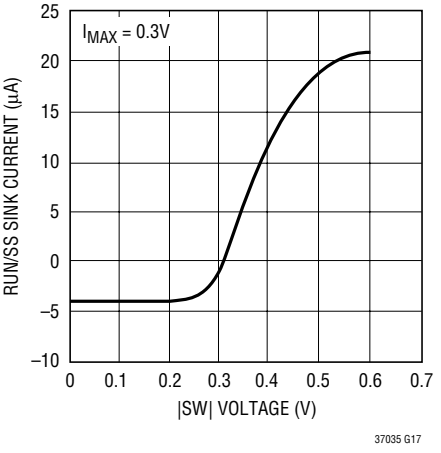
RUN/SS Pull-Up Current vs Temperature



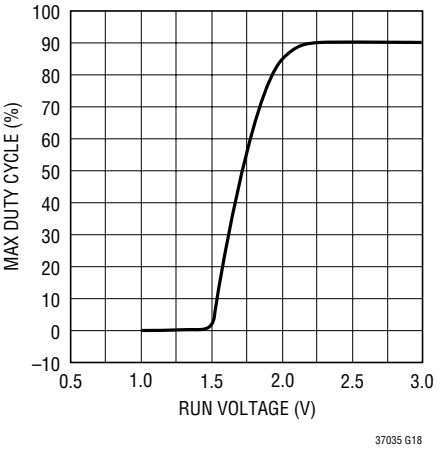
RUN/SS Pull-Up Current vs V_{CC} Voltage



RUN/SS Sink Current vs SW Voltage

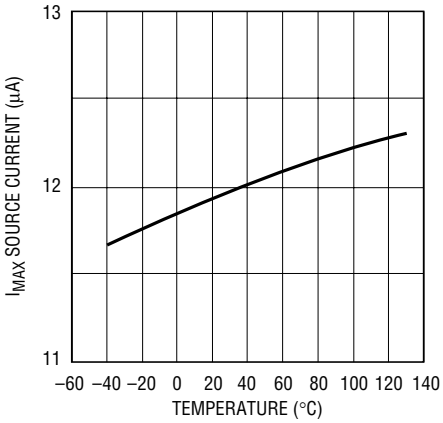


Max % DC vs RUN/SS Voltage



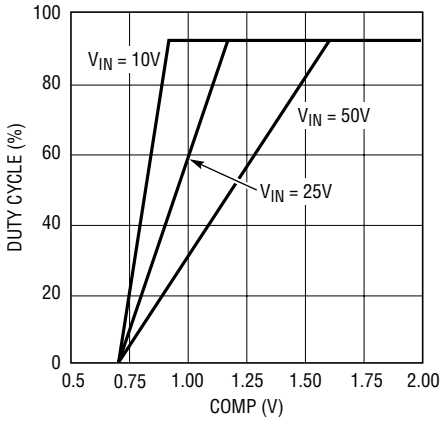
TYPICAL PERFORMANCE CHARACTERISTICS

I_{MAX} Current vs Temperature



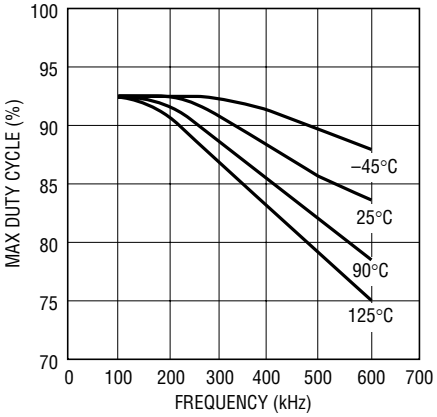
37035 G19

% Duty Cycle vs COMP Voltage



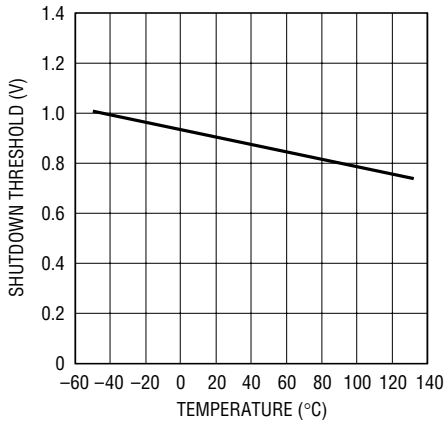
37035 G20

Max % DC vs Frequency and Temperature



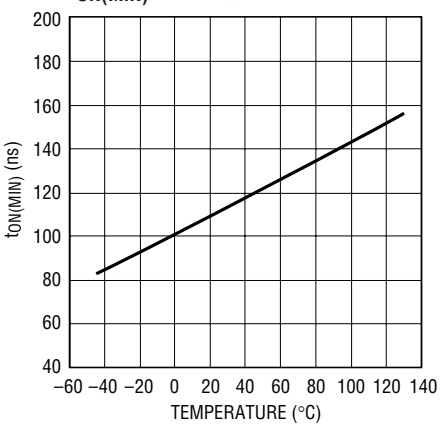
37035 G21

Shutdown Threshold vs Temperature



37035 G22

$t_{ON(MIN)}$ vs Temperature



37035 G23

PIN FUNCTIONS (GN16/G28)

MODE/SYNC (Pin 1/Pin 6): Pulse Skip Mode Enable/Sync Pin. This multifunction pin provides Pulse Skip Mode enable/disable control and an external clock input for synchronization of the internal oscillator. Pulling this pin below 0.8V or to an external logic-level synchronization signal disables Pulse Skip Mode operation and forces continuous operation. Pulling the pin above 0.8V enables Pulse Skip Mode operation. This pin can also be connected to a feedback resistor divider from a secondary winding on the inductor to regulate a second output voltage.

f_{SET} (Pin 2/Pin 7): Frequency Set. A resistor connected to this pin sets the free running frequency of the internal oscillator. See applications section for resistor value selection details.

COMP (Pin 3/Pin 8): Loop Compensation. This pin is connected directly to the output of the internal error amplifier. An RC network is used at the COMP pin to compensate the feedback loop for optimal transient response.

FB (Pin 4/Pin 9): Feedback Input. Connect FB through a resistor divider network to V_{OUT} to set the output voltage. Also connect the loop compensation network from COMP to FB.

I_{MAX} (Pin 5/Pin 10): Current Limit Set. The I_{MAX} pin sets the current limit comparator threshold. If the voltage drop across the bottom MOSFET exceeds the magnitude of the voltage at I_{MAX}, the controller goes into current limit. The I_{MAX} pin has an internal 12µA current source, allowing the current threshold to be set with a single external resistor to ground. See the Current Limit Programming section for more information on choosing R_{IMAX}.

INV (Pin 6/Pin 11): Top/Bottom Gate Invert. Pulling this pin above 2V sets the controller to operate in step-up (boost) mode with the TG output driving the synchronous MOSFET and the BG output driving the main switch. Below 1V, the controller will operate in step-down (buck) mode.

RUN/SS (Pin 7/Pin 13): Run/Soft-Start. Pulling RUN/SS below 0.9V will shut down the LTC3703-5, turn off both of the external MOSFET switches and reduce the quiescent supply current to 25µA. A capacitor from RUN/SS to ground will control the turn-on time and rate of rise of the output voltage at power-up. An internal 4µA current source pull-up at the RUN/SS pin sets the turn-on time at approximately 750ms/µF.

GND (Pin 8/Pin 14): Ground Pin.

BGRTN (Pin 9/Pin 15): Bottom Gate Return. This pin connects to the source of the pull-down MOSFET in the BG driver and is normally connected to ground. Connecting a negative supply to this pin allows the synchronous MOSFET's gate to be pulled below ground to help prevent false turn-on during high dV/dt transitions on the SW node. See the Applications Information section for more details.

BG (Pin 10/Pin 19): Bottom Gate Drive. The BG pin drives the gate of the bottom N-channel synchronous switch MOSFET. This pin swings from BGRTN to DRV_{CC}.

DRV_{CC} (Pin 11/Pin 20): Driver Power Supply Pin. DRV_{CC} provides power to the BG output driver. This pin should be connected to a voltage high enough to fully turn on the external MOSFETs, normally 4.5V to 15V for logic level threshold MOSFETs. DRV_{CC} should be bypassed to BGRTN with a 10µF, low ESR (X5R or better) ceramic capacitor.

V_{CC} (Pin 12/Pin 21) : Main Supply Pin. All internal circuits except the output drivers are powered from this pin. V_{CC} should be connected to a low noise power supply voltage between 4.5V and 15V and should be bypassed to GND (Pin 8) with at least a 0.1µF capacitor in close proximity to the LTC3703-5.

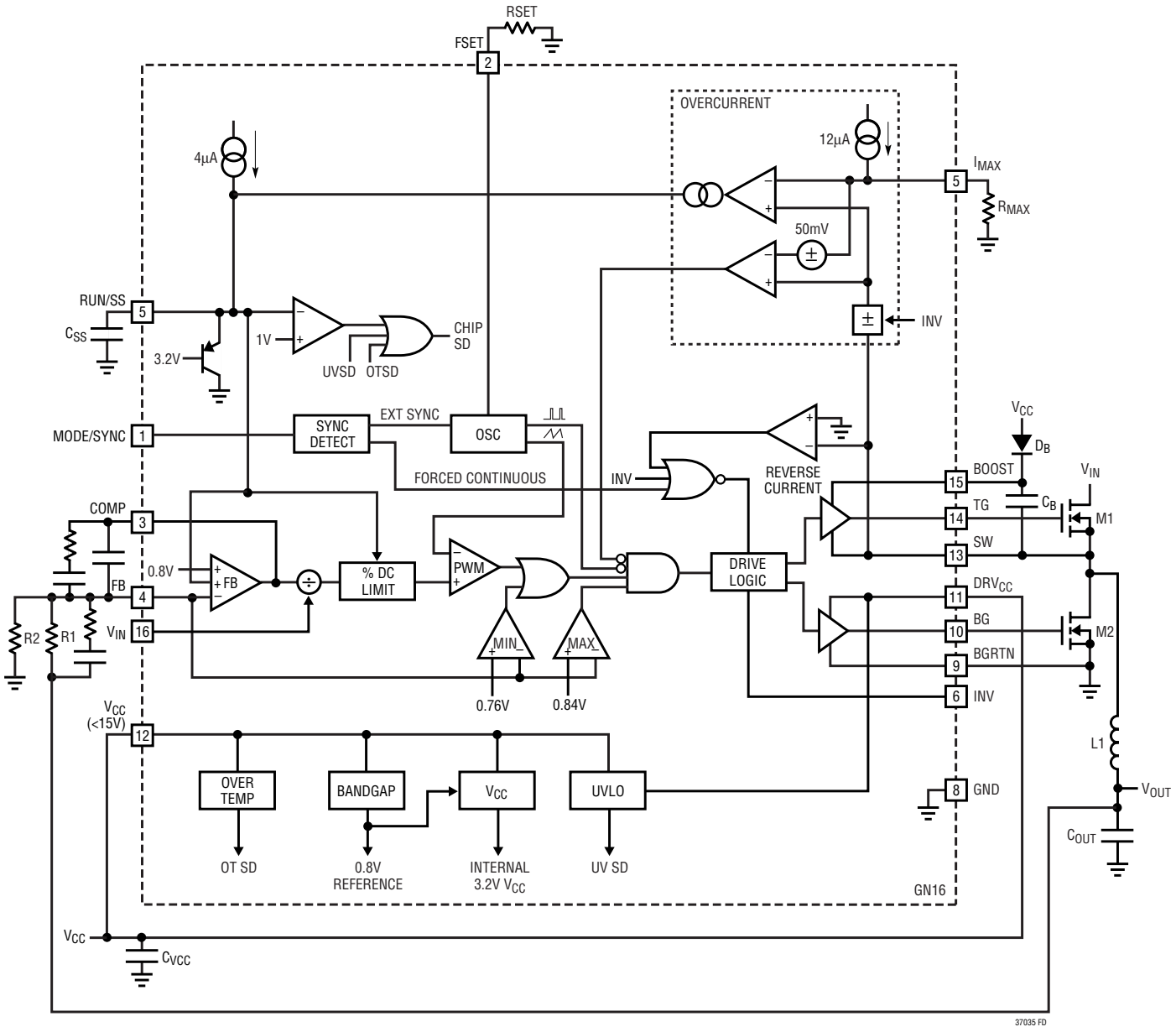
SW (Pin 13/Pin 26): Switch Node Connection to Inductor and Bootstrap Capacitor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to V_{IN}.

TG (Pin 14/Pin 27): Top Gate Drive. The TG pin drives the gate of the top N-channel synchronous switch MOSFET. The TG driver draws power from the BOOST pin and returns to the SW pin, providing true floating drive to the top MOSFET.

BOOST (Pin 15/Pin 28): Top Gate Driver Supply. The BOOST pin supplies power to the floating TG driver. The BOOST pin should be bypassed to SW with a low ESR (X5R or better) 0.1µF ceramic capacitor. An additional fast recovery Schottky diode from DRV_{CC} to BOOST will create a complete floating charge-pumped supply at BOOST.

V_{IN} (Pin 16/Pin 1): Input Voltage Sense Pin. This pin is connected to the high voltage input of the regulator and is used by the internal feedforward compensation circuitry to improve line regulation. **This is not a supply pin**.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

The LTC3703-5 is a constant frequency, voltage mode controller for DC/DC step-down converters. It is designed to be used in a synchronous switching architecture with two external N-channel MOSFETs. Its high operating voltage capability allows it to directly step down input voltages up to 60V without the need for a step-down transformer. For circuit operation, please refer to the Functional Diagram of the IC and the circuit on the first page of this data sheet. The LTC3703-5 uses voltage mode control in which the duty ratio is controlled directly by the error amplifier output and thus requires no current sense resistor. The V_{FB} pin receives the output voltage feedback and is compared to the internal 0.8V reference by the error amplifier, which outputs an error signal at the COMP pin.

OPERATION (Refer to Functional Diagram)

When the load current increases, it causes a drop in the feedback voltage relative to the reference. The COMP voltage then rises, increasing the duty ratio until the output feedback voltage again matches the reference voltage. In normal operation, the top MOSFET is turned on when the RS latch is set by the on-chip oscillator and is turned off when the PWM comparator trips and resets the latch. The PWM comparator trips at the proper duty ratio by comparing the error amplifier output (after being "compensated" by the line feedforward multiplier) to a sawtooth waveform generated by the oscillator. When the top MOSFET is turned off, the bottom MOSFET is turned on until the next cycle begins or, if Pulse Skip Mode operation is enabled, until the inductor current reverses as determined by the reverse current comparator. MAX and MIN comparators ensure that the output never exceed ±5% of nominal value by monitoring V_{FB} and forcing the output back into regulation quickly by either keeping the top MOSFET off or forcing maximum duty cycle. The operation of its other features—fast transient response, outstanding line regulation, strong gate drivers, short-circuit protection, and shutdown/soft-start—are described below.

Fast Transient Response

The LTC3703-5 uses a fast 25MHz op amp as an error amplifier. This allows the compensation network to be optimized for better load transient response. The high bandwidth of the amplifier, along with high switching frequencies and low value inductors, allow very high loop crossover frequencies. The 800mV internal reference allows regulated output voltages as low as 800mV without external level shifting amplifiers.

Line Feedforward Compensation

The LTC3703-5 achieves outstanding line transient response using a patented feedforward correction scheme. With this circuit the duty cycle is adjusted instantaneously to changes in input voltage, thereby avoiding unacceptable overshoot or undershoot. It has the added advantage of making the DC loop gain independent of input voltage. Figure 1 shows how large transient steps at the input have little effect on the output voltage.

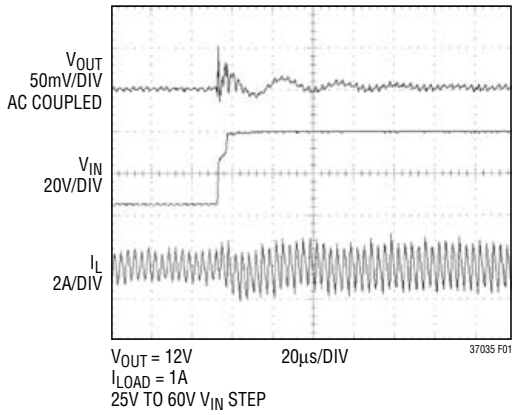


Figure 1. Line Transient Performance

Strong Gate Drivers

The LTC3703-5 contains very low impedance drivers capable of supplying amps of current to slew large MOSFET gates quickly. This minimizes transition losses and allows paralleling MOSFETs for higher current applications. A 60V floating high side driver drives the top side MOSFET and a low side driver drives the bottom side MOSFET (see Figure 2). They can be powered from either a separate DC supply or a voltage derived from the input or output voltage (see MOSFET Driver Supplies section). The bottom side driver is supplied directly from the DRV_{CC} pin. The top MOSFET drivers are biased from floating bootstrap capacitor C_B, which normally is recharged during each off cycle through an external diode from DRV_{CC} when the top MOSFET turns off. In Pulse Skip Mode operation, where it is possible that the bottom MOSFET will be off for an extended period of time, an internal counter guarantees that the bottom MOSFET is turned on at least once every 10 cycles for 10% of the period to refresh the bootstrap capacitor. An undervoltage lockout keeps the LTC3703-5 shut down unless this voltage is above 4.1V.

The bottom driver has an additional feature that helps minimize the possibility of external MOSFET shoot-thru. When the top MOSFET turns on, the switch node dV/dt pulls up the bottom MOSFET's internal gate through the Miller capacitance, even when the bottom driver is holding the gate terminal at ground. If the gate is pulled up high enough, shoot-thru between the top side and bottom side

OPERATION (Refer to Functional Diagram)

MOSFETs can occur. To prevent this from occuring, the bottom driver return is brought out as a separate pin (BGRTN) so that a negative supply can be used to reduce the effect of the Miller pull-up. For example, if a –2V supply is used on BGRTN, the switch node dV/dt could pull the gate up 2V before the V_{GS} of the bottom MOSFET has more than 0V across it.

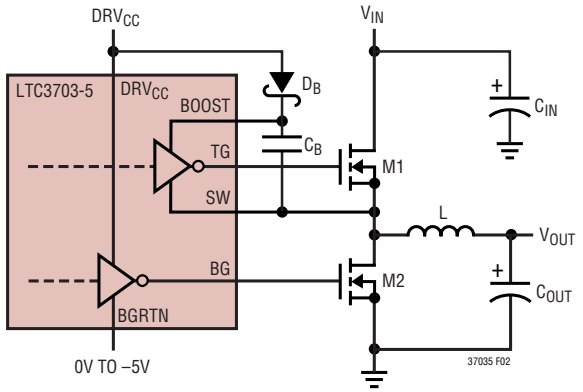


Figure 2. Floating TG Driver Supply and Negative BG Return

Constant Frequency

The internal oscillator can be programmed with an external resistor connected from f_{SET} to ground to run between 100kHz and 600kHz, thereby optimizing component size, efficiency, and noise for the specific application. The internal oscillator can also be synchronized to an external clock applied to the MODE/SYNC pin and can lock to a frequency in the 100kHz to 600kHz range. When locked to an external clock, Pulse Skip Mode operation is automatically disabled. Constant frequency operation brings with it a number of benefits: Inductor and capacitor values can be chosen for a precise operating frequency and the feedback loop can be similarly tightly specified. Noise generated by the circuit will always be at known frequencies. Subharmonic oscillation and slope compensation, common headaches with constant frequency current mode switchers, are absent in voltage mode designs like the LTC3703-5.

Shutdown/Soft-Start

The main control loop is shut down by pulling RUN/SS pin low. Releasing RUN/SS allows an internal 4µA current source to charge the soft-start capacitor C_{SS}. When C_{SS} reaches 1V, the main control loop is enabled with the duty cycle control set to 0%. As C_{SS} continues to charge, the duty cycle is gradually increased, allowing the output voltage to rise. This soft-start scheme smoothly ramps the output voltage to its regulated value, with no overshoot. The RUN/SS voltage will continue ramping until it reaches an internal 4V clamp. Then the MIN feedback comparator is enabled and the LTC3703-5 is in full operation. When the RUN/SS is low, the supply current is reduced to 25µA.

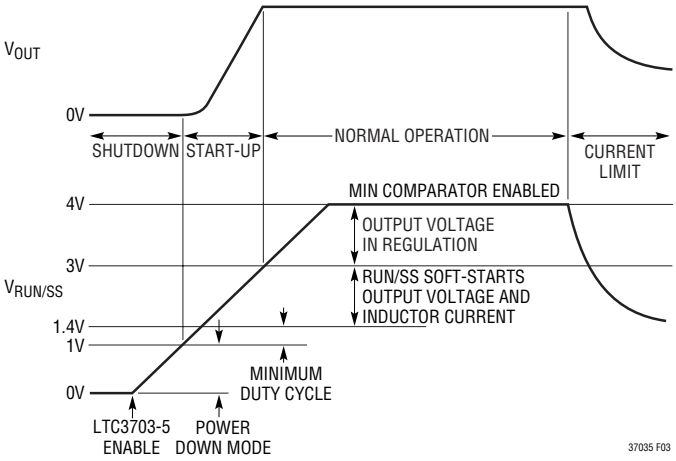


Figure 3. Soft-Start Operation in Start Up and Current Limit

Current Limit

The LTC3703-5 includes an onboard current limit circuit that limits the maximum output current to a user-programmed level. It works by sensing the voltage drop across the bottom MOSFET and comparing that voltage to a user-programmed voltage at the I_{MAX} pin. Since the bottom MOSFET looks like a low value resistor during its on-time, the voltage drop across it is proportional to the current flowing in it. In a buck converter, the average current in the inductor is equal to the output current. This current also flows through the bottom MOSFET during its on-time. Thus by watching the drain-to-source voltage when the bottom MOSFET is on, the LTC3703-5 can monitor the output current. The LTC3703-5 senses this voltage and inverts it to allow it to compare the sensed voltage (which becomes more negative as peak current increases) with a positive voltage at the I_{MAX} pin. The I_{MAX} pin includes a 12µA pull-up, enabling the user to set the voltage at I_{MAX} with a single resistor (R_{IMAX}) to ground. See the Current Limit Programming section for R_{IMAX} selection.

OPERATION (Refer to Functional Diagram)

For maximum protection, the LTC3703-5 current limit consists of a steady-state limit circuit and an instantaneous limit circuit. The steady-state limit circuit is a g_m amplifier that pulls a current from the RUN/SS pin proportional to the difference between the SW and I_{MAX} voltages. This current begins to discharge the capacitor at RUN/SS, reducing the duty cycle and controlling the output voltage until the current regulates at the limit. Depending on the size of the capacitor, it may take many cycles to discharge the RUN/SS voltage enough to properly regulate the output current. This is where the instantaneous limit circuit comes into play. The instantaneous limit circuit is a cycle-by-cycle comparator which monitors the bottom MOSFET's drain voltage and keeps the top MOSFET from turning on whenever the drain voltage is 50mV above the programmed max drain voltage. Thus the cycle-by-cycle comparator will keep the inductor current under control until the g_m amplifier gains control.

Pulse Skip Mode

The LTC3703-5 can operate in one of two modes selectable with the MODE/SYNC pin—Pulse Skip Mode or forced continuous mode. Pulse Skip Mode is selected when increased efficiency at light loads is desired. In this mode, the bottom MOSFET is turned off when inductor current reverses to minimize the efficiency loss due to reverse current flow. As the load is decreased (see Figure 5), the duty cycle is reduced to maintain regulation until its minimum on-time (~200ns) is reached. When the load decreases below this point, the LTC3703-5 begins to skip cycles to maintain regulation. The frequency drops but this further improves efficiency by minimizing gate charge losses. In forced continuous mode, the bottom MOSFET is always on when the top MOSFET is off, allowing the inductor current to reverse at low currents. This mode is less efficient due to resistive losses, but has the advantage of better transient response at low currents, constant frequency operation, and the ability to maintain regulation when sinking current. See Figure 4 for a comparison of the effect on efficiency at light loads for each mode. The MODE/SYNC threshold is 0.8V ±7.5%, allowing the MODE/SYNC to act as a feedback pin for regulating a second winding. If the feedback voltage drops below 0.8V, the LTC3703-5 reverts to continuous operation to maintain regulation in the secondary supply.

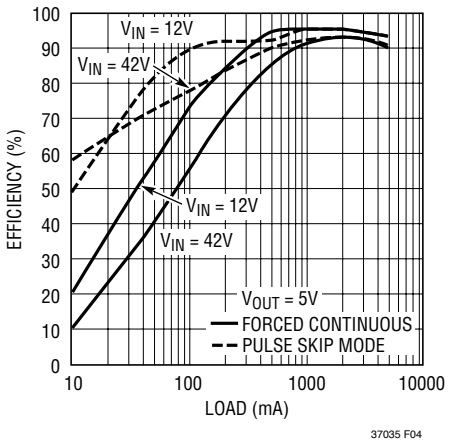


Figure 4. Efficiency in Pulse Skip/Forced Continuous Modes

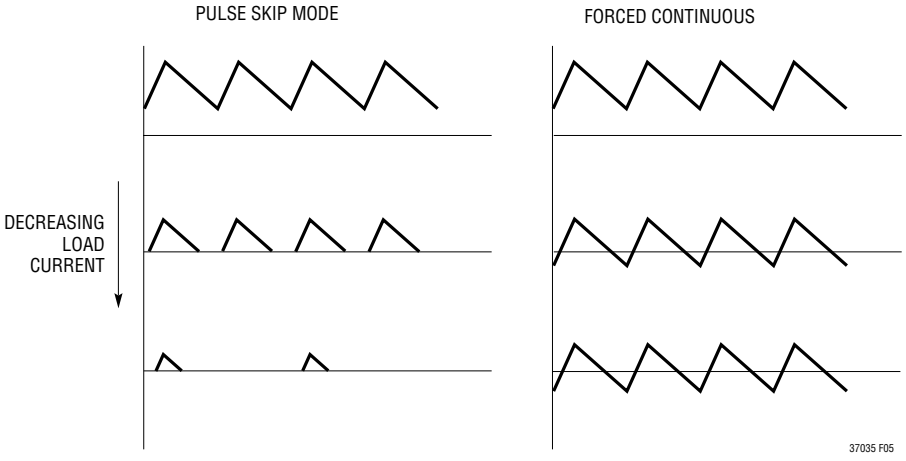


Figure 5. Comparison of Inductor Current Waveforms for Pulse Skip Mode and Forced Continuous Operation

OPERATION (Refer to Functional Diagram)

Buck or Boost Mode Operation

The LTC3703-5 has the capability of operating both as a step-down (buck) and step-up (boost) controller. In boost mode, output voltages as high as 60V can be tightly regulated. With the INV pin grounded, the LTC3703-5 operates in buck mode with TG driving the main (top side) switch and BG driving the synchronous (bottom side) switch. If the INV pin is pulled above 2V, the LTC3703-5 operates in boost mode with BG driving the main (bottom side) switch and TG driving the synchronous (top side) switch. Internal circuit operation is very similar regardless of the operating mode with the following exceptions: In boost mode, Pulse Skip Mode operation is always disabled regardless of the level of the MODE/SYNC pin and the line feedforward compensation is also disabled. The overcurrent circuitry continues to monitor the load current by looking at the drain voltage of the main (bottom side) MOSFET. In boost mode, however, the peak MOSFET current does not equal the load current but instead $I_D = I_{LOAD}/(1 – D)$. This factor needs to be taken into account when programming the I_{MAX} voltage.

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The basic LTC3703-5 application circuit is shown on the first page of this data sheet. External component selection is determined by the input voltage and load requirements as explained in the following sections. After the operating frequency is selected, R_{SET} and L can be chosen. The operating frequency and the inductor are chosen for a desired amount of ripple current and also to optimize efficiency and component size. Next, the power MOSFETs and D1 are selected based on voltage, load and efficiency requirements. C_{IN} is selected for its ability to handle the large RMS currents in the converter and C_{OUT} is chosen with low enough ESR to meet the output voltage ripple and transient specifications. Finally, the loop compensation components are chosen to meet the desired transient specifications.

Operating Frequency

The choice of operating frequency and inductor value is a trade off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses and gate charge losses. However, lower frequency operation requires more inductance for a given amount of ripple current, resulting in a larger inductor size and higher cost. If the ripple current is allowed to increase, larger output capacitors may be required to maintain the same output ripple. For converters with high step-down V_{IN} to V_{OUT} ratios, another consideration is the minimum on-time of the LTC3703-5 (see the Minimum On-time Considerations section). A final consideration for operating frequency is that in noise-sensitive communications systems, it is often desirable to keep the switching noise out of a sensitive frequency band.

The LTC3703-5 uses a constant frequency architecture that can be programmed over a 100kHz to 600kHz range with a single resistor from the f_{SET} pin to ground, as shown in the circuit on the first page of this data sheet. The nominal voltage on the f_{SET} pin is 1.2V, and the current that flows from this pin is used to charge and discharge an internal oscillator capacitor. The value of R_{SET} for a given operating frequency can be chosen from Figure 6 or from the following equation:

$$R_{SET}(k\Omega) = \frac{7100}{f(kHz) - 25}$$

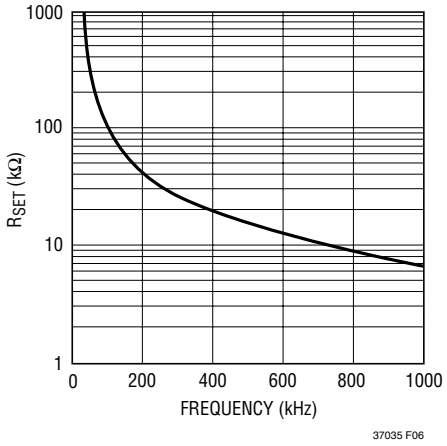

Figure 6. Timing Resistor (R_{SET}) Value

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The oscillator can also be synchronized to an external clock applied to the MODE/SYNC pin with a frequency in the range of 100kHz to 600kHz (refer to the MODE/SYNC Pin section for more details). In this synchronized mode, Pulse Skip Mode operation is disabled. The clock high level must exceed 2V for at least 25ns. As shown in Figure 7, the top MOSFET turn-on will follow the rising edge of the external clock by a constant delay equal to one-tenth of the cycle period.

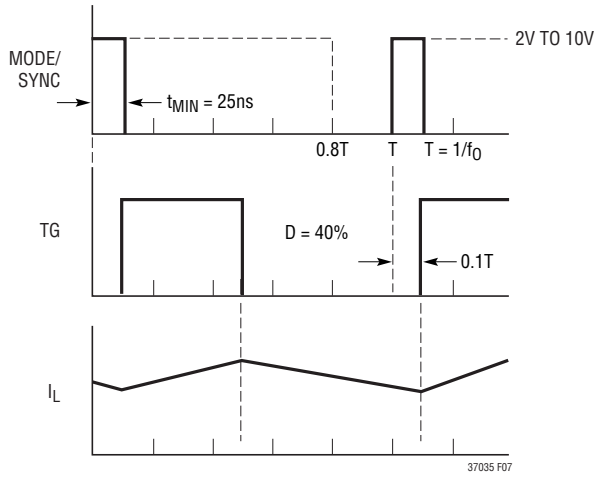

Figure 7. MODE/SYNC Clock Input and Switching Waveforms for Synchronous Operation

Inductor

The inductor in a typical LTC3703-5 circuit is chosen for a specific ripple current and saturation current. Given an input voltage range and an output voltage, the inductor value and operating frequency directly determine the ripple current. The inductor ripple current in the buck mode is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Thus highest efficiency operation is obtained at low frequency with small ripple current. To achieve this, however, requires a large inductor.

A reasonable starting point is to choose a ripple current between 20% and 40% of $I_{O(MAX)}$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductor in buck mode should be chosen according to:

$$L \geq \frac{V_{OUT}}{f\,\Delta I_{L(MAX)}}\left(1-\frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor also has an affect on low current operation when Pulse Skip Mode operation is enabled. The frequency begins to decrease when the output current drops below the average inductor current at which the LTC3703-5 is operating at its $t_{ON(MIN)}$ in discontinuous mode (see Figure 5). Lower inductance increases the peak inductor current that occurs in each minimum on-time pulse and thus increases the output current at which the frequency starts decreasing.

Power MOSFET Selection

The LTC3703-5 requires at least two external N-channel power MOSFETs, one for the top (main) switch and one or more for the bottom (synchronous) switch. The number, type and "on" resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than 1/3 of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFETs' "on" resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low "on" resistance with significantly reduced input capacitance for the main switch application in switching regulators.

Selection criteria for the power MOSFETs include the "on" resistance $R_{DS(ON)}$, input capacitance, breakdown voltage and maximum output current.

The most important parameter in high voltage applications is breakdown voltage BV_{DSS}. Both the top and bottom MOSFETs will see full input voltage plus any additional ringing on the switch node across its drain-to-source during its off-time and must be chosen with the

APPLICATIONS INFORMATION

appropriate breakdown specification. Since most MOSFETs in the 30V to 60V range have logic level thresholds ($V_{GS(MIN)} \geq 4.5V$), the LTC3703-5 is designed to be used with a 4.5V to 15V gate drive supply (DRV_{CC} pin).

For maximum efficiency, on-resistance $R_{DS(ON)}$ and input capacitance should be minimized. Low $R_{DS(ON)}$ minimizes conduction losses and low input capacitance minimizes transition losses. MOSFET input capacitance is a combination of several components but can be taken from the typical "gate charge" curve included on most data sheets (Figure 8).

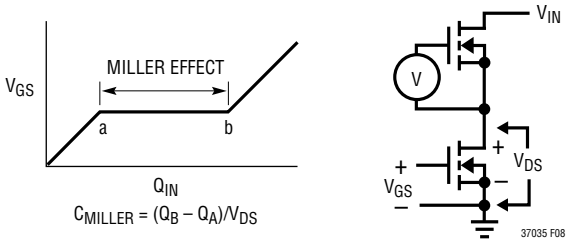

Figure 8. Gate Charge Characteristic

The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturers data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included.

When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{MainSwitchDutyCycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{SynchronousSwitchDutyCycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DR(ON)} + V_{IN}{}^2\frac{I_{MAX}}{2}(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{CC}-V_{TH(IL)}}+\frac{1}{V_{TH(IL)}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), V_{IN} is the drain potential *and* the change in drain potential in the particular application. $V_{TH(IL)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique described above.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For $V_{IN} < 25V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 25V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, and typically varies from 0.005/°C to 0.01/°C depending on the particular MOSFET used.

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Multiple MOSFETs can be used in parallel to lower $R_{DS(ON)}$ and meet the current and thermal requirements if desired. The LTC3703-5 contains large low impedance drivers capable of driving large gate capacitances without significantly slowing transition times. In fact, when driving MOSFETs with very low gate charge, it is sometimes helpful to slow down the drivers by adding small gate resistors (10Ω or less) to reduce noise and EMI caused by the fast transitions.

Schottky Diode Selection

The Schottky diode D1 shown in the circuit on the first page of this data sheet conducts during the dead time between the conduction of the power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead time and requiring a reverse recovery period that could cost as much as 1% to 2% in efficiency. A 1A Schottky diode is generally a good size for 3A to 5A regulators. Larger diodes result in additional losses due to their larger junction capacitance. The diode can be omitted if the efficiency loss can be tolerated.

Input Capacitor Selection

In continuous mode, the drain current of the top MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN} which must be supplied by the input capacitor. To prevent large input transients, a low ESR input capacitor sized for the maximum RMS current is given by:

$$I_{CIN(RMS)} \cong I_{O(MAX)} \frac{V_{OUT}}{V_{IN}} \left(\frac{V_{IN}}{V_{OUT}} - 1 \right)^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{O(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the ripple current ratings from capacitor manufacturers are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be placed in parallel to meet size or height requirements in the design.

Because tantalum and OS-CON capacitors are not available in voltages above 30V, ceramics or aluminum electrolytics must be used for regulators with input supplies above 30V. Ceramic capacitors have the advantage of very low ESR and can handle high RMS current, but ceramics with high voltage ratings (>50V) are not available with more than a few microfarads of capacitance. Furthermore, ceramics have high voltage coefficients which means that the capacitance values decrease even more when used at the rated voltage. X5R and X7R type ceramics are recommended for their lower voltage and temperature coefficients. Another consideration when using ceramics is their high Q which, if not properly damped, may result in excessive voltage stress on the power MOSFETs. Aluminum electrolytics have much higher bulk capacitance, but they have higher ESR and lower RMS current ratings.

A good approach is to use a combination of aluminum electrolytics for bulk capacitance and ceramics for low ESR and RMS current. If the RMS current cannot be handled by the aluminum capacitors alone, when used together, the percentage of RMS current that will be supplied by the aluminum capacitor is reduced to approximately:

$$\%I_{RMS,ALUM} \approx \frac{1}{\sqrt{1+(8fCR_{ESR})^2}} \bullet 100\%$$

where R_{ESR} is the ESR of the aluminum capacitor and C is the overall capacitance of the ceramic capacitors. Using an aluminum electrolytic with a ceramic also helps damp the high Q of the ceramic, minimizing ringing.

Output Capacitor Selection

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple. The output ripple (ΔV_{OUT}) is approximately equal to:

$$\Delta V_{OUT} \leq \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}} \right)$$

Since ΔI_L increases with input voltage, the output ripple is highest at maximum input voltage. ESR also has a significant effect on the load transient response. Fast load transitions at the output will appear as voltage across the ESR of C_{OUT} until the feedback loop in the LTC3703-5 can change the inductor current to match the new load current

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value. Typically, once the ESR requirement is satisfied the capacitance is adequate for filtering and has the required RMS current rating.

Manufacturers such as Nichicon, Nippon Chemi-Con and Sanyo should be considered for high performance throughhole capacitors. The OS-CON (organic semiconductor dielectric) capacitor available from Sanyo has the lowest product of ESR and size of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the effect of their lead inductance.

In surface mount applications, multiple capacitors placed in parallel may be required to meet the ESR, RMS current handling and load step requirements. Dry tantalum, special polymer and aluminum electrolytic capacitors are available in surface mount packages. Special polymer capacitors offer very low ESR but have lower capacitance density than other types. Tantalum capacitors have the highest capacitance density but it is important to only use types that have been surge tested for use in switching power supplies. Several excellent surge-tested choices are the AVX TPS and TPSV or the KEMET T510 series. Aluminum electrolytic capacitors have significantly higher ESR, but can be used in cost-driven applications providing that consideration is given to ripple current ratings and long term reliability. Other capacitor types include Panasonic SP and Sanyo POSCAPs.

Output Voltage

The LTC3703-5 output voltage is set by a resistor divider according to the following formula:

$$V_{OUT} = 0.8V\left(1+\frac{R1}{R2}\right)$$

The external resistor divider is connected to the output as shown in the Functional Diagram, allowing remote voltage sensing. The resultant feedback signal is compared with the internal precision 800mV voltage reference by the error amplifier. The internal reference has a guaranteed tolerance of ±1%. Tolerance of the feedback resistors will add additional error to the output voltage. 0.1% to 1% resistors are recommended.

MOSFET Driver Supplies (DRV_{CC} and BOOST)

The LTC3703-5 drivers are supplied from the DRV_{CC} and BOOST pins (see Figure 2), which have an absolute maximum voltage of 15V. If the main supply voltage, V_{IN}, is higher than 15V a separate supply with a voltage between 5V and 15V must be used to power the drivers. If a separate supply is not available, one can easily be generated from the main supply using one of the circuits shown in Figure 9. If the output voltage is between 5V and 15V, the output can be used to directly power the drivers as shown in Figure 9a. If the output is below 5V, Figure 9b shows an easy way to boost the supply voltage to a sufficient level. This boost circuit uses the LT1613 in a ThinSOT™ package and a chip inductor for minimal extra area (<0.2 in^2). Two other possible schemes are an extra winding on the inductor (Figure 9c) or a capacitive charge pump (Figure 9d). All the circuits shown in Figure 9 require a start-up circuit (Q1, D1 and R1) to provide driver power at initial start-up or following a short-circuit. The resistor R1 must be sized so that it supplies sufficient base current and zener bias current at the lowest expected value of V_{IN}. When using an existing supply, the supply must be capable of supplying the required gate driver current which can be estimated from:

$$I_{DRVCC} = (f)(Q_{G(TOP)} + Q_{G(BOTTOM)})$$

This equation for I_{DRVCC} is also useful for properly sizing the circuit components shown in Figure 9.

An external bootstrap capacitor, C_B, connected to the BOOST pin supplies the gate drive voltage for the topside MOSFETs. Capacitor C_B is charged through external diode, D_B, from the DRV_{CC} supply when SW is low. When the top side MOSFET is turned on, the driver places the C_B voltage across the gate-source of the top MOSFET. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{DRVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the top side MOSFET(s). The reverse breakdown of the external diode, D_B, must be greater than $V_{IN(MAX)}$. Another important consideration for the external diode is the reverse recovery and reverse leakage, either of which may cause excessive reverse

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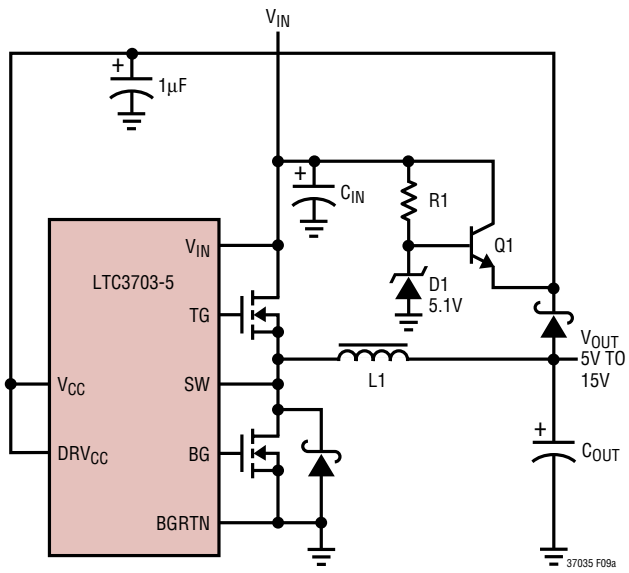

Figure 9a. V_{CC} Generated from 5V < V_{OUT} < 15V

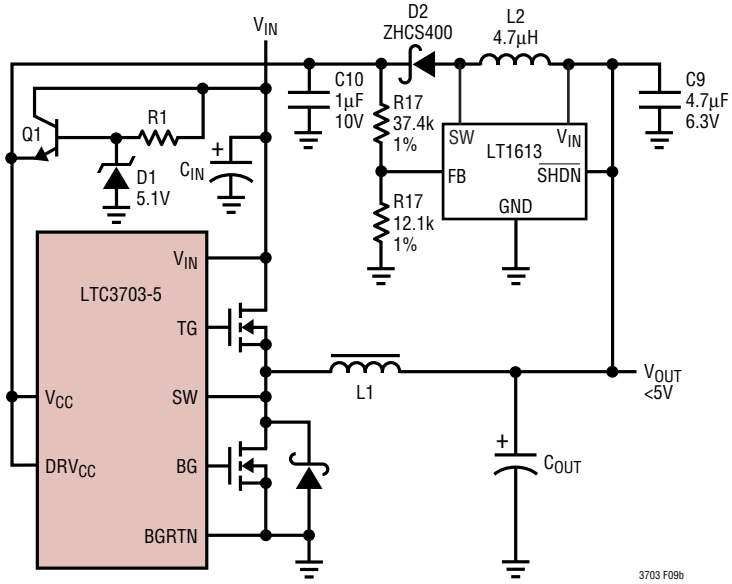

Figure 9b. V_{CC} Generated from V_{OUT} < 5V

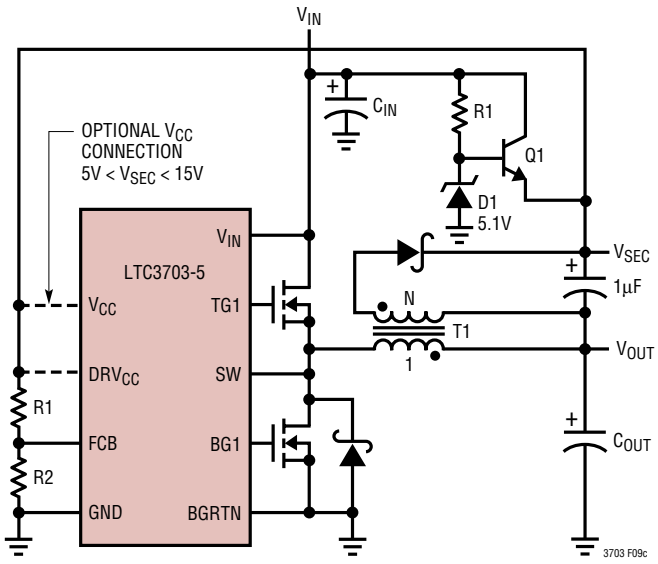

Figure 9c. Secondary Output Loop and V_{CC} Connection

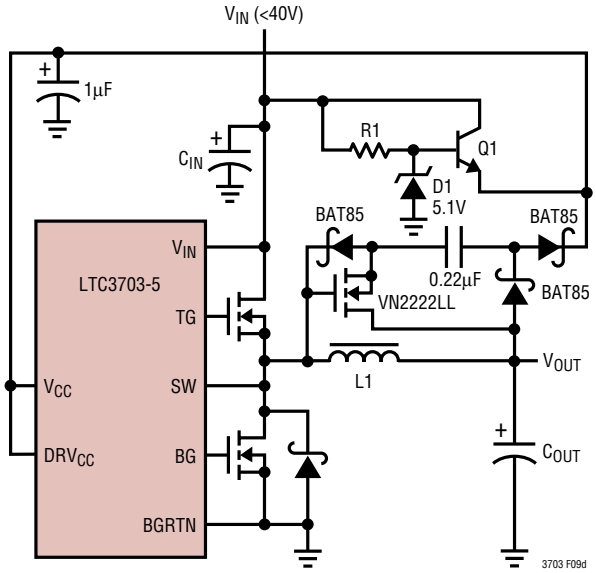

Figure 9d. Capacitive Charge Pump for V_{CC} (V_{IN} < 40V)

current to flow at full reverse voltage. If the reverse current times reverse voltage exceeds the maximum allowable power dissipation, the diode may be damaged. For best results, use an ultrafast recovery diode such as the MMDL770T1.

An internal undervoltage lockout (UVLO) monitors the voltage on DRV_{CC} to ensure that the LTC3703-5 has sufficient gate drive voltage. If the DRV_{CC} voltage falls below the UVLO threshold, the LTC3703-5 shuts down and the gate drive outputs remain low.

Bottom MOSFET Source Supply (BGRTN)

The bottom gate driver, BG, switches from DRV_{CC} to BGRTN where BGRTN can be a voltage between ground and –5V. Why not just keep it simple and always connect BGRTN to ground? In high voltage switching converters, the switch

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node dV/dt can be many volts/ns, which will pull up on the gate of the bottom MOSFET through its Miller capacitance. If this Miller current, times the internal gate resistance of the MOSFET plus the driver resistance, exceeds the threshold of the FET, shoot-through will occur. By using a negative supply on BGRTN, the BG can be pulled below ground when turning the bottom MOSFET off. This provides a few extra volts of margin before the gate reaches the turn-on threshold of the MOSFET. Be aware that the maximum voltage difference between DRV_{CC} and BGRTN is 15V. If, for example, V_{BGRTN} = –2V, the maximum voltage on DRV_{CC} pin is now 13V instead of 15V.

Current Limit Programming

Programming current limit on the LTC3703-5 is straight forward. The I_{MAX} pin sets the current limit by setting the maximum allowable voltage drop across the bottom MOSFET. The voltage across the MOSFET is set by its on-resistance and the current flowing in the inductor, which is the same as the output current. The LTC3703-5 current limit circuit inverts the negative voltage across the MOSFET before comparing it to the voltage at I_{MAX}, allowing the current limit to be set with a positive voltage.

To set the current limit, calculate the expected voltage drop across the bottom MOSFET at the maximum desired current and maximum junction temperature:

$$V_{PROG} = (I_{LIMIT})(R_{DS(ON)})(1 + \delta)$$

where δ is explained in the MOSFET Selection section. V_{PROG} is then programmed at the I_{MAX} pin using the internal 12µA pull-up and an external resistor:

$$R_{IMAX} = V_{PROG}/12\mu A$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the largest power loss in the converter. Note that it is important to check for self-consistency between the assumed MOSFET junction temperature and the resulting value of I_{LIMIT} which heats the MOSFET switches.

Caution should be used when setting the current limit based upon the $R_{DS(ON)}$ of the MOSFETs. The maximum current limit is determined by the minimum MOSFET on-resistance. Data sheets typically specify nominal and maximum values for $R_{DS(ON)}$, but not a minimum. A reasonable assumption is that the minimum $R_{DS(ON)}$ lies the same amount below the typical value as the maximum lies above it. Consult the MOSFET manufacturer for further guidelines.

For best results, use a V_{PROG} voltage between 100mV and 500mV. Values outside of this range may give less accurate current limit. The current limit can also be disabled by floating the I_{MAX} pin.

FEEDBACK LOOP/COMPENSATION

Feedback Loop Types

In a typical LTC3703-5 circuit, the feedback loop consists of the modulator, the external inductor, the output capacitor and the feedback amplifier with its compensation network. All of these components affect loop behavior and must be accounted for in the loop compensation. The modulator consists of the internal PWM generator, the output MOSFET drivers and the external MOSFETs themselves. From a feedback loop point of view, it looks like a linear voltage transfer function from COMP to SW and has a gain roughly equal to the input voltage. It has fairly benign AC behavior at typical loop compensation frequencies with significant phase shift appearing at half the switching frequency.

The external inductor/output capacitor combination makes a more significant contribution to loop behavior. These components cause a second order LC roll off at the output, with the attendant 180° phase shift. This rolloff is what filters the PWM waveform, resulting in the desired DC output voltage, but the phase shift complicates the loop compensation if the gain is still higher than unity at the pole frequency. Eventually (usually well above the LC pole frequency), the reactance of the output capacitor will approach its ESR and the rolloff due to the capacitor will stop, leaving 6dB/octave and 90° of phase shift (Figure 10).

So far, the AC response of the loop is pretty well out of the user's control. The modulator is a fundamental piece of the LTC3703-5 design and the external L and C are usually chosen based on the regulation and load current requirements without considering the AC loop response. The

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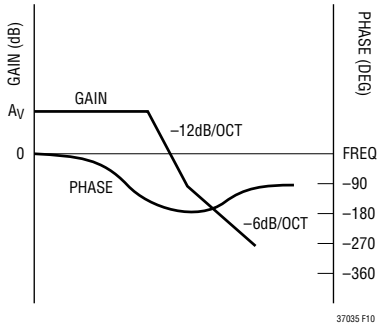

Figure 10. Transfer Function of Buck Modulator

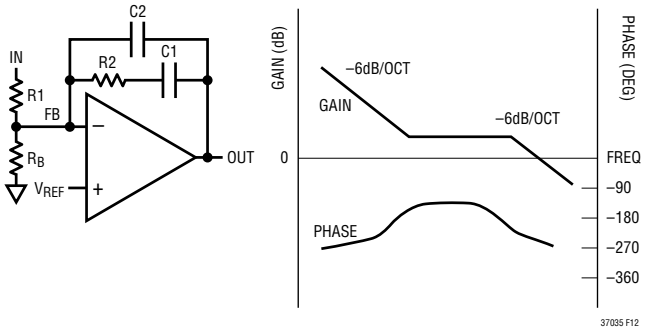

Figure 12. Type 2 Schematic and Transfer Function

feedback amplifier, on the other hand, gives us a handle with which to adjust the AC response. The goal is to have 180° phase shift at DC (so the loop regulates) and something less than 360° phase shift at the point that the loop gain falls to 0dB. The simplest strategy is to set up the feedback amplifier as an inverting integrator, with the 0dB frequency lower than the LC pole (Figure 11). This "Type 1" configuration is stable but transient response is less than exceptional if the LC pole is at a low frequency.

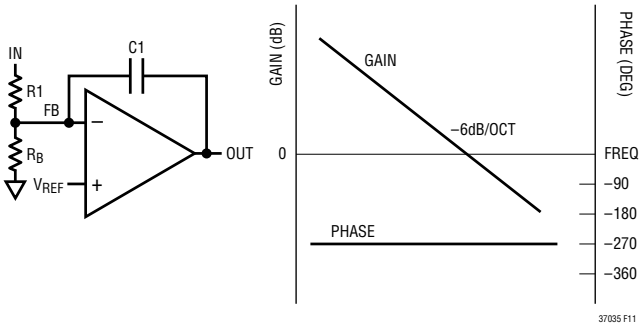

Figure 11. Type 1 Schematic and Transfer Function

Figure 12 shows an improved "Type 2" circuit that uses an additional pole-zero pair to temporarily remove 90° of phase shift. This allows the loop to remain stable with 90° more phase shift in the LC section, provided the loop reaches 0dB gain near the center of the phase "bump." Type 2 loops work well in systems where the ESR zero in the LC roll-off happens close to the LC pole, limiting the total phase shift due to the LC. The additional phase compensation in the feedback amplifier allows the 0dB point to be at or above the LC pole frequency, improving loop bandwidth substantially over a simple Type 1 loop. It has limited ability to compensate for LC combinations where low capacitor ESR keeps the phase shift near 180° for an extended frequency range. LTC3703-5 circuits using conventional switching grade electrolytic output capacitors can often get acceptable phase margin with Type 2 compensation.

"Type 3" loops (Figure 13) use two poles and two zeros to obtain a 180° phase boost in the middle of the frequency band. A properly designed Type 3 circuit can maintain acceptable loop stability even when low output capacitor ESR causes the LC section to approach 180° phase shift well above the initial LC roll-off. As with a Type 2 circuit, the loop should cross through 0dB in the middle of the phase bump to maximize phase margin. Many LTC3703-5 circuits using low ESR tantalum or OS-CON output capacitors need Type 3 compensation to obtain acceptable phase margin with a high bandwidth feedback loop.

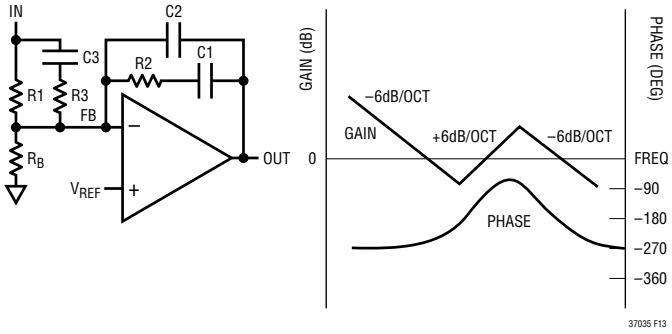

Figure 13. Type 3 Schematic and Transfer Function

Feedback Component Selection

Selecting the R and C values for a typical Type 2 or Type 3 loop is a nontrivial task. The applications shown in this data sheet show typical values, optimized for the power components shown. They should give acceptable performance with similar power components, but can be way off

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if even one major power component is changed significantly. Applications that require optimized transient response will require recalculation of the compensation values specifically for the circuit in question. The underlying mathematics are complex, but the component values can be calculated in a straightforward manner if we know the gain and phase of the modulator at the crossover frequency.

Modulator gain and phase can be measured directly from a breadboard or can be simulated if the appropriate parasitic values are known. Measurement will give more accurate results, but simulation can often get close enough to give a working system. To measure the modulator gain and phase directly, wire up a breadboard with an LTC3703-5 and the actual MOSFETs, inductor and input and output capacitors that the final design will use. This breadboard should use appropriate construction techniques for high speed analog circuitry: bypass capacitors located close to the LTC3703-5, no long wires connecting components, appropriately sized ground returns, etc. Wire the feedback amplifier as a simple Type 1 loop, with a 10k resistor from V_{OUT} to FB and a 0.1µF feedback capacitor from COMP to FB. Choose the bias resistor (R_B) as required to set the desired output voltage. Disconnect R_B from ground and connect it to a signal generator or to the source output of a network analyzer (Figure 14) to inject a test signal into the loop. Measure the gain and phase from the COMP pin to the output node at the positive terminal of the output capacitor. Make sure the analyzer's input is AC coupled so that the DC voltages present at both the COMP and V_{OUT} nodes don't corrupt the measurements or damage the analyzer.

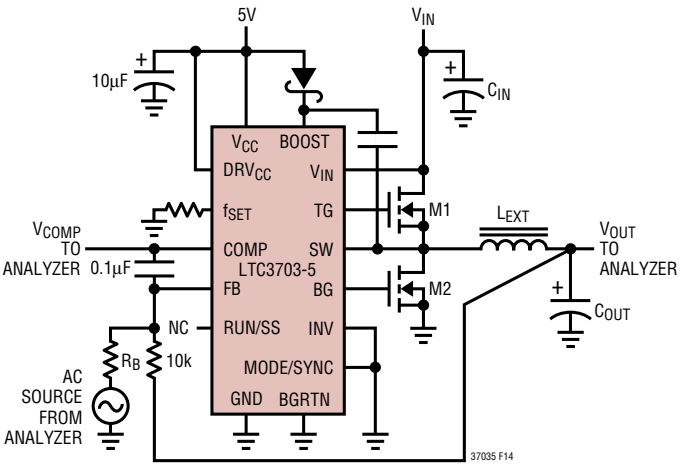

Figure 14. Modulator Gain/Phase Measurement Set-Up

If breadboard measurement is not practical, a SPICE simulation can be used to generate approximate gain/phase curves. Plug the expected capacitor, inductor and MOSFET values into the following SPICE deck and generate an AC plot of V(V_{OUT})/V(COMP) in dB and phase of V_{OUT} in degrees. Refer to your SPICE manual for details of how to generate this plot.

```
*3703-5 modulator gain/phase
*2003 Linear Technology
*this file written to run with PSpice 8.0
*may require modifications for other
SPICE simulators

*MOSFETs
rfet mod sw 0.02      ;MOSFET rdson

*inductor
lext sw out1 10u      ;inductor value
rl out1 out 0.015     ;inductor series R

*output cap
cout out out2 540u    ;capacitor value
resr out2 0 0.01      ;capacitor ESR

*3703-5 internals
emod mod 0 value = {43*v(comp)}
                      ;3703-5multiplier
vstim comp 0 0 ac 1   ;ac stimulus
.ac dec 100 1k 1meg
.probe
.end
```

With the gain/phase plot in hand, a loop crossover frequency can be chosen. Usually the curves look something like Figure 10. Choose the crossover frequency in the rising or flat parts of the phase curve, beyond the external LC poles. Frequencies between 10kHz and 50kHz usually work well. Note the gain (GAIN, in dB) and phase (PHASE, in degrees) at this point. The desired feedback amplifier gain will be –GAIN to make the loop gain at 0dB at this frequency. Now calculate the needed phase boost, assuming 60° as a target phase margin:

$$BOOST = -(PHASE + 30°)$$

If the required BOOST is less than 60°, a Type 2 loop can be used successfully, saving two external components.

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BOOST values greater than 60° usually require Type 3 loops for satisfactory performance.

Finally, choose a convenient resistor value for R1 (10k is usually a good value). Now calculate the remaining values:

(K is a constant used in the calculations)

f = chosen crossover frequency

$G = 10^{(GAIN/20)}$ (this converts GAIN in dB to G in absolute gain)

TYPE 2 Loop:

$$K = \tan\left(\frac{BOOST}{2} + 45^\circ\right)$$

$$C2 = \frac{1}{2\pi \bullet f \bullet G \bullet K \bullet R1}$$

$$C1 = C2\left(K^2 - 1\right)$$

$$R2 = \frac{K}{2\pi \bullet f \bullet C1}$$

$$R_B = \frac{V_{REF}(R1)}{V_{OUT} - V_{REF}}$$

TYPE 3 Loop:

$$K = \tan^2\left(\frac{BOOST}{4} + 45^\circ\right)$$

$$C2 = \frac{1}{2\pi \bullet f \bullet G \bullet R1}$$

$$C1 = C2\left(K - 1\right)$$

$$R2 = \frac{\sqrt{K}}{2\pi \bullet f \bullet C1}$$

$$R3 = \frac{R1}{K - 1}$$

$$C3 = \frac{1}{2\pi f\sqrt{K} \bullet R3}$$

$$R_B = \frac{V_{REF}(R1)}{V_{OUT} - V_{REF}}$$

Boost Converter Design

The following sections discuss the use of the LTC3703-5 as a step-up (boost) converter. In boost mode, the LTC3703-5 can step-up output voltages as high as 60V. These sections discuss only the design steps specific to a boost converter. For the design steps common to both a buck and a boost, see the applicable section in the buck mode section. An example of a boost converter circuit is shown in the Typical Applications section. To operate the LTC3703-5 in boost mode, the INV pin should be tied to the V_{CC} voltage (or a voltage above 2V). Note that in boost mode, pulse-skip operation and the line feedforward compensation are disabled.

For a boost converter, the duty cycle of the main switch is:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

For high V_{OUT} to V_{IN} ratios, the maximum V_{OUT} is limited by the LTC3703-5's maximum duty cycle which is typically 93%. The maximum output voltage is therefore:

$$V_{OUT(MAX)} = \frac{V_{IN(MIN)}}{1 - D_{MAX}} \cong 14V_{IN(MIN)}$$

Boost Converter: Inductor Selection

In a boost converter, the average inductor current equals the average input current. Thus, the maximum average inductor current can be calculated from:

$$I_{L(MAX)} = \frac{I_{O(MAX)}}{1 - D_{MAX}} = I_{O(MAX)} \bullet \frac{V_O}{V_{IN(MIN)}}$$

As with a buck converter, choose the ripple current to be 20% to 40% of $I_{L(MAX)}$. The ripple current amplitude then determines the inductor value as follows:

$$L = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

The minimum required saturation current for the inductor is:

$I_{L(SAT)} > I_{L(MAX)} + \Delta I_L/2$

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Boost Converter: Power MOSFET Selection

For information about choosing power MOSFETs for a boost converter, see the Power MOSFET Selection section for the buck converter, since MOSFET selection is similar. However, note that the power dissipation equations for the MOSFETs at maximum output current in a boost converter are:

$$P_{MAIN} = D_{MAX}\left(\frac{I_{MAX}}{1-D_{MAX}}\right)^2(1+\delta)R_{DS(ON)} + \frac{1}{2}V_{OUT}{}^2\left(\frac{I_{MAX}}{1-D_{MAX}}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{CC}-V_{TH(IL)}}+\frac{1}{V_{TH(IL)}}\right](f)$$

$$P_{SYNC} = -\left(\frac{1}{1-D_{MAX}}\right)(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

Boost Converter: Output Capacitor Selection

In boost mode, the output capacitor requirements are more demanding due to the fact that the current waveform is pulsed instead of continuous as in a buck converter. The choice of component(s) is driven by the acceptable ripple voltage which is affected by the ESR, ESL and bulk capacitance as shown in Figure 15. The total output ripple voltage is:

$$\Delta V_{OUT} = I_{O(MAX)}\left(\frac{1}{f\bullet C_{OUT}}+\frac{ESR}{1-D_{MAX}}\right)$$

where the first term is due to the bulk capacitance and second term due to the ESR.

The choice of output capacitor is driven also by the RMS ripple current requirement. The RMS ripple current is:

$$I_{RMS(COUT)} \approx I_{O(MAX)}\bullet\sqrt{\frac{V_O - V_{IN(MIN)}}{V_{IN(MIN)}}}$$

At lower output voltages (less than 30V), it may be possible to satisfy both the output ripple voltage and RMS ripple current requirements with one or more capacitors of a single capacitor type. However, at output voltages above 30V where capacitors with both low ESR and high bulk capacitance are hard to find, the best approach is to use a combination of aluminum and ceramic capacitors (see discussion in Input Capacitor section for the buck converter). With this combination, the ripple voltage can be improved significantly. The low ESR ceremic capacitor will minimize the ESR step, while the electrolytic will supply the required bulk capacitance.

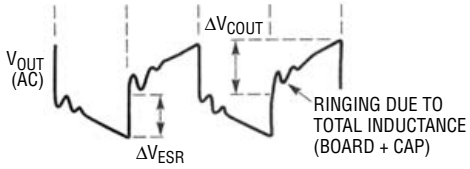

Figure 15. Output Voltage Ripple Waveform for a Boost Converter

Boost Converter: Input Capacitor Selection

The input capacitor of a boost converter is less critical than the output capacitor, due to the fact that the inductor is in series with the input and the input current waveform is continuous. The input voltage source impedance determines the size of the input capacitor, which is typically in the range of 10µF to 100µF. A low ESR capacitor is recommended though not as critical as for the output capacitor.

The RMS input capacitor ripple current for a boost converter is:

$$I_{RMS(CIN)} = 0.3\bullet\frac{V_{IN(MIN)}}{L\bullet f}\bullet D_{MAX}$$

Please note that the input capacitor can see a very high surge current when a battery is suddenly connected to the input of the converter and solid tantalum capacitors can fail catastrophically under these conditions. **Be sure to specify surge-tested capacitors!**

Boost Converter: Current Limit Programming

The LTC3703-5 provides current limiting in boost mode by monitoring the V_{DS} of the main switch during its on-time and comparing it to the voltage at I_{MAX}. To set the current limit, calculate the expected voltage drop across the MOSFET at the maximum desired inductor current and

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maximum junction temperature. The maximum inductor current is a function of both duty cycle and maximum load current, so the limit must be set for the maximum expected duty cycle (minimum V_{IN}) in order to ensure that the current limit does not kick in at loads < $I_{O(MAX)}$:

$$V_{PROG} = \frac{I_{O(MAX)}}{1-D_{MAX}} R_{DS(ON)} (1+\delta)$$

$$= \left(\frac{V_{OUT}}{V_{IN(MIN)}} \right) I_{O(MAX)} \bullet R_{DS(ON)} (1+\delta)$$

Once V_{PROG} is determined, R_{IMAX} is chosen as follows:

$$R_{IMAX} = V_{PROG}/12\mu A$$

Note that in a boost mode architecture, it is only possible to provide protection for "soft" shorts where $V_{OUT} > V_{IN}$. For hard shorts, the inductor current is limited only by the input supply capability. Refer to Current Limit Programming for buck mode for further considerations for current limit programming.

Boost Converter: Feedback Loop/Compensation

Compensating a voltage mode boost converter is unfortunately more difficult than for a buck converter. This is due to an additional right-half plane (RHP) zero that is present in the boost converter but not in a buck. The additional phase lag resulting from the RHP zero is difficult if not impossible to compensate even with a Type 3 loop, so the best approach is usually to roll off the loop gain at a lower frequency than what could be achievable in buck converter.

A typical gain/phase plot of a voltage-mode boost converter is shown in Figure 16. The modulator gain and phase can be measured as described for a buck converter or can be estimated as follows:

$$\text{GAIN (COMP-to-}V_{OUT}\text{ DC gain)} = 20\text{Log}(V_{OUT}^2/V_{IN})$$

$$\text{Dominant Pole: } f_P = \frac{V_{IN}}{V_{OUT}} \bullet \frac{1}{2\pi\sqrt{LC}}$$

Since significant phase shift begins at frequencies above the dominant LC pole, choose a crossover frequency no greater than about half this pole frequency. The gain of the compensation network should equal –GAIN at this frequency so that the overall loop gain is 0dB here. The compensation component to achieve this, using a Type 1 amplifier (see Figure 11), is:

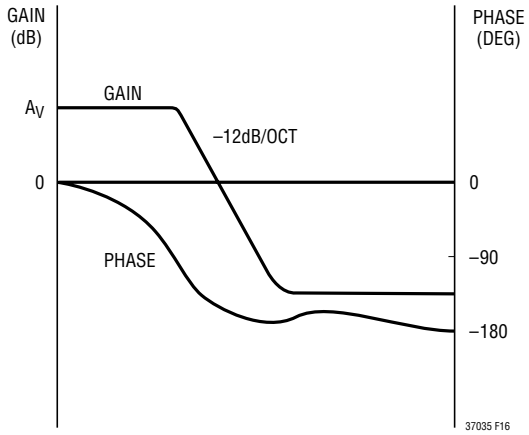

Figure 16. Transfer Function of Boost Modulator

$$G = 10^{-GAIN/20}$$

$$C1 = 1/(2\pi \bullet f \bullet G \bullet R1)$$

Run/Soft-Start Function

The RUN/SS pin is a multipurpose pin that provide a soft-start function and a means to shut down the LTC3703-5. Soft-start reduces the input supply's surge current by gradually increasing the duty cycle and can also be used for power supply sequencing.

Pulling RUN/SS below 1V puts the LTC3703-5 into a low quiescent current shutdown ($I_Q \cong 25\mu A$). This pin can be driven directly from logic as shown in Figure 17. Releasing

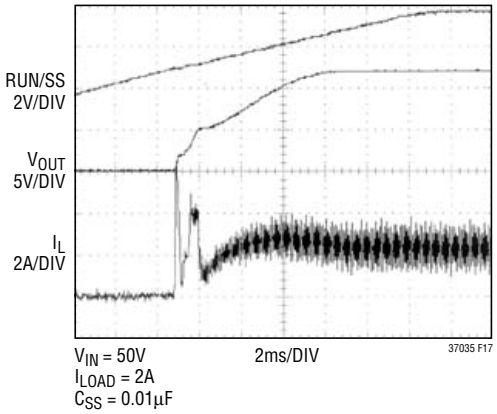

Figure 17. LTC3703-5 Startup Operation

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the RUN/SS pin allows an internal 4μA current source to charge up the soft-start capacitor C_{SS}. When the voltage on RUN/SS reaches 1V, the LTC3703-5 begins operating at its minimum on-time. As the RUN/SS voltage increases from 1V to 3V, the duty cycle is allowed to increase from 0% to 100%. The duty cycle control minimizes input supply inrush current and elimates output voltage overshoot at start-up and ensures current limit protection even with a hard short. The RUN/SS voltage is internally clamped at 4V.

If RUN/SS starts at 0V, the delay before starting is approximately:

$$t_{DELAY,START} = \frac{1V}{4\mu A} C_{SS} = (0.25s/\mu F)C_{SS}$$

plus an additional delay, before the output will reach its regulated value, of:

$$t_{DELAY,REG} \geq \frac{3V - 1V}{4\mu A} C_{SS} = (0.5s/\mu F)C_{SS}$$

The start delay can be reduced by using diode D1 in Figure 18.

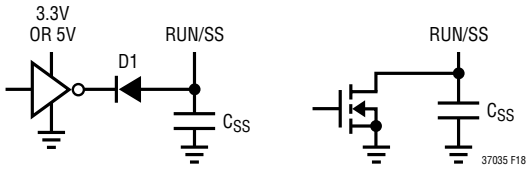

Figure 18. RUN/SS Pin Interfacing

MODE/SYNC Pin (Operating Mode and Secondary Winding Control)

The MODE/SYNC pin is a dual function pin that can be used for enabling or disabling Pulse Skip Mode operation and also as an external clock input for synchronizing the internal oscillator (see next section). Pulse Skip Mode is enabled when the MODE/SYNC pin is above 0.8V and is disabled, i.e. forced continuous, when the pin is below 0.8V.

In addition to providing a logic input to force continuous operation and external synchronization, the MODE/SYNC pin provides a means to regulate a flyback winding output as shown in Figure 9c. The auxiliary output is taken from a second winding on the core of the inductor, converting it to a transformer. The auxiliary output voltage is set by the main output voltage and the turns ratio of the extra winding to the primary winding as follows:

$$V_{SEC} \approx (N + 1)V_{OUT}$$

Since the secondary winding only draws current when the synchronous switch is on, load regulation at the auxiliary output will be relatively good as long as the main output is running in continuous mode. As the load on the primary output drops and the LTC3703-5 switches to Pulse Skip Mode operation, the auxiliary output may not be able to maintain regulation, especially if the load on the auxiliary output remains heavy. To avoid this, the auxiliary output voltage can be divided down with a conventional feedback resistor string with the divided auxiliary output voltage fed back to the MODE/SYNC pin. The MODE/SYNC threshold is trimmed to 800mV with 20mV of hysteresis, allowing precise control of the auxiliary voltage and is set as follows:

$$V_{SEC(MIN)} \approx 0.8V\left(1 + \frac{R1}{R2}\right)$$

where R1 and R2 are shown in Figure 9c.

If the LTC3703-5 is operating in Pulse Skip Mode and the auxiliary output voltage drops below $V_{SEC(MIN)}$, the MODE/SYNC pin will trip and the LTC3703-5 will resume continuous operation regardless of the load on the main output. Thus, the MODE/SYNC pin removes the requirement that power must be drawn from the inductor primary in order to extract power from the auxiliary winding. With the loop in continuous mode (MODE/SYNC < 0.8V), the auxiliary outputs may nominally be loaded without regard to the primary output load.

The following table summarizes the possible states available on the MODE/SYNC pin:

Table 1.

MODE/SYNC Pin	Condition
DC Voltage: 0V to 0.75V	Forced Continuous Current Reversal Enabled
DC Voltage: ≥ 0.87V	Pulse Skip Mode Operation No Current Reversal
Feedback Resistors	Regulating a Secondary Winding
Ext. Clock: 0V to ≥ 2V	Forced Continuous No Current Reversal

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MODE/SYNC Pin (External Synchronization)

The internal LTC3703-5 oscillator can be synchronized to an external oscillator by applying and clocking the MODE/SYNC pin with a signal above $2V_{P-P}$. The internal oscillator locks to the external clock after the second clock transition is received. When external synchronization is detected, LTC3703-5 will operate in forced continuous mode. If an external clock transition is not detected for three successive periods, the internal oscillator will revert to the frequency programmed by the R_{SET} resistor. The internal oscillator can synchronize to frequencies between 100kHz and 600kHz, independent of the frequency programmed by the R_{SET} resistor. However, it is recommended that an R_{SET} resistor be chosen such that the frequency programmed by the R_{SET} resistor is close to the expected frequency of the external clock. In this way, the best converter operation (ripple, component stress, etc) is achieved if the external clock signal is lost.

Minimum On-Time Considerations (Buck Mode)

Minimum on-time $t_{ON(MIN)}$ is the smallest amount of time that the LTC3703-5 is capable of turning the top MOSFET on and off again. It is determined by internal timing delays and the amount of gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \bullet f} > t_{ON(MIN)}$$

where $t_{ON(MIN)}$ is typically 200ns.

If the duty cycle falls below what can be accommodated by the minimum on-time, the LTC3703-5 will begin to skip cycles. The output will be regulated, but the ripple current and ripple voltage will increase. If lower frequency operation is acceptable, the on-time can be increased above $t_{ON(MIN)}$ for the same step-down ratio.

Pin Clearance/Creepage Considerations

The LTC3703-5 is available in two packages (GN16 and G28) both with identical functionality. The GN16 package gives the smallest size solution, however the 0.013" (minimum) space between pins may not provide sufficient PC board trace clearance between high and low voltage pins in higher voltage applications. Where clearance is an issue, the G28 package should be used. The G28 package has 4 unconnected pins between the all adjacent high voltage and low voltage pins, providing 5(0.0106") = 0.053" clearance which will be sufficient for most applications up to 60V. For more information, refer to the printed circuit board design standards described in IPC-2221 (www.ipc.org).

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power (x100%). Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power. It is often useful to analyze the individual losses to determine what is limiting the efficiency and what change would produce the most improvement. Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3703-5 circuits: 1) LTC3703-5 V_{CC} current, 2) MOSFET gate current, 3) I^2R losses and 4) Topside MOSFET transition losses.

1. V_{CC} Supply current. The V_{CC} current is the DC supply current given in the Electrical Characteristics table which powers the internal control circuitry of the LTC3703-5. Total supply current is typically about 2.5mA and usually results in a small (<1%) loss which is proportional to V_{CC}.

2. DRV_{CC} current is MOSFET driver current. This current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched on and then off, a packet of gate charge Q_G moves from DRV_{CC} to ground. The resulting dQ/dt is a current out of the DRV_{CC} supply. In continuous mode, $I_{DRVCC} = f(Q_{G(TOP)} + Q_{G(BOT)})$, where $Q_{G(TOP)}$ and $Q_{G(BOT)}$ are the gate charges of the top and bottom MOSFETs.

3. I^2R losses are predicted from the DC resistances of MOSFETs, the inductor and input and output capacitor ESR. In continuous mode, the average output current flows through L but is "chopped" between the topside

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MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the DCR resistance of L to obtain I^2R losses. For example, if each $R_{DS(ON)}$ = 25mΩ and R_L = 25mΩ, then total resistance is 50mΩ. This results in losses ranging from 1% to 5% as the output current increases from 1A to 5A for a 5V output.

4. Transition losses apply only to the topside MOSFET in buck mode and they become significant when operating at higher input voltages (typically 20V or greater). Transition losses can be estimated from the second term of the P_{MAIN} equation found in the Power MOSFET Selection section.

The transition losses can become very significant at the high end of the LTC3703-5 operating voltage range. To improve efficiency, one may consider lowering the frequency and/or using MOSFETs with lower C_{RSS} at the expense of higher $R_{DS(ON)}$.

Other losses including C_{IN} and C_{OUT} ESR dissipative losses, Schottky conduction losses during dead-time, and inductor core losses generally account for less than 2% total additional loss.

Transient Response

Due to the high gain error amplifier and line feedforward compensation of the LTC3703-5, the output accuracy due to DC variations in input voltage and output load current will be almost negligible. For the few cycles following a load transient, however, the output deviation may be larger while the feedback loop is responding. Consider a typical 48V input to 5V output application circuit, subjected to a 1A to 5A load transient. Initially, the loop is in regulation and the DC current in the output capacitor is zero. Suddenly, an extra 4A (= 5A-1A) flows out of the output capacitor while the inductor is still supplying only 1A. This sudden change will generate a (4A) • (R_{ESR}) voltage step at the output; with a typical 0.015Ω output capacitor ESR, this is a 60mV step at the output.

The feedback loop will respond and will move at the bandwidth allowed by the external compensation network towards a new duty cycle. If the unity gain crossover frequency is set to 50kHz, the COMP pin will get to 60% of the way to 90% duty cycle in 3µs. Now the inductor is seeing 43V across itself for a large portion of the cycle and its current will increase from 1A at a rate set by di/dt = V/L. If the inductor value is 10µH, the peak di/dt will be 43V/10µH or 4.3A/µs. Sometime in the next few micro-seconds after the switch cycle begins, the inductor current will have risen to the 5A level of the load current and the output voltage will stop dropping. At this point, the inductor current will rise somewhat above the level of the output current to replenish the charge lost from the output capacitor during the load transient. With a properly compensated loop, the entire recovery time will be inside of 10µs.

Most loads care only about the maximum deviation from ideal, which occurs somewhere in the first two cycles after the load step hits. During this time, the output capacitor does all the work until the inductor and control loop regain control. The initial drop (or rise if the load steps down) is entirely controlled by the ESR of the capacitor and amounts to most of the total voltage drop. To minimize this drop, choose a low ESR capacitor and/or parallel multiple capacitors at the output. The capacitance value accounts for the rest of the voltage drop until the inductor current rises. With most output capacitors, several devices paralleled to get the ESR down will have so much capacitance that this drop term is negligible. Ceramic capacitors are an exception; a small ceramic capacitor can have suitably low ESR with relatively small values of capacitance, making this second drop term more significant.

Optimizing Loop Compensation

Loop compensation has a fundamental impact on transient recovery time, the time it takes the LTC3703-5 to recover after the output voltage has dropped due to a load step. Optimizing loop compensation entails maintaining the highest possible loop bandwidth while ensuring loop stability. The feedback component selection section describes in detail the techniques used to design an optimized Type 3 feedback loop, appropriate for most LTC3703-5 systems.

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Measurement Techniques

Measuring transient response presents a challenge in two respects: obtaining an accurate measurement and generating a suitable transient to test the circuit. Output measurements should be taken with a scope probe directly across the output capacitor. Proper high frequency probing techniques should be used. In particular, don't use the 6" ground lead that comes with the probe! Use an adapter that fits on the tip of the probe and has a short ground clip to ensure that inductance in the ground path doesn't cause a bigger spike than the transient signal being measured. Conveniently, the typical probe tip ground clip is spaced just right to span the leads of a typical output capacitor.

Now that we know how to measure the signal, we need to have something to measure. The ideal situation is to use the actual load for the test and switch it on and off while watching the output. If this isn't convenient, a current step generator is needed. This generator needs to be able to turn on and off in nanoseconds to simulate a typical switching logic load, so stray inductance and long clip leads between the LTC3703-5 and the transient generator must be minimized.

Figure 19 shows an example of a simple transient generator. Be sure to use a noninductive resistor as the load element—many power resistors use an inductive spiral pattern and are not suitable for use here. A simple solution is to take ten 1/4W film resistors and wire them in parallel

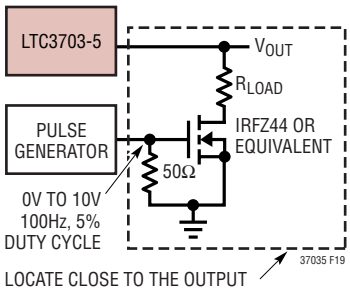

Figure 19. Transient Load Generator

to get the desired value. This gives a noninductive resistive load which can dissipate 2.5W continuously or 50W if pulsed with a 5% duty cycle, enough for most LTC3703-5 circuits. Solder the MOSFET and the resistor(s) as close to the output of the LTC3703-5 circuit as possible and set up the signal generator to pulse at a 100Hz rate with a 5% duty cycle. This pulses the LTC3703-5 with 500µs transients10ms apart, adequate for viewing the entire transient recovery time for both positive and negative transitions while keeping the load resistor cool.

Design Example

As a design example, take a supply with the following specifications: V_{IN} = 20V to 60V (48V nominal), V_{OUT} = 12V ±5%, $I_{OUT(MAX)}$ = 10A, f=250kHz. First, calculate R_{SET} to give the 250kHz operating frequency:

R_{SET} = 7100/(250-25) = 31.6k

Next, choose the inductor value for about 40% ripple current at maximum V_{IN}:

$$L = \frac{12V}{(250kHz)(0.4)(10A)}\left(1-\frac{12}{60}\right) = 10\mu H$$

With 10µH inductor, ripple current will vary from 1.9A to 3.8A (19% to 38%) over the input supply range.

Next, verify that the minimum on-time is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MIN)}(f)} = \frac{12}{60(250kHz)} = 800ns$$

which is above the LTC3703-5's 200ns minimum on-time.

Next, choose the top and bottom MOSFET switch. Since the drain of each MOSFET will see the full supply voltage 60V(max) plus any ringing, choose a 60V MOSFET. Si7850DP has a 60V BV_{DSS}, $R_{DS(ON)}$ = 22mΩ(max), δ = 0.007/°C, C_{MILLER} = (9nC – 3nC)/30V = 200pF, $V_{GS(MILLER)}$ = 3.8V, θ_{JA} = 20°C/W. The power dissipation can be

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estimated at maximum input voltage, assuming a junction temperature of 100°C (30°C above an ambient of 70°C):

$$P_{MAIN} = \frac{12}{60}(10)^2[1+0.007(100-25)](0.022)$$
$$+(60)^2\left(\frac{10}{2}\right)(2)(200pF)\bullet\left(\frac{1}{10-3.8}+\frac{1}{3.8}\right)(250k)$$
$$=0.67W+0.76W=1.43W$$

And double check the assumed T_J in the MOSFET:

T_J = 70°C + (1.43W)(20°C/W) = 99°C

Since the synchronous MOSFET will be conducting over twice as long each period (almost 100% of the period in short circuit) as the top MOSFET, use two Si7850DP MOSFETs on the bottom:

$$P_{SYNC} = \left(\frac{60-12}{60}\right)(10)^2[1+0.007(100-25)]\bullet$$
$$\left(\frac{0.022}{2}\right)=1.34W$$

T_J = 70°C + (1.34W)(20°C/W) = 97°C

Next, set the current limit resistor. Since I_{MAX} = 10A, the limit should be set such that the minimum current limit is >10A. Minimum current limit occurs at maximum $R_{DS(ON)}$. Using the above calculation for bottom MOSFET T_J, the max $R_{DS(ON)}$ = (22mΩ/2) [1 + 0.007 (97-25)] = 16.5mΩ

Therefore, I_{MAX} pin voltage should be set to (10A)(0.0165) = 0.165V. The R_{SET} resistor can now be chosen to be 0.165V/12µA = 14kΩ.

C_{IN} is chosen for an RMS current rating of about 5A (I_{MAX}/2) at 85°C. For the output capacitor, two low ESR OS-CON capacitors (18mΩ each) are used to minimize output voltage changes due to inductor current ripple and load steps. The ripple voltage will be:

$\Delta V_{OUT(RIPPLE)} = \Delta I_{L(MAX)}$ (ESR) = (4A)(0.018Ω/2)
= 36mV

However, a 0A to 10A load step will cause an output voltage change of up to:

$\Delta V_{OUT(STEP)} = \Delta I_{LOAD(ESR)}$ = (10A)(0.009Ω)
= 90mV

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3703-5. These items are also illustrated graphically in the layout diagram of Figure 20. For layout of a boost mode converter, layout is similar with V_{IN} and V_{OUT} swapped. Check the following in your layout:

1. Keep the signal and power grounds separate. The signal ground consists of the LTC3703-5 GND pin, the ground return of C_{VCC}, and the (–) terminal of V_{OUT}. The power ground consists of the Schottky diode anode, the source of the bottom side MOSFET, and the (–) terminal of the input capacitor and DRV_{CC} capacitor. Connect the signal and power grounds together at the (–) terminal of the output capacitor. Also, try to connect the (–) terminal of the output capacitor as close as possible to the (–) terminals of the input and DRV_{CC} capacitor and away from the Schottky loop described in (2).

2. The high di/dt loop formed by the top N-channel MOSFET, the bottom MOSFET and the C_{IN} capacitor should have short leads and PC trace lengths to minimize high frequency noise and voltage stress from inductive ringing.

3. Connect the drain of the top side MOSFET directly to the (+) plate of C_{IN}, and connect the source of the bottom side MOSFET directly to the (–) terminal of C_{IN}. This capacitor provides the AC current to the MOSFETs.

4. Place the ceramic C_{DRVCC} decoupling capacitor immediately next to the IC, between DRV_{CC} and BGRTN. This capacitor carries the MOSFET drivers' current peaks. Likewise the C_B capacitor should also be next to the IC between BOOST and SW.

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5. Place the small-signal components away from high frequency switching nodes (BOOST, SW, TG, and BG). In the layout shown in Figure 20, all the small signal components have been placed on one side of the IC and all of the power components have been placed on the other. This also helps keep the signal ground and power ground isolated.

6. A separate decoupling capacitor for the supply, V_{CC}, is useful with an RC filter between the DRV_{CC} supply and V_{CC} pin to filter any noise injected by the drivers. Connect this capacitor close to the IC, between the V_{CC} and GND pins and keep the ground side of the V_{CC} capacitor (signal ground) isolated from the ground side of the DRV_{CC} capacitor (power ground).

7. For optimum load regulation and true remote sensing, the top of the output resistor divider should connect independently to the top of the output capacitor (Kelvin connection), staying away from any high dV/dt traces. Place the divider resistors near the LTC3703-5 in order to keep the high impedance FB node short.

8. For applications with multiple switching power converters connected to the same input supply, make sure that the input filter capacitor for the LTC3703-5 is not shared with other converters. AC input current from another converter could cause substantial input voltage ripple, and this could interfere with the operation of the LTC3703-5. A few inches of PC trace or wire ($L \cong 100nH$) between C_{IN} of the LTC3703-5 and the actual source V_{IN} should be sufficient to prevent input noise interference problems.

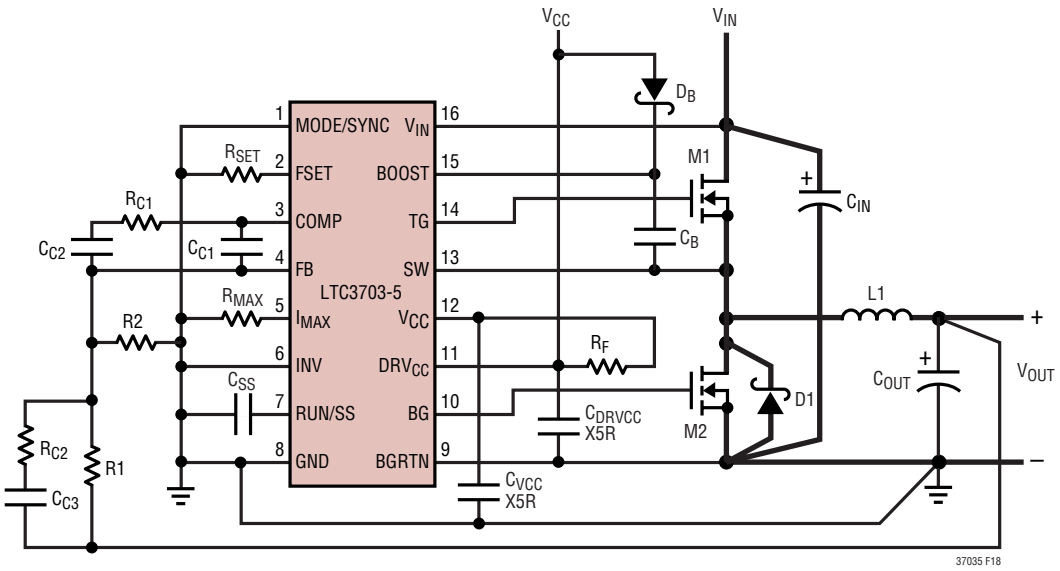
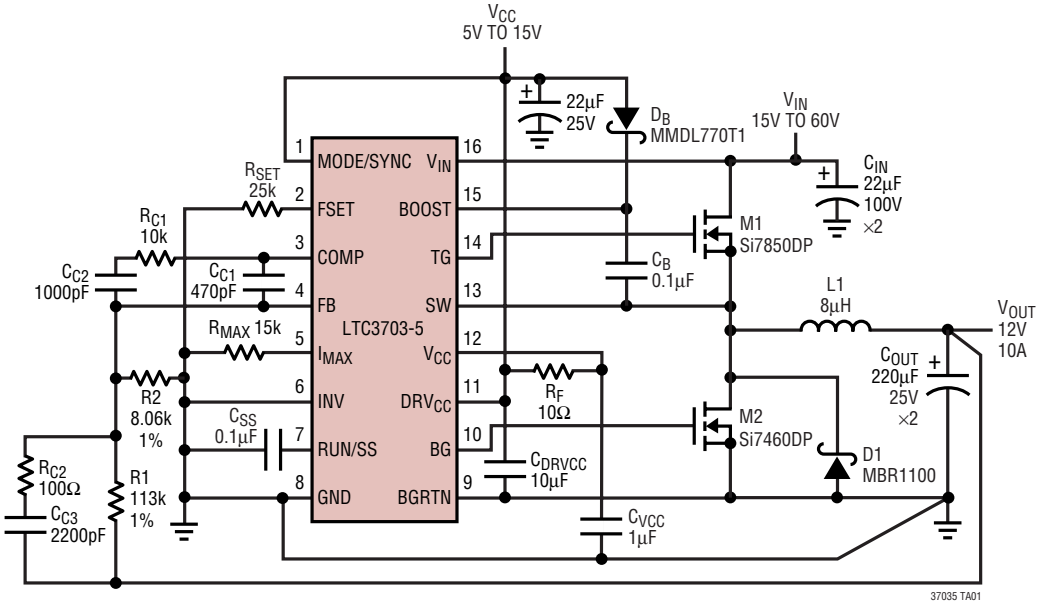


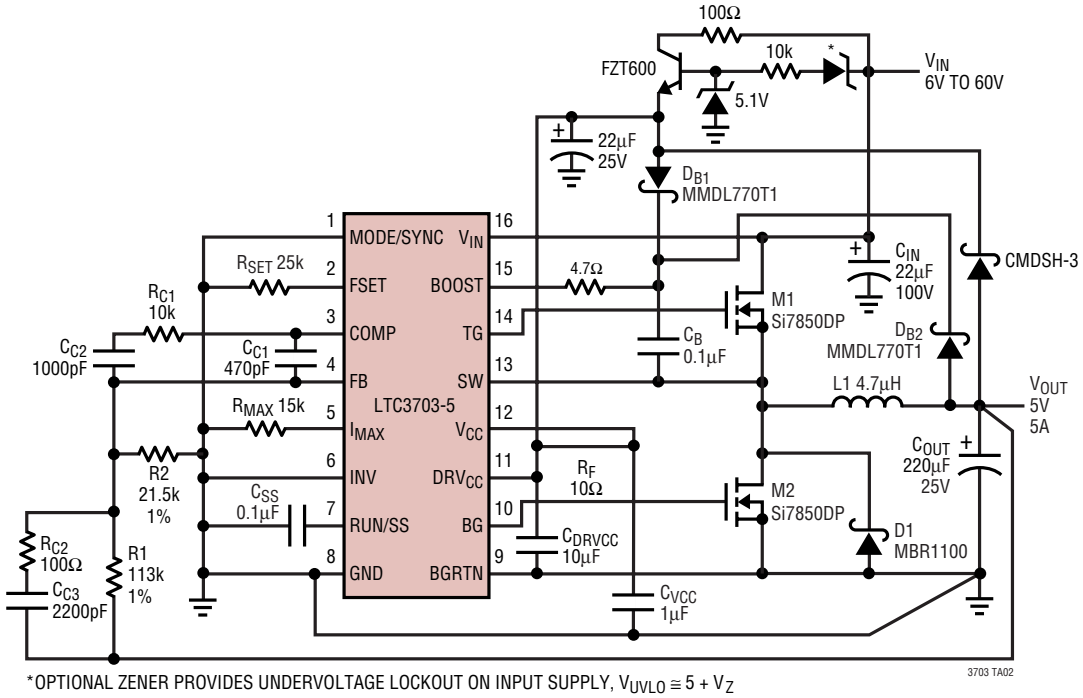
Figure 20. LTC3703-5 Buck Converter Suggested Layout

TYPICAL APPLICATIONS

15V-60V Input Voltage to 12V/10A Step-Down Converter with Pulse Skip Mode Enabled



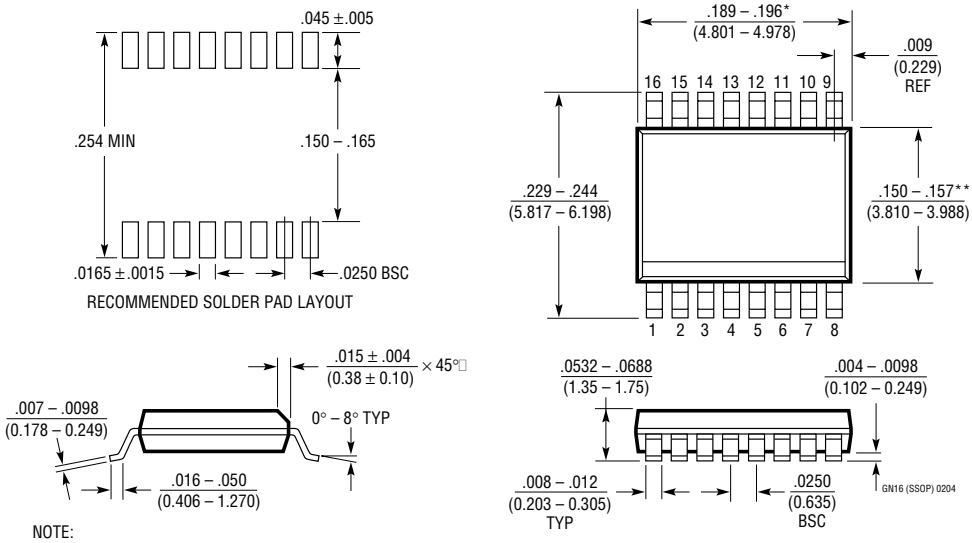
Single Input Supply 5V/5A Output Step-Down Converter



*OPTIONAL ZENER PROVIDES UNDERVOLTAGE LOCKOUT ON INPUT SUPPLY, $V_{UVLO} \cong 5 + V_Z$

PACKAGE DESCRIPTION

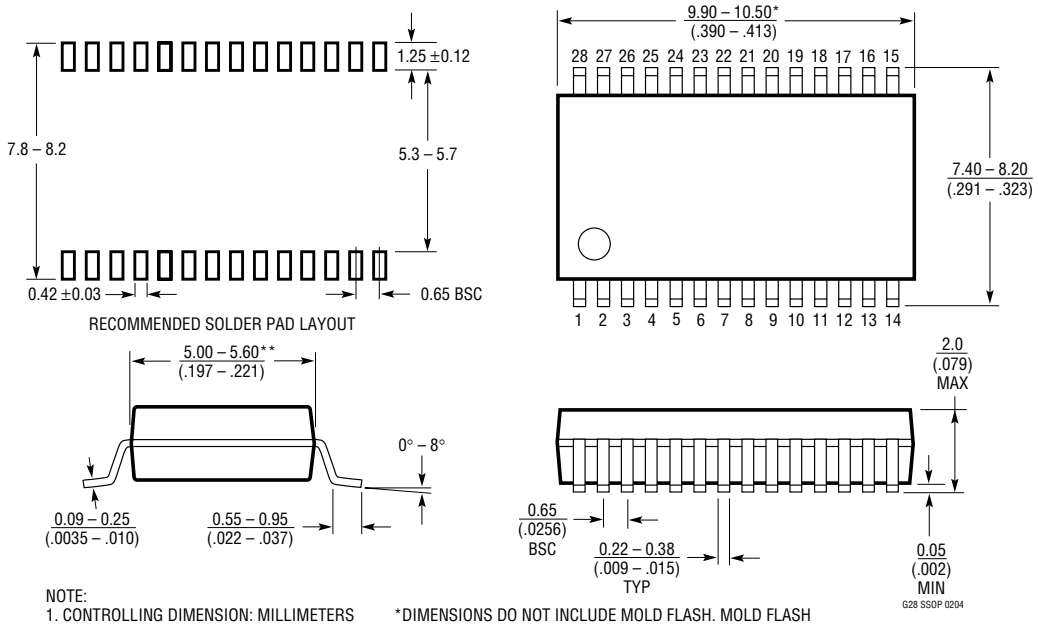
GN Package
16-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)

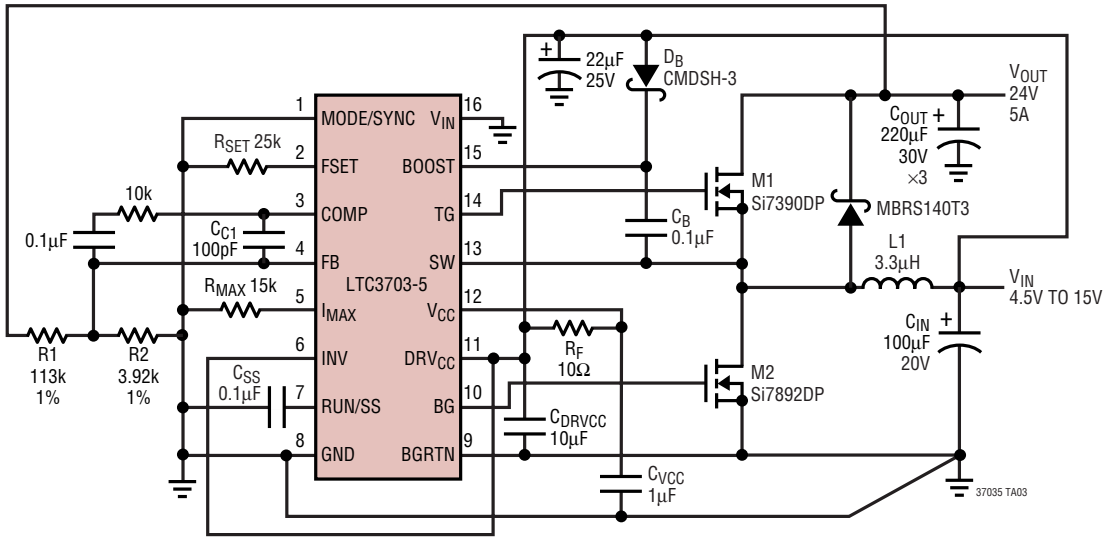


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{(\text{INCHES})}$
3. DRAWING NOT TO SCALE

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

TYPICAL APPLICATION

5V to 24V/5A Synchronous Boost Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1074HV/LT1076HV	Monolithic 5A/2A Step-Down DC/DC Converters	V_{IN} up to 60V, TO-220 and DD Packages
LT1339	High Power Synchronous DC/DC Controller	V_{IN} up to 60V, Drivers 10,000pF Gate Capacitance, $I_{OUT} \leq 20A$
LTC1702A	Dual, 2-Phase Synchronous DC/DC Controller	550kHz Operation, No R_{SENSE}, $3V \leq V_{IN} \leq 7V$, $I_{OUT} \leq 20A$
LTC1735	Synchronous Step-Down DC/DC Controller	$3.5V \leq V_{IN} \leq 36V$, $0.8V \leq V_{OUT} \leq 6V$, Current Mode, $I_{OUT} \leq 20A$
LTC1778	No R_{SENSE} Synchronous DC/DC Controller	$4V \leq V_{IN} \leq 36V$, Fast Transient Response, Current Mode, $I_{OUT} \leq 20A$
LT1956	Monolithic 1.5A, 500kHz Step-Down Regulator	$5.5V \leq V_{IN} \leq 60V$, 2.5mA Supply Current, 16-Pin SSOP
LT3010	50mA, 3V to 80V Linear Regulator	$1.275V \leq V_{OUT} \leq 60V$, No Protection Diode Required, 8-Lead MSOP
LT3430/LT3431	Monolithic 3A, 200kHz/500kHz Step-Down Regulator	$5.5V \leq V_{IN} \leq 60V$, 0.1Ω Saturation Switch, 16-Pin SSOP
LT3433	Monolithic Step-Up/Step-Down DC/DC Converter	$4V \leq V_{IN} \leq 60V$, 500mA Switch, Automatic Step-Up/Step-Down, Single Inductor
LTC®3703	100V Synchronous DC/DC Controller	V_{IN} up to 100V, 9.3V to 15V Gate Drive Supply
LT3800	60V Synchronous DC/DC Controller	$4V \leq V_{IN} \leq 60V$, Current Mode, $1.23V \leq V_{OUT} \leq 36V$

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