

West Bridge[®]: Astoria[™] USB and Mass Storage Peripheral Controller

Features

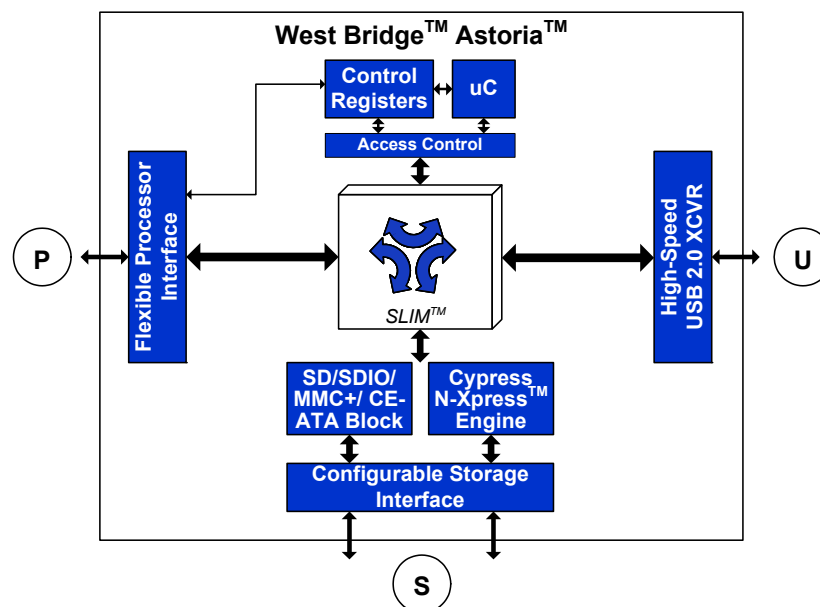
- Multimedia device support
 - Up to two SD, SDIO, MMC, MMC+, and CE-ATA devices
- Supports Microsoft[®] Media Transfer Protocol (MTP) with optimized data throughput
- Simultaneous Link to Independent Multimedia (SLIM[®]) architecture, enabling simultaneous and independent data paths between the processor and USB, and between the USB and mass storage
- High-speed USB at 480 Mbps
 - USB 2.0 compliant
 - Integrated USB switch
 - Integrated USB 2.0 transceiver, smart serial interface engine
 - 16 programmable endpoints
- GPIF (General Programmable Interface)
 - Allows direct connection to most parallel interface
 - Programmable waveform descriptors and configuration registers to define waveforms
 - Supports multiple Ready (RDY) inputs and Control (CTL) outputs
- Flexible processor interface that supports:
 - Multiplexing and nonmultiplexing address and data interface
 - SRAM interface
 - Pseudo cellular random access memory (CRAM) interface (Antioch interface)
 - Pseudo NAND flash interface

- SPI (slave mode) interface
- Direct memory access (DMA) slave support
- FlexBoot
 - Processor can boot from the processor interface port
- Ultra low power, 1.8-V core operation
- Low power modes
- Small footprint:
 - 3.91 × 3.91 × 0.55 mm 81-ball WLCSP (SP and Lite SP)
 - 6 × 6 × 1.0 mm 100-ball VFBGA
 - 10 × 10 × 1.20 mm 121-ball FBGA
- Supports I²C boot and processor boot
- Selectable clock input frequencies
 - 19.2 MHz, 24 MHz, 26 MHz, and 48 MHz

Applications

- Cellular phones
- Portable media players
- Personal digital assistants
- Portable navigation devices
- Digital cameras
- POS terminals
- Portable video recorders
- Data cards and wireless dongles

Logic Block Diagram



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Functional Overview

Turbo-MTP Support

Turbo-MTP is an implementation of Microsoft's MTP enabled by West Bridge. In the current generation of MTP-enabled mobile phones, all protocol packets need to be handled by the main processor. West Bridge Turbo-MTP switches these packet types and sends only control packets to the processor, while data payloads are written directly to mass storage, thereby bringing the high performance of West Bridge to MTP. For more information refer to the application note [Optimizing Performance using West Bridge® Controllers with Turbo-MTP](#).

SLIM Architecture

The SLIM architecture enables three different interfaces (P-port, S-port, and U-port) to connect to one another independently.

With this architecture, connecting a device using Astoria to a PC through USB does not disturb any of the functions of the device. The device can still access mass storage at the same time as the PC synchronizes with the main processor.

The SLIM architecture enables new usage models in which a PC can access a mass storage device independent of the main processor or enumerate access to both the mass storage and the main processor at the same time.

In a handset, this typically enables using the phone as a thumb drive, downloading media files to the phone while still having full functionality available on the phone, or using the same phone as a modem to connect the PC to the web.

8051 Microprocessor

The 8051 microprocessor embedded in Astoria does basic transaction management for all the transactions between P-Port, S-Port, and U-Port. The 8051 does not reside in the data path; it manages the path. The data path is optimized for performance. The 8051 executes firmware that supports SD, SDIO, MMC+, and CE-ATA devices at the S-Port.

Configuration and Status Registers

The West Bridge Astoria device includes configuration and status registers that are accessible as memory mapped registers through the processor interface. The configuration registers allow the system to specify certain Astoria behaviors. For example, it is able to mask certain status registers from raising an interrupt. The status registers convey various status such as the addresses of buffers for read operations.

Processor Interface (P-Port)

Communication with the external processor is realized through a dedicated processor interface. This interface is configured to support different interface standards. This interface supports multiplexing and nonmultiplexing address or data bus in both synchronous and asynchronous pseudo CRAM-mapped, and nonmultiplexing address or data asynchronous SRAM-mapped memory accesses. The interface also can be configured to a pseudo NAND interface to support the processor's NAND interface. In addition, this interface can be configured to support SPI slave. Asynchronous accesses can reach a bandwidth of up to 66.7 MBps. Synchronous accesses can be performed at 33 MHz across 16 bits for up to 66.7 MBps bandwidth. The

P-Port of the WLCSP package only supports PNAND and SPI interface.

The memory address is decoded to access any of the multiple endpoint buffers inside Astoria. These endpoints serve as buffers for data between each pair of ports, for example, between the processor port and the USB port. The processor writes and reads into these buffers through the memory interface.

Access to these buffers is controlled by either using a DMA protocol or using an interrupt to the main processor. These two modes are configurable by the external processor. The 81-ball WLCSP package only supports interrupt.

As a DMA slave, Astoria generates a DMA request signal to signify to the main processor that a specific buffer is ready to be read from or written to. The external processor monitors this signal and polls Astoria for the specific buffers ready for read or write. It then performs the appropriate read or write operations on the buffer through the processor interface. This way, the external processor only deals with the buffers to access a multitude of storage devices connected to Astoria.

In the interrupt mode, Astoria communicates important buffer status changes to the external processor using an interrupt signal. The external processor then polls Astoria for the specific buffers ready for read or write and it performs the appropriate read or write operations through the processor interface.

FlexBoot

FlexBoot is an optional feature that Astoria emulates a NAND Flash device. In this optional feature, the P-Port is configured as pseudo NAND interface. The processor can download its boot image through the P-Port.

When P-Port is configured to pseudo NAND interface, it supports two operation modes:

- Logic NAND Access (LNA) mode
- Non-Logic NAND Access (non-LNA) mode

LNA refers to the mode of operation where Astoria emulates a NAND flash device. This mode is designed for systems that require booting of the system processor from a NAND Flash device. In this type of application, the system processor can communicate to Astoria using common NAND commands to boot from a NAND Flash connected to Astoria's S-port. In this mode of operation, Astoria mimics a real NAND device and allows the system processor to use its internal boot-ROM to boot from Astoria, as it boots from a NAND Flash.

In the non-LNA mode of operation, the system processor interfaces with Astoria using standard NAND interface, but does not use standard NAND commands. In this mode, Astoria responds to a subset of NAND commands. The system processor uses a set of APIs provided by Cypress to communicate through its NAND controller to Astoria. For details, refer to the application note ["Interfacing To West Bridge™ Astoria's™ Pseudo-NAND Processor Port"](#).

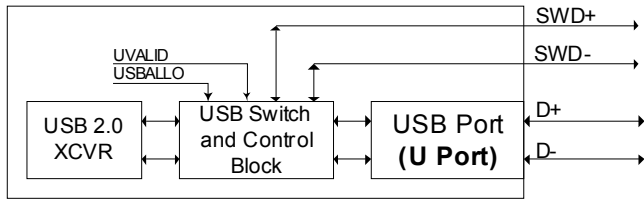
USB Interface (U-Port)

In accordance with the USB 2.0 specification, Astoria can operate in both full speed and high speed USB modes. The USB interface consists of the USB transceiver and can be accessed by both the P-Port and the S-Port.

The Astoria USB interface supports programmable CONTROL/BULK/INTERRUPT/ISOCRONOUS endpoints.

Astoria also has an integrated USB switch (see [Figure 1](#)) that allows interfacing to an external full speed USB PHY.

Figure 1. U-Port With Switch and Control Block



Mass Storage Support (S-Port)

The S-Port is configurable in five different interface modes:

- Simultaneously supporting an SD/SDIO/MMC+/CE-ATA port and an GPIF
- Supporting two SD/SDIO/MMC+/CE-ATA ports
- Supporting SD/SDIO/MMC+/CE-ATA port and GPIO
- Supporting GPIF and GPIO
- Supporting GPIO

These configurations are controlled by the 8051 firmware.

S-Port Configuration Modes

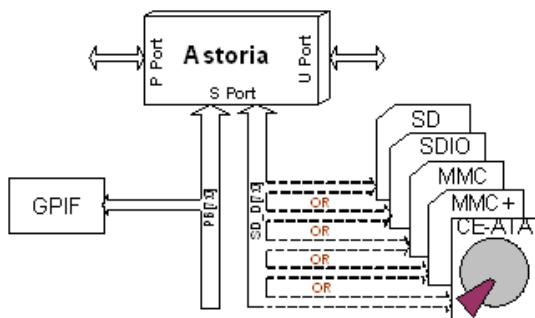
The S Port is configurable in six different interface modes:

- GPIF and SD/SDIO/MMC/CE-ATA interface mode
- Dual SD/SDIO/MMC/CE-ATA interface mode
- SD/SDIO/MMC/CE-ATA and GPIO interface mode
- GPIF and GPIO interface mode
- GPIO interface mode

GPIF and SD/SDIO/MMC/CE-ATA Interface Mode

This mode configures the S-Port into GPIF and SD/SDIO/MMC/MMC+/CE-ATA ports as shown in [Figure 2](#). The SD/SDIO/MMC/MMC+/CE-ATA port supports either SD, SDIO, MMC, MMC+, or CE-ATA device.

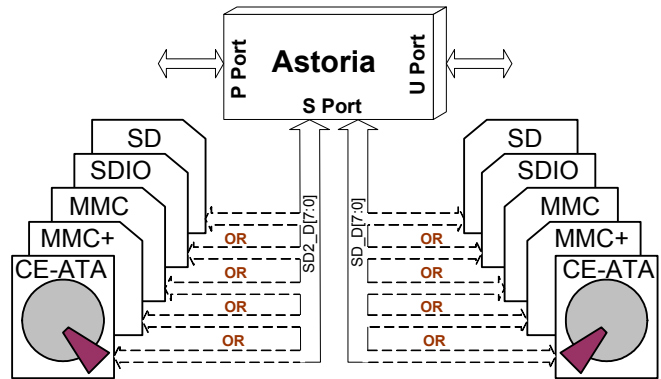
Figure 2. GPIF and SD/SDIO/MMC/CE-ATA Interface Mode



Dual SD/SDIO/MMC/CE-ATA Interface Mode

The dual SD/SDIO/MMC/MMC+/CE-ATA interface mode configures the S-Port for up to two SD/SDIO/MMC/MMC+/CE-ATA port as shown in [Figure 3](#). Each SD/SDIO/MMC/MMC+/CE-ATA port is independent and supports different SD, SDIO, MMC, MMC+, or CE-ATA devices.

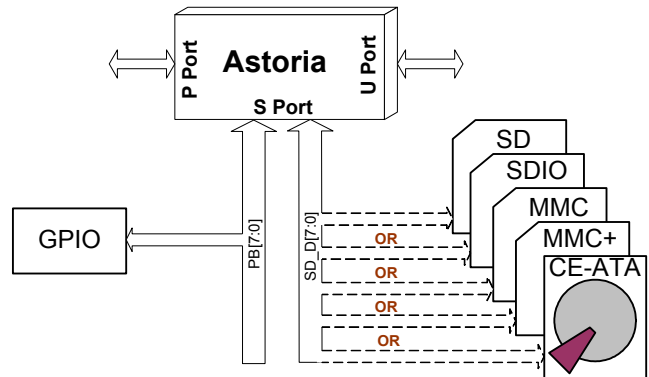
Figure 3. Dual SD/SDIO/MMC/CE-ATA Interface Mode



SD/SDIO/MMC/CE-ATA and GPIO Interface

The SD/SDIO/MMC/MMC+/CE-ATA and GPIO interface mode configures the S-Port to support SD/SDIO/MMC/MMC+/CE-ATA device and GPIOs as shown in [Figure 4](#). Each GPIO is configured as either input or output independently. The processor accesses those GPIO through the P-Port driver's API.

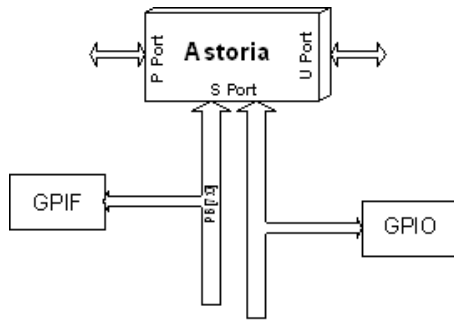
Figure 4. SD/SDIO/MMC/CE-ATA and GPIO Interface Mode



GIPIF and GPIO Interface

The GIPIF and GPIO interface mode configure the S-Port to support GIPIF and GPIO as shown in Figure 5. Each GPIO is configured as either input or output independently. The processor accesses those GPIO through the P-Port driver's API.

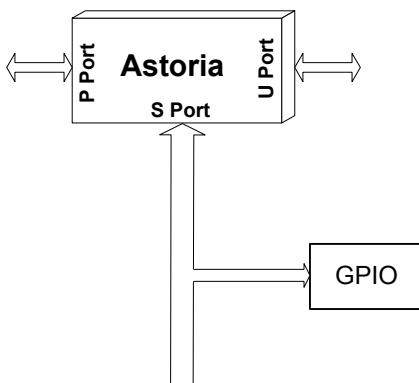
Figure 5. GIPIF and GPIO Interface Mode



GPIO Interface Mode

The GPIO interface mode configures the S-Port to all GPIO as shown in Figure 6. Each GPIO is configured as either input or output independently. The processor accesses those GPIO through the P-Port driver's API.

Figure 6. GPIO Interface Mode



SD/SDIO/MMC+/CE-ATA Port (S-Port)

When Astoria is configured with firmware to support SD, SDIO, MMC+, and CE-ATA, this interface supports:

- The Multimedia Card System Specification, MMCA Technical Committee, Version 4.1
- SD Memory Card Specification – Part 1, Physical Layer Specification, SD Group, Version 1.10, October 15, 2004
- SD Memory Card Specification – Part 1, Physical Layer Specification, SD Group, Version 2.0, May 9, 2006

- SD Specifications – Part E1 SDIO Specification, Version 1.10, August 18, 2004

- CE-ATA Specification – CE-ATA Digital Protocol, CE-ATA Committee, Version 1.1, September, 2005

West Bridge Astoria provides support for 1-bit and 4-bit SD; SDIO cards; 1-bit, 4-bit, and 8-bit MMC; MMC+ cards; and CE-ATA drive. For the SD, SDIO, MMC/MMC Plus, and CE-ATA, this block supports one card for one physical bus interface.

Astoria supports SD commands including the multisector program command that are handled by the API.

GPIO Port (S-Port)

The GPIO in S-Port is configurable as either input or output direction independently. The processor accesses the GPIO through the P-Port driver's API.

Clocking

Astoria allows connection of a crystal between the XTALIN and XTALOUT pins or an external clock at the XTALIN pin. The 81-ball WLCSP package only supports the external clock. The power supply level at the crystal supply XVDDQ determines whether a crystal or a clock is provided. If XVDDQ is detected to be 1.8 V, Astoria assumes that a clock input is provided. For a crystal to be connected, XVDDQ must be 3.3 V.

Note Clock inputs at 3.3 V level are not supported.

Astoria's 100-ball VFPGA package supports external crystal and clock inputs at 19.2, 24, and 26 MHz frequencies. At 48 MHz, only clock inputs are supported. The 81-ball SPWLCSP only supports 19.2 and 26 MHz external clock input. The 81-ball Lite SP WLCSP only supports 26 MHz external clock or crystal input. The crystal or clock frequency selection is shown in Table 1 on page 6, Table 2 on page 6, and Table 3 on page 6.

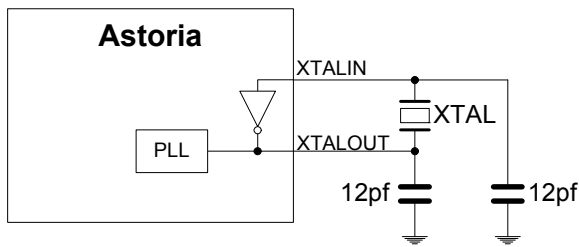
The XTALIN frequency is independent of the clock and data rate of the 8051 microprocessor or any of the device interfaces (including P-Port and S-Port). The internal PLL applies the proper clock multiply option depending on the input frequency.

For applications that use an external clock source to drive XTALIN, the XTALOUT pin must be left floating. The external clock source must also stop high or low and not toggle, to achieve the lowest possible current consumption. The requirements for an external clock source are shown in Table 4 on page 6.

Astoria has an on-chip oscillator circuit that uses an external 19.2, 24, and 26 MHz (± 150 ppm) crystal with the following characteristics:

- Parallel resonant
- Fundamental mode
- 1 mW drive level
- 12 pF (5% tolerance) load capacitors
- 150 ppm

Figure 7. Crystal Configuration



* 12 pF capacitor values assumes a trace capacitance of 3 pF per side on a four layer FR4 PCA

Table 1. 100-ball FVBGA Clock Selection

XTALSCLC[1]	XTALSCLC[0]	Freq	Crystal/Clock
0	0	19.2 MHz	Crystal/Clock
0	1	24 MHz	Crystal/Clock
1	0	48 MHz	Clock
1	1	26 MHz	Crystal/Clock

Table 2. 81-ball SP WLCSP Clock Selection

XTALSCLC	Freq	Crystal/Clock
0	19.2 MHz	Clock
1	26 MHz	Clock

Table 3. 81-ball Lite SP WLCSP Clock Supports 26 MHz

XTALSCLC	Freq	Crystal/Clock
NA	26 MHz	Clock or Crystal

Table 4. External Clock Requirements

Parameter	Description	Specification		Unit
		Min	Max	
Vn (AVDDQ)	Supply voltage noise at frequencies < 50 MHz	–	20	mV p-p
PN_100	Input phase noise at 100 Hz	–	–75	dBc/Hz
PN_1k	Input phase noise at 1 kHz offset	–	–104	dBc/Hz
PN_10k	Input phase noise at 10 kHz offset	–	–120	dBc/Hz
PN_100k	Input phase noise at 100 kHz offset	–	–128	dBc/Hz
PN_1M	Input phase noise at 1 MHz offset	–	–130	dBc/Hz
	Duty cycle	30	70	%
	Maximum frequency deviation	–	150	ppm
	Overshoot	–	3	%
	Undershoot	–	–3	%

Power Domains

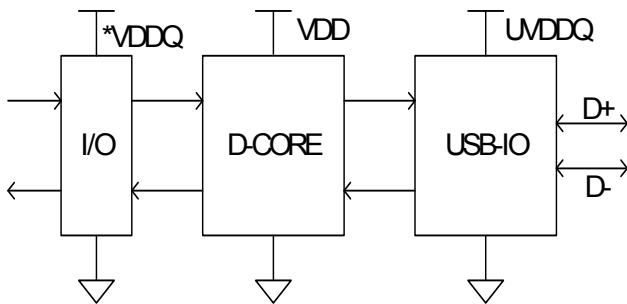
Astoria has multiple power domains that serve different purposes within the chip.

- VDDQ refers to a group of four independent supply domains for the digital I/Os. The nominal voltage level on these supplies are 1.8 V, 2.5 V, or 3.3 V. The three separate I/O power domains are:
 - PVDDQ – P-Port Processor interface I/O
 - SNVDDQ – S-Port GPIF interface I/O
 - SSVDDQ – S-Port SD interface I/O
 - GVDDQ – Other miscellaneous I/O
- UVDDQ is the 3.3-V nominal supply for the USB I/O and some analog circuits. It also supplies power to the USB transceiver
- VDD33 supply is required for the power sequence control circuits. For more details, see [Pin Assignments on page 9](#).

- VDD is the supply voltage for the logic core. The nominal supply voltage level is 1.8 V. This supplies the core logic circuits. The same supply must also be used for AVDDQ
- AVDDQ is the 1.8 V supply for PLL and USB serializer analog components. The same supply must also be used for VDD. The maximum permitted noise on AVDDQ is 20 mV p-p
- XVDDQ is the clock I/O supply; 3.3 V for XTAL or 1.8 V for an external clock

Noise guideline for all supplies except AVDDQ is a maximum of 100 mV p-p. All I/O supplies of Astoria must be ON when a system is active even if Astoria is not in use. The core VDD can also be deactivated at any time to preserve power if there is a minimum impedance of 1 kΩ between the VDD pin and ground. All I/Os tristate when the core is disabled.

Figure 8. Astoria Power Supply Domains



Power Supply Sequence

The power supplies are independently sequenced without damaging the part. All power supplies must be up and stable before the device operates. If the supplies are not stable, the remaining domains are in low power (standby) state.

Power Modes

In addition to the normal operating mode, Astoria contains several low power states when normal operation is not required.

Normal Mode

Normal mode is the mode in which Astoria is fully functional. In this mode, data transfer functions described in this document are performed.

Suspend Mode

This mode is entered internally by 8051 (the external processor only initiates entry into this mode through Mailbox commands). This mode is exited by the D+ bus going low, GPIO[0] going to a pre-determined state or by asserting CE# LOW.

In Astoria's suspend mode:

- The clocks are shut off
- All I/Os maintain their previous state
- Core power supply must be retained
- The states of the configuration registers, endpoint buffers, and the program RAM are maintained. All transactions must be complete before Astoria enters suspend mode (state of outstanding transactions are not preserved)
- The firmware resumes its operation from where it was suspended because the program counter is not reset
- Only inputs that are sensed are RESET#, GPIO[0]/SD_CD, GPIO[1]/SD2_CD, SD_D3, SD2_D3, D+, and CE#. The last three are wake up sources (each can be individually enabled or disabled)
- Hard Reset can be performed by asserting the RESET# input, and Astoria is initialized

Standby Mode

Standby mode is a low-power state. This is the lowest power mode of Astoria while still maintaining external supply levels.

This mode is entered through the deassertion of the WAKEUP input pin or through internal register settings. To leave this mode, assert the WAKEUP, CE#, and RESET#; change state of GPIO[0]/SD_CD, GPIO[1]/SD2_CD, SD_D3, and SD2_D3.

In this mode all configuration register settings and program RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed in values. Therefore, the external processor must ensure that the required data is read before placing Astoria in the standby mode.

In the standby mode:

- The program counter is reset on waking up from standby mode
- All outputs are tristated and I/O is placed in input only configuration. Values of I/Os in standby mode are listed in the pin assignments table
- Core power supply must be retained
- Hard Reset can be performed by asserting the RESET# input, and Astoria is initialized
- PLL is disabled
- USB switches the SWD+/SWD- to D+/D-

Core Power Down Mode

The core power supply V_{DD} is powered down in this state. Because AVDDQ is tied to the same supply as V_{DD} , it is also powered down. The endpoint buffers, configuration registers, and program RAM do not maintain state. All VDDQ power supplies (except AVDDQ) must be ON and not power down in this mode. VDD33 must also remain ON. It has an option that the UVDDQ can be powered down or stay ON while V_{DD} is powered down when SWD+/SWD- are not connected. The UVDDQ cannot be powered down when SWD+/SWD- is connected, or V_{DD} is active. When UVDDQ is powered down, D+/D- cannot be driven by an external device.

In the WLCSP package, AVDDQ is internally tied to XVDDQ. Due to this, the clock input at XTALIN must be brought to a steady low level prior to entry into Core Power Down Mode. In the WLCSP package, VDD33 is tied to UVDDQ internally. UVDDQ must be ON during the core power down mode

The core power down mode has two power down options:

- Core only power down – VDD power down
- Core and USB power down – VDD and UVDDQ are both powered down. In this option, SWD+/SWD- are not connected and cannot be driven by an external device

In these power down options, the endpoint buffers, configuration registers, or the program RAM do not maintain state. It is necessary to reload the firmware on exiting from this mode. All VDDQ power supplies must be ON and not powered down in this mode.

In the 82-ball WLCSP package, in the core power down mode, the USB switches the SWD+/SWD- to D+/D-.

Packages and Interface Options

Astoria provides one 100-ball VFBGA, one 100-ball BGA, one 121-ball FBGA and two types of 81-ball WLCSP packages. The two WLCSP packages are SP WLCSP and Lite SP WLCSP. These two packages have different interface options as listed in Table 5. The 100-ball VFBGA/BGA package pin list is listed in Table 6 on page 9, the 81-ball SP CSP package is listed in Table 10 on page 21, and the 81-ball Lite SP CSP package in Table 11 on page 24.

Table 5. Interface Options for 100-ball VFBGA, 81-ball SP, and 81-ball Lite SP

Package	P-Port						S-Port				Clock		
	PCRAM	SRAM	ADM	PNAND	I ² C	SPI	SD1	SD2	GPIF	GPIO	Ext CLK	Crystal	Freq. (MHz)
100-ball BGA / VFBGA	√	√	√	√	√	√	√	√	√	√	√	√	19.2, 24, 26, 48
121-ball FBGA	√	√	√	√	√	√	√	√	√	√	√	√	19.2, 24, 26, 48
81-ball SP WLCSP				√	√	√	√	√	√	√	√		19.2, 26
81-ball Lite SP WLCSP		√	√	√	√		√			√	√	√	26

Pin Assignments

Table 6. Astoria 100-ball VFBGA Package Pin Assignments

	Pin Name										Pin Description	Power Domain			
	Ball #	PCRAM Non-Multiplexing	I/O	Address / Data bus Multiplexing (ADM)	I/O	SRAM	I/O	PNAND	I/O	SPI			I/O		
P-Port	J2	CLK (pull low in Asyn mode)	I	CLK (pull low in Async mode)	I	Ext pull low	I	Ext pull low	I	SCK	I	Clock	PVDDQ VGND		
	G1	CE#	I	CE#	I	CE#	I	CE#	I	SS#	I	CE# or SPI Slave Select			
	H3	A7	I	Ext pull up	I	A7	I	A7 ≥ 1:SBD A7 ≥ 0:LBD	I	Ext pull up	I	Addr. Bus 7			
	H2	A6	I	SDA	I	A6	I	SDA	I/O	SDA	I/O	A6 or I ² C data			
	H1	A5	I	SCL	I	A5	I	SCL	I/O	SCL	I/O	A5 or I ² C clock			
	J3	A4	I	Ext pull up	I	A4	I	WP#	I	Ext pull up	I	A4 or PNAND WP			
	J1	A3	I	A3 = 0 (Ext pull low)	I	A3	I	A3 = 0 (Ext pull low)	I	A3 = 1 (Ext pull up)	I	A3			
	K3	A2	I	A2 = 1 (Ext pull up)	I	A2	I	A2 = 0 (Ext pull low)	I	A2 = 0 (Ext pull low)	I	A2			
	K2	A1	I	Ext pull up	I	A1	I	RB#	O	Ext pull up	I	A1 or PNAND R/B#			
	K1	A0	I	Ext pull up	I	A0	I	CLE	I	Ext pull up	I	A0 or PNAND CLE			
	G2	DQ[15]	I/O	AD[15]	I/O	DQ[15]	I/O	I/O[15]	I/O	Ext pull up	I	D15, AD15, or I/O15			
	G3	DQ[14]	I/O	AD[14]	I/O	DQ[14]	I/O	I/O[14]	I/O	Ext pull up	I	D14, AD14, or I/O14			
	F1	DQ[13]	I/O	AD[13]	I/O	DQ[13]	I/O	I/O[13]	I/O	Ext pull up	I	D13, AD13, or I/O13			
	F2	DQ[12]	I/O	AD[12]	I/O	DQ[12]	I/O	I/O[12]	I/O	Ext pull up	I	D12, AD12, or I/O12			
	F3	DQ[11]	I/O	AD[11]	I/O	DQ[11]	I/O	I/O[11]	I/O	Ext pull up	I	D11, AD11, or I/O11			
	E1	DQ[10]	I/O	AD[10]	I/O	DQ[10]	I/O	I/O[10]	I/O	Ext pull up	I	D10, AD10, or I/O10			
	E2	DQ[9]	I/O	AD[9]	I/O	DQ[9]	I/O	I/O[9]	I/O	Ext pull up	I	D9, AD9, or I/O9			
	E3	DQ[8]	I/O	AD[8]	I/O	DQ[8]	I/O	I/O[8]	I/O	Ext pull up	I	D8, AD8, or I/O8			
	D1	DQ[7]	I/O	AD[7]	I/O	DQ[7]	I/O	I/O[7]	I/O	Ext pull up	I	D7, AD7, or I/O7			
	D2	DQ[6]	I/O	AD[6]	I/O	DQ[6]	I/O	I/O[6]	I/O	Ext pull up	I	D6, AD6, or I/O6			
	D3	DQ[5]	I/O	AD[5]	I/O	DQ[5]	I/O	I/O[5]	I/O	Ext pull up	I	D5, AD5, or I/O5			
	C1	DQ[4]	I/O	AD[4]	I/O	DQ[4]	I/O	I/O[4]	I/O	Ext pull up	I	D4, AD4, or I/O4			
	C2	DQ[3]	I/O	AD[3]	I/O	DQ[3]	I/O	I/O[3]	I/O	Ext pull up	I	D3, AD3, or I/O3			
	C3	DQ[2]	I/O	AD[2]	I/O	DQ[2]	I/O	I/O[2]	I/O	Ext pull up	I	D2, AD2, or I/O2			
	B1	DQ[1]	I/O	AD[1]	I/O	DQ[1]	I/O	I/O[1]	I/O	SDO	O	SPI SDO, AD1or D1			
	B2	DQ[0]	I/O	AD[0]	I/O	DQ[0]	I/O	I/O[0]	I/O	SDI	I	SPI SDI, AD0, or D0			
	A1	ADV#	I	ADV#	I		I	ALE	I	Ext pull up	I	Address Valid			
	B3	OE#	I	OE#	I	OE#	I	RE#	I	Ext pull up	I	Output Enable			
	A2	WE#	I	WE#	I	WE#	I	WE#	I	Ext pull up	I	WE#			
	DRQ & Int	A3	INT#	O	INT#	O	INT#	O	INT#	O	SINT#	O		INT Request	GVDDQ VGND
		A4	DRQ#	O	DRQ#	O	DRQ#	O	DRQ#	O	N/C	O		DMA Request	
B4		DACK#	I	DACK#	I	DACK#	I	DACK#	I	Ext pull up	I	DMA Acknowledgement			
U-Port	A5	D+							I/O/Z			USB D+	UVDDQ UVSSQ		
	A6	D-							I/O/Z			USB D-			
	A7	SWD+							I/O/Z			USB Switch DP			
	C6	SWD-							I/O/Z			USB Switch DM			

Table 6. Astoria 100-ball VFBGA Package Pin Assignments (continued)

		Pin Name										Pin Description	Power Domain
Ball #	Double SDIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO Configuration	I/O	GPIF Configuration	I/O	GPIF & GPIO Configuration	I/O			
S-Port	G9	SD_D[7]	I/O	SD_D[7]	I/O	PD[7] (GPIO)	I/O	GPIF_DATA[15]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO or GPIF Data	SSVDDQ VGND
	G10	SD_D[6]	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	GPIF_DATA[14]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F9	SD_D[5]	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	GPIF_DATA[13]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F10	SD_D[4]	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	GPIF_DATA[12]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E9	SD_D[3]	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	GPIF_DATA[11]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E10	SD_D[2]	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	GPIF_DATA[10]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D9	SD_D[1]	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	GPIF_DATA[9]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D10	SD_D[0]	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	GPIF_DATA[8]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F8	SD_CLK	O	SD_CLK	O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	SD Clock or GPIO	
	G8	SD_CMD	I/O	SD_CMD	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	SD CMD or GPIO	
	H8	SD_POW		SD_POW		PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	SD Power or GPIO	
	H10	SD_WP	I	SD_WP	I	N/C		N/C		PC[5] (GPIO)		SD Write Protect	
	K7	SD2_D[7]	I/O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	GPIF_DATA[7]	I/O	GPIF_DATA[7]	I/O	SD2 Data or GPIO or GPIF Data	SNVDDQ VGND
	K8	SD2_D[6]	I/O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	GPIF_DATA[6]	I/O	GPIF_DATA[6]	I/O	SD2 Data or GPIO or GPIF Data	
	J8	SD2_D[5]	I/O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	GPIF_DATA[5]	I/O	GPIF_DATA[5]	I/O	SD2 Data or GPIO or GPIF Data	
	K9	SD2_D[4]	I/O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	GPIF_DATA[4]	I/O	GPIF_DATA[4]	I/O	SD2 Data or GPIO or GPIF Data	
	J9	SD2_D[3]	I/O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	GPIF_DATA[3]	I/O	GPIF_DATA[3]	I/O	SD2 Data or GPIO or GPIF Data	
	H9	SD2_D[2]	I/O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	GPIF_DATA[2]	I/O	GPIF_DATA[2]	I/O	SD2 Data or GPIO or GPIF Data	
	K10	SD2_D[1]	I/O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	GPIF_DATA[1]	I/O	GPIF_DATA[1]	I/O	SD2 Data or GPIO or GPIF Data	
	J10	SD2_D[0]	I/O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	GPIF_DATA[0]	I/O	GPIF_DATA[0]	I/O	SD2 Data or GPIO or GPIF Data	
	K6	SD2_CLK	O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	SD2 Clock or GPIO	
	J6	SD2_CMD	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	SD2 CMD or GPIO	
	J5	SD2_POW	O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	SD2 Power or GPIO	
	K4	N/C	O	N/C	O	N/C	O	GPIF_CTL[1]	O	GPIF_CTL[1]	O	GPIF Control Signal	
	H6	N/C	O	N/C	O	N/C	O	GPIF_CTL[0]	O	GPIF_CTL[0]	O	GPIF Control Signal	
J7	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	GPIO		
J4	N/C	I	N/C	I	N/C	I	GPIF_RDY[0]	O	GPIF_RDY[0]	O	GPIF Ready Signal		
K5	SD2_WP	O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	SD Write Protect or GPIO		
Other	B10	RESETOUT	O	RESETOUT	O	RESETOUT	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT / GPIF_RDY[1]	O	Reset Out	GVDDQ VGND
	C9	SD2_CD	I/O I	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	GPIO or SD2 CD	
	D8	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	GPIO or SD CD	
	C10	RESET#									I	RESET	
	C7	WAKEUP									I	Wake Up Signal	

Table 6. Astoria 100-ball VFBGA Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Conf	C5	XTALSLC[1]	I	Clock Select 1	GVDDQ VGND
	C4	XTALSLC[0]		Clock Select 0	
	E8	TEST[2]	I	Test Cfg 2	
	C8	TEST[1]		Test Cfg 1	
	D7	TEST[0]		Test Cfg 0	
Clock	A8	XTALIN	I	Crystal/Clock IN	XVDDQ VGND
	B8	XTALOUT	O	Crystal Out	
Power	D4, H4	PVDDQ	Power	Processor I/F VDD	
	H5	SNVDDQ	Power	GPiF VDD	
	B5	UVDDQ	Power	USB VDD	
	H7	SSVDDQ	Power	SDIO VDD	
	D6	GVDDQ	Power	Misc I/O VDD	
	B9	AVDDQ	Power	Analog VDD	
	B7	XVDDQ	Power	Crystal VDD	
	D5, G4, G5, G6, G7, F7	VDD	Power	Core VDD	
	A10	VDD33	Power	Independent 3.3 V	
	B6	UVSSQ	Power	USB GND	
	A9	AVSSQ	Power	Analog GND	
	E4, E5, E6, E7, F4, F5, F6	VGND	Power	Core GND	

Table 7. Astoria CYWB0224ABS 121-ball FBGA Package Pin Assignments

		Pin Name										Pin Description	Power Domain
Ball #	PCRAM Non Multiplexing	I/O	Addr/Data bus Multiplexing (ADM)	I/O	SRAM	I/O	PNAND	I/O	SPI	I/O			
J2	CLK (pull-low in Asyn mode)	I	CLK (pull-low in Asyn mode)	I	Ext pull-low	I	Ext pull-low	I	SCK	I	Clock	PVDDQ VGND	
G1	CE#	I	CE#	I	CE#	I	CE#	I	SS#	I	CE# or SPI Slave Select		
H3	A7	I	Ext pull-up	I	A7	I	A7 ≥ 1: SBD A7 ≥ 0: LBD	I	Ext pull-up	I	Addr. Bus 7		
H2	A6	I	SDA	I	A6	I	SDA	I/O	SDA	I/O	A6 or I ² C data		
H1	A5	I	SCL	I	A5	I	SCL	I/O	SCL	I/O	A5 or I ² C clock		
J3	A4	I	Ext pull-up	I	A4	I	WP#	I	Ext pull-up	I	A4 or PNAND WP		
J1	A3	I	A3 = 0 (Ext pull-low)	I	A3	I	A3 = 0 (Ext pull-low)	I	A3 = 1 (Ext pull-up)	I	A3		
K3	A2	I	A2 = 1 (Ext pull-up)	I	A2	I	A2 = 0 (Ext pull-low)	I	A2 = 0 (Ext pull-low)	I	A2		
K2	A1	I	Ext pull-up	I	A1	I	RB#	O	Ext pull-up	I	A1 or PNAND R/B#		
K1	A0	I	Ext pull-up	I	A0	I	CLE	I	Ext pull-up	I	A0 or PNAND CLE		
P-Port	G2	DQ[15]	I/O	AD[15]	I/O	DQ[15]	I/O	I/O[15]	I/O	Ext pull-up	I		D15, AD15, or I/O15
	G3	DQ[14]	I/O	AD[14]	I/O	DQ[14]	I/O	I/O[14]	I/O	Ext pull-up	I		D14, AD14, or I/O14
	F1	DQ[13]	I/O	AD[13]	I/O	DQ[13]	I/O	I/O[13]	I/O	Ext pull-up	I		D13, AD13, or I/O13
	F2	DQ[12]	I/O	AD[12]	I/O	DQ[12]	I/O	I/O[12]	I/O	Ext pull-up	I		D12, AD12, or I/O12
	F3	DQ[11]	I/O	AD[11]	I/O	DQ[11]	I/O	I/O[11]	I/O	Ext pull-up	I		D11, AD11, or I/O11
	E1	DQ[10]	I/O	AD[10]	I/O	DQ[10]	I/O	I/O[10]	I/O	Ext pull-up	I		D10, AD10, or I/O10
	E2	DQ[9]	I/O	AD[9]	I/O	DQ[9]	I/O	I/O[9]	I/O	Ext pull-up	I		D9, AD9, or I/O9
	E3	DQ[8]	I/O	AD[8]	I/O	DQ[8]	I/O	I/O[8]	I/O	Ext pull-up	I		D8, AD8, or I/O8
	D1	DQ[7]	I/O	AD[7]	I/O	DQ[7]	I/O	I/O[7]	I/O	Ext pull-up	I		D7, AD7, or I/O7
	D2	DQ[6]	I/O	AD[6]	I/O	DQ[6]	I/O	I/O[6]	I/O	Ext pull-up	I		D6, AD6, or I/O6
	D3	DQ[5]	I/O	AD[5]	I/O	DQ[5]	I/O	I/O[5]	I/O	Ext pull-up	I	D5, AD5, or I/O5	
	C1	DQ[4]	I/O	AD[4]	I/O	DQ[4]	I/O	I/O[4]	I/O	Ext pull-up	I	D4, AD4, or I/O4	
	C2	DQ[3]	I/O	AD[3]	I/O	DQ[3]	I/O	I/O[3]	I/O	Ext pull-up	I	D3, AD3, or I/O3	
	C3	DQ[2]	I/O	AD[2]	I/O	DQ[2]	I/O	I/O[2]	I/O	Ext pull-up	I	D2, AD2, or I/O2	
	B1	DQ[1]	I/O	AD[1]	I/O	DQ[1]	I/O	I/O[1]	I/O	SDO	O	SPI SDO, AD1or D1	
	B2	DQ[0]	I/O	AD[0]	I/O	DQ[0]	I/O	I/O[0]	I/O	SDI	I	SPI SDI, AD0, or D0	
A1	ADV#	I	ADV#	I		I	ALE	I	Ext pull-up	I	Address Valid		
B3	OE#	I	OE#	I	OE#	I	RE#	I	Ext pull-up	I	Output Enable		
A2	WE#	I	WE#	I	WE#	I	WE#	I	Ext pull-up	I	WE#		
DRQ & Int	A3	INT#	O	INT#	O	INT#	O	INT#	O	SINT#	O	INT Request	GVDDQ VGND
	A4	DRQ#	O	DRQ#	O	DRQ#	O	DRQ#	O	N/C	O	DMA Request	
	B4	DACK#	I	DACK#	I	DACK#	I	DACK#	I	Ext pull-up	I	DMA Acknowledgement	
U-Port	A5	D+								I/O/Z	USB D+	UVDDQ UVSSQ	
	A6	D-								I/O/Z	USB D-		
	A7	SWD+								I/O/Z	USB Switch DP		
	C6	SWD-								I/O/Z	USB Switch DM		

Table 7. Astoria CYWB0224ABS 121-ball FBGA Package Pin Assignments (continued)

		Pin Name										Pin Description	Power Domain
Ball #	Double SDIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO Configuration	I/O	GIPIF Configuration	I/O	GIPIF & GPIO Configuration	I/O			
S-Port	G9	SD_D[7]	I/O	SD_D[7]	I/O	PD[7] (GPIO)	I/O	GIPIF_DATA[15]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO or GIPIF Data	SSVDDQ VGND
	G10	SD_D[6]	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	GIPIF_DATA[14]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO or GIPIF Data	
	F9	SD_D[5]	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	GIPIF_DATA[13]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO or GIPIF Data	
	F10	SD_D[4]	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	GIPIF_DATA[12]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO or GIPIF Data	
	E9	SD_D[3]	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	GIPIF_DATA[11]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO or GIPIF Data	
	E10	SD_D[2]	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	GIPIF_DATA[10]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO or GIPIF Data	
	D9	SD_D[1]	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	GIPIF_DATA[9]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO or GIPIF Data	
	D10	SD_D[0]	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	GIPIF_DATA[8]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO or GIPIF Data	
	F8	SD_CLK	O	SD_CLK	O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	SD Clock or GPIO	
	G8	SD_CMD	I/O	SD_CMD	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	SD CMD or GPIO	
	H8	SD_POW		SD_POW		PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	SD Power or GPIO	
	H10	SD_WP	I	SD_WP	I	N/C	I	N/C		PC[5] (GPIO)		SD Write Protect	
	K7	SD2_D[7]	I/O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	GIPIF_DATA[7]	I/O	GIPIF_DATA[7]	I/O	SD2 Data or GPIO or GIPIF Data	SNVDDQ VGND
	K8	SD2_D[6]	I/O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	GIPIF_DATA[6]	I/O	GIPIF_DATA[6]	I/O	SD2 Data or GPIO or GIPIF Data	
	J8	SD2_D[5]	I/O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	GIPIF_DATA[5]	I/O	GIPIF_DATA[5]	I/O	SD2 Data or GPIO or GIPIF Data	
	K9	SD2_D[4]	I/O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	GIPIF_DATA[4]	I/O	GIPIF_DATA[4]	I/O	SD2 Data or GPIO or GIPIF Data	
	J9	SD2_D[3]	I/O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	GIPIF_DATA[3]	I/O	GIPIF_DATA[3]	I/O	SD2 Data or GPIO or GIPIF Data	
	H9	SD2_D[2]	I/O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	GIPIF_DATA[2]	I/O	GIPIF_DATA[2]	I/O	SD2 Data or GPIO or GIPIF Data	
	K10	SD2_D[1]	I/O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	GIPIF_DATA[1]	I/O	GIPIF_DATA[1]	I/O	SD2 Data or GPIO or GIPIF Data	
	J10	SD2_D[0]	I/O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	GIPIF_DATA[0]	I/O	GIPIF_DATA[0]	I/O	SD2 Data or GPIO or GIPIF Data	
	K6	SD2_CLK	O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	SD2 Clock or GPIO	
	J6	SD2_CMD	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA [7] (GPIO)	I/O	SD2 CMD or GPIO	
	J5	SD2_POW	O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	SD2 Power or GPIO	
	K4	N/C	O	N/C	O	N/C	O	GIPIF_CTL[1]	O	GIPIF_CTL[1]	O	GIPIF Control Signal	
	H6	N/C	O	N/C	O	N/C	O	GIPIF_CTL[0]	O	GIPIF_CTL[0]	O	GIPIF Control Signal	
J7	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	GPIO		
J4	N/C	I	N/C	I	N/C	I	GIPIF_RDY[0]	O	GIPIF_RDY[0]	O	GIPIF Ready Signal		
K5	SD2_WP	O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	SD Write Protect or GPIO		
Other	B10	RESETOUT	O	RESETOUT	O	RESETOUT	O	RESETOUT / GIPIF_RDY[1]	O	RESETOUT / GIPIF_RDY[1]	O	RESETOUT	GVDDQ VGND
	C9	SD2_CD	I/O I	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	GPIO or SD2 CD	
	D8	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	GPIO or SD CD	
	C10	RESET#									I	RESET	
	C7	WAKEUP									I	Wake Up Signal	

Table 7. Astoria CYWB0224ABS 121-ball FBGA Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Conf	C5	XTALSLC[1]	I	Clock Select 1	GVDDQ VGND
	C4	XTALSLC[0]		Clock Select 0	
	E8	TEST[2]	I	Test Cfg 2	
	C8	TEST[1]		Test Cfg 1	
	D7	TEST[0]		Test Cfg 0	
Clock	A8	XTALIN	I	Crystal / Clock IN	XVDDQ VGND
	B8	XTALOUT	O	Crystal Out	
Power	D4 H4	PVDDQ	Power	Processor I/F VDD	
	H5	SNVDDQ	Power	GPIO VDD	
	B5	UVDDQ	Power	USB VDD	
	H7	SSVDDQ	Power	SDIO VDD	
	D6	GVDDQ	Power	Misc I/O VDD	
	B9	AVDDQ	Power	Analog VDD	
	B7	XVDDQ	Power	Crystal VDD	
	D5, G4, G5, G6, G7, F7	VDD	Power	Core VDD	
	A10	VDD33	Power	Independent 3.3 V	
	B6	UVSSQ	Power	USB GND	
	A9	AVSSQ	Power	Analog GND	
	E4, E5, E6, E7, F4, F5, F6	VGND	Power	Core GND	

Table 8. Astoria CYWB0220ABS 121-ball FBGA Package Pin Assignments

		Pin Name										Pin Description	Power Domain
Ball #	PCRAM Non Multiplexing	I/O	Addr/Data bus Multiplexing (ADM)	I/O	SRAM	I/O	PNAND	I/O	SPI	I/O			
J2	CLK (pull-low in Asyn mode)	I	CLK (pull-low in Asyn mode)	I	Ext pull-low	I	Ext pull-low	I	SCK	I	Clock	PVDDQ VGND	
G1	CE#	I	CE#	I	CE#	I	CE#	I	SS#	I	CE# or SPI Slave Select		
H3	A7	I	Ext pull-up	I	A7	I	A7 ≥ 1: SBD A7 ≥ 0: LBD	I	Ext pull-up	I	Addr. Bus 7		
H2	A6	I	SDA	I	A6	I	SDA	I/O	SDA	I/O	A6 or I ² C data		
H1	A5	I	SCL	I	A5	I	SCL	I/O	SCL	I/O	A5 or I ² C clock		
J3	A4	I	Ext pull-up	I	A4	I	WP#	I	Ext pull-up	I	A4 or PNAND WP		
J1	A3	I	A3 = 0 (Ext pull-low)	I	A3	I	A3 = 0 (Ext pull-low)	I	A3 = 1 (Ext pull-up)	I	A3		
K3	A2	I	A2 = 1 (Ext pull-up)	I	A2	I	A2 = 0 (Ext pull-low)	I	A2 = 0 (Ext pull-low)	I	A2		
K2	A1	I	Ext pull-up	I	A1	I	RB#	O	Ext pull-up	I	A1 or PNAND R/B#		
K1	A0	I	Ext pull-up	I	A0	I	CLE	I	Ext pull-up	I	A0 or PNAND CLE		
P-Port	G2	DQ[15]	I/O	AD[15]	I/O	DQ[15]	I/O	I/O[15]	I/O	Ext pull-up	I	D15, AD15, or I/O15	
	G3	DQ[14]	I/O	AD[14]	I/O	DQ[14]	I/O	I/O[14]	I/O	Ext pull-up	I	D14, AD14, or I/O14	
	F1	DQ[13]	I/O	AD[13]	I/O	DQ[13]	I/O	I/O[13]	I/O	Ext pull-up	I	D13, AD13, or I/O13	
	F2	DQ[12]	I/O	AD[12]	I/O	DQ[12]	I/O	I/O[12]	I/O	Ext pull-up	I	D12, AD12, or I/O12	
	F3	DQ[11]	I/O	AD[11]	I/O	DQ[11]	I/O	I/O[11]	I/O	Ext pull-up	I	D11, AD11, or I/O11	
	E1	DQ[10]	I/O	AD[10]	I/O	DQ[10]	I/O	I/O[10]	I/O	Ext pull-up	I	D10, AD10, or I/O10	
	E2	DQ[9]	I/O	AD[9]	I/O	DQ[9]	I/O	I/O[9]	I/O	Ext pull-up	I	D9, AD9, or I/O9	
	E3	DQ[8]	I/O	AD[8]	I/O	DQ[8]	I/O	I/O[8]	I/O	Ext pull-up	I	D8, AD8, or I/O8	
	D1	DQ[7]	I/O	AD[7]	I/O	DQ[7]	I/O	I/O[7]	I/O	Ext pull-up	I	D7, AD7, or I/O7	
	D2	DQ[6]	I/O	AD[6]	I/O	DQ[6]	I/O	I/O[6]	I/O	Ext pull-up	I	D6, AD6, or I/O6	
	D3	DQ[5]	I/O	AD[5]	I/O	DQ[5]	I/O	I/O[5]	I/O	Ext pull-up	I	D5, AD5, or I/O5	
	C1	DQ[4]	I/O	AD[4]	I/O	DQ[4]	I/O	I/O[4]	I/O	Ext pull-up	I	D4, AD4, or I/O4	
	C2	DQ[3]	I/O	AD[3]	I/O	DQ[3]	I/O	I/O[3]	I/O	Ext pull-up	I	D3, AD3, or I/O3	
	C3	DQ[2]	I/O	AD[2]	I/O	DQ[2]	I/O	I/O[2]	I/O	Ext pull-up	I	D2, AD2, or I/O2	
	B1	DQ[1]	I/O	AD[1]	I/O	DQ[1]	I/O	I/O[1]	I/O	SDO	O	SPI SDO, AD1or D1	
	B2	DQ[0]	I/O	AD[0]	I/O	DQ[0]	I/O	I/O[0]	I/O	SDI	I	SPI SDI, AD0, or D0	
	A1	ADV#	I	ADV#	I		I	ALE	I	Ext pull-up	I	Address Valid	
B3	OE#	I	OE#	I	OE#	I	RE#	I	Ext pull-up	I	Output Enable		
A2	WE#	I	WE#	I	WE#	I	WE#	I	Ext pull-up	I	WE#		
DRQ & Int	A3	INT#	O	INT#	O	INT#	O	INT#	O	SINT#	O	INT Request	GVDDQ VGND
	A4	DRQ#	O	DRQ#	O	DRQ#	O	DRQ#	O	N/C	O	DMA Request	
	B4	DACK#	I	DACK#	I	DACK#	I	DACK#	I	Ext pull-up	I	DMA Acknowledgement	

Table 8. Astoria CYWB0220ABS 121-ball FBGA Package Pin Assignments (continued)

		Pin Name										Pin Description	Power Domain	
	Double SDIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO Configuration	I/O	GPIO Configuration	I/O	GPIO Configuration	I/O	GPIO Configuration	I/O		
S-Port	G9	SD_D[7]	I/O	SD_D[7]	I/O	PD[7] (GPIO)	I/O	GPIF_DATA[15]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO or GPIF Data	SSVDDQ VGND	
	G10	SD_D[6]	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	GPIF_DATA[14]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO or GPIF Data		
	F9	SD_D[5]	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	GPIF_DATA[13]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO or GPIF Data		
	F10	SD_D[4]	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	GPIF_DATA[12]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO or GPIF Data		
	E9	SD_D[3]	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	GPIF_DATA[11]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO or GPIF Data		
	E10	SD_D[2]	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	GPIF_DATA[10]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO or GPIF Data		
	D9	SD_D[1]	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	GPIF_DATA[9]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO or GPIF Data		
	D10	SD_D[0]	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	GPIF_DATA[8]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO or GPIF Data		
	F8	SD_CLK	O	SD_CLK	O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	SD Clock or GPIO		
	G8	SD_CMD	I/O	SD_CMD	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	SD CMD or GPIO		
	H8	SD_POW		SD_POW		PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	SD Power or GPIO		
	H10	SD_WP	I	SD_WP	I	N/C		N/C		PC[5] (GPIO)		SD Write Protect		
	K7	SD2_D[7]	I/O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	GPIF_DATA[7]	I/O	GPIF_DATA[7]	I/O	SD2 Data or GPIO or GPIF Data	SNVDDQ VGND	
	K8	SD2_D[6]	I/O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	GPIF_DATA[6]	I/O	GPIF_DATA[6]	I/O	SD2 Data or GPIO or GPIF Data		
	J8	SD2_D[5]	I/O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	GPIF_DATA[5]	I/O	GPIF_DATA[5]	I/O	SD2 Data or GPIO or GPIF Data		
	K9	SD2_D[4]	I/O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	GPIF_DATA[4]	I/O	GPIF_DATA[4]	I/O	SD2 Data or GPIO or GPIF Data		
	J9	SD2_D[3]	I/O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	GPIF_DATA[3]	I/O	GPIF_DATA[3]	I/O	SD2 Data or GPIO or GPIF Data		
	H9	SD2_D[2]	I/O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	GPIF_DATA[2]	I/O	GPIF_DATA[2]	I/O	SD2 Data or GPIO or GPIF Data		
	K10	SD2_D[1]	I/O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	GPIF_DATA[1]	I/O	GPIF_DATA[1]	I/O	SD2 Data or GPIO or GPIF Data		
	J10	SD2_D[0]	I/O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	GPIF_DATA[0]	I/O	GPIF_DATA[0]	I/O	SD2 Data or GPIO or GPIF Data		
	K6	SD2_CLK	O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	SD2 Clock or GPIO		
	J6	SD2_CMD	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	SD2 CMD or GPIO		
	J5	SD2_POW	O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	SD2 Power or GPIO		
	K4	N/C	O	N/C	O	N/C	O	GPIF_CTL[1]	O	GPIF_CTL[1]	O	GPIF Control Signal		
	H6	N/C	O	N/C	O	N/C	O	GPIF_CTL[0]	O	GPIF_CTL[0]	O	GPIF Control Signal		
J7	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	GPIO			
J4	N/C	I	N/C	I	N/C	I	GPIF_RDY[0]	O	GPIF_RDY[0]	O	GPIF Ready Signal			
K5	SD2_WP	O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	SD Write Protect or GPIO			
Other	B10	RESETOUT	O	RESETOUT	O	RESETOUT	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT / GPIF_RDY[1]	O	Reset Out	GVDDQ VGND	
	C9	SD2_CD	I/O I	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	GPIO or SD2 CD		
	D8	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	GPIO or SD CD		
	C10	RESET#									I	RESET		
	C7	WAKEUP									I	Wake Up Signal		

Table 8. Astoria CYWB0220ABS 121-ball FBGA Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Conf	C5	XTALSLC[1]	I	Clock Select 1	GVDDQ VGND
	C4	XTALSLC[0]		Clock Select 0	
	E8	TEST[2]	I	Test Cfg 2	
	C8	TEST[1]		Test Cfg 1	
	D7	TEST[0]		Test Cfg 0	
Clock	A8	XTALIN	I	Crystal / Clock IN	XVDDQ VGND
	B8	XTALOUT	O	Crystal Out	
Power	D4 H4	PVDDQ	Power	Processor I/F VDD	
	H5	SNVDDQ	Power	GPIF VDD	
	B5	UVDDQ	Power	USB VDD	
	H7	SSVDDQ	Power	SDIO VDD	
	D6	GVDDQ	Power	Misc I/O VDD	
	B9	AVDDQ	Power	Analog VDD	
	B7	XVDDQ	Power	Crystal VDD	
	D5, G4, G5, G6, G7, F7	VDD	Power	Core VDD	
	A10	VDD33	Power	Independent 3.3 V	
	B6	UVSSQ	Power	USB GND	
	A9	AVSSQ	Power	Analog GND	
	E4, E5, E6, E7, F4, F5, F6	VGND	Power	Core GND	

Table 9. Astoria CYWB0216ABS 121-ball FBGA Package Pin Assignments

	Pin Name			Pin Description	Power Domain	
	Ball #	Pull Direction	I/O			
Unused Pins	J2	P/D	I	Pull-down	PVDDQ VGND	
	G1	P/U	I	Pull-up		
	H3	P/U	I	Pull-up		
	J3	P/U	I	Pull-up		
	J1	P/U	I	Pull-up		
	K3	P/D	I	Pull-down		
	K2	P/U	I	Pull-up		
	K1	P/U	I	Pull-up		
	G2	P/U	I	Pull-up		
	G3	P/U	I	Pull-up		
	F1	P/U	I	Pull-up		
	F2	P/U	I	Pull-up		
	F3	P/U	I	Pull-up		
	E1	P/U	I	Pull-up		
	E2	P/U	I	Pull-up		
	E3	P/U	I	Pull-up		
	D1	P/U	I	Pull-up		
	D2	P/U	I	Pull-up		
	D3	P/U	I	Pull-up		
	C1	P/U	I	Pull-up		
	C2	P/U	I	Pull-up		
	C3	P/U	I	Pull-up		
	B1	P/U	O	Pull-up		
	B2	P/U	I	Pull-up		
	A1	P/U	I	Pull-up		
	B3	P/U	I	Pull-up		
	A2	P/U	I	Pull-up		
	A3	N/C		O	No Connect	GVDDQ VGND
A4	N/C		O	No Connect		
B4	P/U		I	Pull-up		
I²C Pins	Interface Pins			I/O	Pin Description	
	H2	SDA	I/O	I ² C data	PVDDQ VGND	
H1	SCL	I/O	I ² C clock			
U-Port	A5	D+	I/O/Z	USB D+	UVDDQ UVSSQ	
	A6	D-	I/O/Z	USB D-		
	A7	SWD+	I/O/Z	USB Switch DP		
	C6	SWD-	I/O/Z	USB Switch DM		

Table 9. Astoria CYWB0216ABS 121-ball FBGA Package Pin Assignments (continued)

		Pin Name									Pin Description	Power Domain	
	Double SDIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO Configuration	I/O	GPIF Configuration	I/O	GPIF & GPIO Configuration	I/O			
S-Port	G9	SD_D[7]	I/O	SD_D[7]	I/O	PD[7] (GPIO)	I/O	GPIF_DATA[15]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO or GPIF Data	SSVDDQ VGND
	G10	SD_D[6]	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	GPIF_DATA[14]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F9	SD_D[5]	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	GPIF_DATA[13]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F10	SD_D[4]	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	GPIF_DATA[12]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E9	SD_D[3]	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	GPIF_DATA[11]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E10	SD_D[2]	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	GPIF_DATA[10]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D9	SD_D[1]	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	GPIF_DATA[9]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	D10	SD_D[0]	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	GPIF_DATA[8]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F8	SD_CLK	O	SD_CLK	O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	PC[7] (GPIO)	I/O	SD Clock or GPIO	
	G8	SD_CMD	I/O	SD_CMD	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	PC[3] (GPIO)	I/O	SD CMD or GPIO	
	H8	SD_POW		SD_POW		PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	PC[6] (GPIO)	I/O	SD Power or GPIO	
	H10	SD_WP	I	SD_WP	I	N/C		N/C		PC[5] (GPIO)		SD Write Protect	
	K7	SD2_D[7]	I/O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	GPIF_DATA[7]	I/O	GPIF_DATA[7]	I/O	SD2 Data or GPIO or GPIF Data	SNVDDQ VGND
	K8	SD2_D[6]	I/O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	GPIF_DATA[6]	I/O	GPIF_DATA[6]	I/O	SD2 Data or GPIO or GPIF Data	
	J8	SD2_D[5]	I/O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	GPIF_DATA[5]	I/O	GPIF_DATA[5]	I/O	SD2 Data or GPIO or GPIF Data	
	K9	SD2_D[4]	I/O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	GPIF_DATA[4]	I/O	GPIF_DATA[4]	I/O	SD2 Data or GPIO or GPIF Data	
	J9	SD2_D[3]	I/O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	GPIF_DATA[3]	I/O	GPIF_DATA[3]	I/O	SD2 Data or GPIO or GPIF Data	
	H9	SD2_D[2]	I/O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	GPIF_DATA[2]	I/O	GPIF_DATA[2]	I/O	SD2 Data or GPIO or GPIF Data	
	K10	SD2_D[1]	I/O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	GPIF_DATA[1]	I/O	GPIF_DATA[1]	I/O	SD2 Data or GPIO or GPIF Data	
	J10	SD2_D[0]	I/O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	GPIF_DATA[0]	I/O	GPIF_DATA[0]	I/O	SD2 Data or GPIO or GPIF Data	
	K6	SD2_CLK	O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	SD2 Clock or GPIO	
	J6	SD2_CMD	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	SD2 CMD or GPIO	
	J5	SD2_POW	O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	SD2 Power or GPIO	
	K4	N/C	O	N/C	O	N/C	O	GPIF_CTL[1]	O	GPIF_CTL[1]	O	GPIF Control Signal	
	H6	N/C	O	N/C	O	N/C	O	GPIF_CTL[0]	O	GPIF_CTL[0]	O	GPIF Control Signal	
J7	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	PA[5] (GPIO)	I/O	GPIO		
J4	N/C	I	N/C	I	N/C	I	GPIF_RDY[0]	O	GPIF_RDY[0]	O	GPIF Ready Signal		
K5	SD2_WP	O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	PC[2] (GPIO)	I/O	SD Write Protect or GPIO		
Other	B10	RESETOUT	O	RESETOUT	O	RESETOUT	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT / GPIF_RDY[1]	O	Reset Out	GVDDQ VGND
	C9	SD2_CD	I/O I	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	GPIO or SD2 CD	
	D8	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0]) or SD_CD	I/O I	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	GPIO or SD CD	
	C10	RESET#									I	RESET	
	C7	WAKEUP									I	Wake Up Signal	

Table 9. Astoria CYWB0216ABS 121-ball FBGA Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Conf	C5	XTALSLC[1]	I	Clock Select 1	GVDDQ VGND
	C4	XTALSLC[0]		Clock Select 0	
	E8	TEST[2]	I	Test Cfg 2	
	C8	TEST[1]		Test Cfg 1	
	D7	TEST[0]		Test Cfg 0	
Clock	A8	XTALIN	I	Crystal/Clock IN	XVDDQ VGND
	B8	XTALOUT	O	Crystal Out	
Power	D4 H4	PVDDQ	Power	Processor I/F VDD	
	H5	SNVDDQ	Power	NAND VDD	
	B5	UVDDQ	Power	USB VDD	
	H7	SSVDDQ	Power	SDIO VDD	
	D6	GVDDQ	Power	Misc I/O VDD	
	B9	AVDDQ	Power	Analog VDD	
	B7	XVDDQ	Power	Crystal VDD	
	D5, G4, G5, G6, G7, F7	VDD	Power	Core VDD	
	A10	VDD33	Power	Independent 3.3 V	
	B6	UVSSQ	Power	USB GND	
	A9	AVSSQ	Power	Analog GND	
	E4, E5, E6, E7, F4, F5, F6	VGND	Power	Core GND	

Table 10. Astoria 81-ball SP WLCSP Package Pin Assignments

		Pin Name				Pin Description	Power Domain
	Ball #	PNAND	I/O	SPI	I/O		
P-Port	H9	Ext pull low	I	SCK	I	Clock	PVDDQ VGND
	F9	CE#	I	SS#	I	CE# or SPI Slave Select	
	E7	SDA	I/O	SDA	I/O	I2C data	
	H8	SCL	I/O	SCL	I/O	I2C clock	
	J9	WP#	I	Ext pull up	I	PNAND WP	
	G8	A[3]=0; (Ext pull low)	I	A[3]=0; (Ext pull up)	I	A[3]	
	E6	A[2]=0; (Ext pull low)	I	A[2]=0; (Ext pull low)	I	A[2]	
	G9	RB#	O	Ext pull up	I	PNAND R/B#	
	F8	CLE	I	Ext pull up	I	PNAND CLE	
	D9	I/O[7]	I/O	Ext pull up	I	IO7	
	D8	I/O[6]	I/O	Ext pull up	I	IO6	
	C9	I/O[5]	I/O	Ext pull up	I	IO5	
	B9	I/O[4]	I/O	Ext pull up	I	IO4	
	C8	I/O[3]	I/O	Ext pull up	I	IO3	
	C7	I/O[2]	I/O	Ext pull up	I	IO2	
	B8	I/O[1]	I/O	SDO	O	IO1 or SPI SDO	
	A8	I/O[0]	I/O	SDI	I	IO0 or SPI SDI	
	B7	ALE	I	Ext pull up	I	Address Valid	
	B6	RE#	I	Ext pull up	I	Output Enable	
A7	WE#	I	Ext pull up	I	WE#		
Int	C1	INT#	O	SINT#	O	INT Request	GVDDQ VGND
U-Port	A4	D+			I/O/Z	USB D+	UVDDQ UVSSQ
	A5	D-			I/O/Z	USB D-	
	C4	SWD+			I/O/Z	USB Switch D+	
	C5	SWD-			I/O/Z	USB Switch D-	

Table 10. Astoria 81-ball SP WLCSP Package Pin Assignments (continued)

		Pin Name										Pin Description	Power Domain
Ball #	Double SDIO Configuration	I/O	SDIO & GPIO Configuration	I/O	GPIO Configuration	I/O	GPIF Configuration	I/O	GPIF & GPIO Configuration	I/O			
S-Port	H2	SD_D[7]	I/O	SD_D[7]	I/O	PD[7] (GPIO)	I/O	GPIF_DATA [15]	I/O	PD[7] (GPIO)	I/O	SD Data or GPIO or GPIF Data	SSVDDQ VGND
	H1	SD_D[6]	I/O	SD_D[6]	I/O	PD[6] (GPIO)	I/O	GPIF_DATA [14]	I/O	PD[6] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	G3	SD_D[5]	I/O	SD_D[5]	I/O	PD[5] (GPIO)	I/O	GPIF_DATA [13]	I/O	PD[5] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	G2	SD_D[4]	I/O	SD_D[4]	I/O	PD[4] (GPIO)	I/O	GPIF_DATA [12]	I/O	PD[4] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F2	SD_D[3]	I/O	SD_D[3]	I/O	PD[3] (GPIO)	I/O	GPIF_DATA [11]	I/O	PD[3] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	F3	SD_D[2]	I/O	SD_D[2]	I/O	PD[2] (GPIO)	I/O	GPIF_DATA [10]	I/O	PD[2] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E3	SD_D[1]	I/O	SD_D[1]	I/O	PD[1] (GPIO)	I/O	GPIF_DATA [9]	I/O	PD[1] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	E2	SD_D[0]	I/O	SD_D[0]	I/O	PD[0] (GPIO)	I/O	GPIF_DATA [8]	I/O	PD[0] (GPIO)	I/O	SD Data or GPIO or GPIF Data	
	G1	SD_CLK	O	SD_CLK		PC-7 (GPIO)	I/O	PC-7 (GPIO)	I/O	PC-7 (GPIO)	I/O	SD Clock or GPIO	
	F4	SD_CMD	I/O	SD_CMD	I/O	PC-3 (GPIO)	I/O	PC-3 (GPIO)	I/O	PC-3 (GPIO)	I/O	SD CMD or GPIO	
	J1	SD_POW	O	SD_POW	O	PC-6 (GPIO)	I/O	PC-6 (GPIO)	I/O	PC-6 (GPIO)	I/O	SD Power or GPIO	
	E1	SD_WP	I	SD_W	I	N/C	I	N/C	I	PC-5 (GPIO)	I/O	SD Write Protect	
	H5	SD2_D[7]	I/O	PB[7] (GPIO)	I/O	PB[7] (GPIO)	I/O	GPIF_DATA [7]	I/O	GPIF_DATA [7]	I/O	SD2 Data or GPIO or GPIF Data	SNVDDQ VGND
	J4	SD2_D[6]	I/O	PB[6] (GPIO)	I/O	PB[6] (GPIO)	I/O	GPIF_DATA [6]	I/O	GPIF_DATA [6]	I/O	SD2 Data or GPIO or GPIF Data	
	G5	SD2_D[5]	I/O	PB[5] (GPIO)	I/O	PB[5] (GPIO)	I/O	GPIF_DATA [5]	I/O	GPIF_DATA [5]	I/O	SD2 Data or GPIO or GPIF Data	
	H4	SD2_D[4]	I/O	PB[4] (GPIO)	I/O	PB[4] (GPIO)	I/O	GPIF_DATA [4]	I/O	GPIF_DATA [4]	I/O	SD2 Data or GPIO or GPIF Data	
	J3	SD2_D[3]	I/O	PB[3] (GPIO)	I/O	PB[3] (GPIO)	I/O	GPIF_DATA [3]	I/O	GPIF_DATA [3]	I/O	SD2 Data or GPIO or GPIF Data	
	G4	SD2_D[2]	I/O	PB[2] (GPIO)	I/O	PB[2] (GPIO)	I/O	GPIF_DATA [2]	I/O	GPIF_DATA [2]	I/O	SD2 Data or GPIO or GPIF Data	
	H3	SD2_D[1]	I/O	PB[1] (GPIO)	I/O	PB[1] (GPIO)	I/O	GPIF_DATA [1]	I/O	GPIF_DATA [1]	I/O	SD2 Data or GPIO or GPIF Data	
	J2	SD2_D[0]	I/O	PB[0] (GPIO)	I/O	PB[0] (GPIO)	I/O	GPIF_DATA [0]	I/O	GPIF_DATA [0]	I/O	SD2 Data or GPIO or GPIF Data	
	F7	SD2_CLK	O	PA[6] (GPIO)	I/O	PA[6] (GPIO)	I/O	PA-6 (GPIO)	I/O	PA-6 (GPIO)	I/O	SD2 Clock or GPIO	
	H6	SD2_CMD	I/O	PA[7] (GPIO)	I/O	PA[7] (GPIO)	I/O	PA-7 (GPIO)	I/O	PA-7 (GPIO)	I/O	SD2 CMD or GPIO	
	G7	SD2_POW	O	PC[0] (GPIO)	I/O	PC[0] (GPIO)	I/O	PC-0 (GPIO)	I/O	PC-0 (GPIO)	I/O	SD2 Power or GPIO	
	J8	N/C	O	N/C	O	N/C	O	GPIF_CTL[1]	O	GPIF_CTL[1]	O	GPIF Control Signal	
J5	N/C	O	N/C	O	N/C	O	GPIF_CTL[0]	O	GPIF_CTL[0]	O	GPIF Control Signal		
G6	PA-5 (GPIO)	I/O	PA-5 (GPIO)	I/O	PA-5 (GPIO)	I/O	PA-5 (GPIO)	I/O	PA-5 (GPIO)	I/O	GPIO		
H7	N/C	I	N/C	I	N/C	I	GPIF_RDY[0]	O	GPIF_RDY[0]	O	GPIF Ready Signal		
J7	SD2_WP	O	PC-2 (GPIO)	I/O	PC-2 (GPIO)	I/O	PC-2 (GPIO)	I/O	PC-2 (GPIO)	I/O	SD Write Protect or GPIO		
Other	C2	RESETOUT	O	RESETOUT	O	RESETOUT	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT / GPIF_RDY[1]	O	RESETOUT or GPIF	GVDDQ VGND
	D2	PC-5 (GPIO[1]) or SD2_CD	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	PC-5 (GPIO[1])	I/O	GPIO or SD2 CD	
	D1	PC-4 (GPIO[0]) or SD_CD	I/O	PC-4 (GPIO[0]) or SD_CD	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	PC-4 (GPIO[0])	I/O	GPIO or SD CD	
	C3	RESET#									I	RESET	
	D4	WAKEUP									I	Wake Up Signal	

Table 10. Astoria 81-ball SP WLCSP Package Pin Assignments (continued)

	Pin Name			Pin Description	Power Domain
Conf	A1	XTALSLC	I	Clock Select	GVDDQ VGND
	B1	TEST[2]	I	Test Cfg 2	
	C6	TEST[1]	I	Test Cfg 1	
	B4	TEST[0]	I	Test Cfg 0	
CLK	A2	XTALIN	I	Crystal / Clock IN	XVDDQ VGND
Power	A9, E8	PVDDQ	Power	Processor I/F VDD	
	J6	SNVDDQ	Power	GPIO VDD	
	B5	UVDDQ	Power	USB VDD	
	F1	SSVDDQ	Power	SDIO VDD	
	D3	GVDDQ	Power	Misc I/O VDD	
	B3	AVDDQ	Power	Analog VDD	
	A6, D6, E5, F6	VDD	Power	Core VDD	
	A3	UVSSQ	Power	USB GND	
	B2	AVSSQ	Power	Analog GND	
	D5, D7, E4, E9, F5	VGND	Power	Core GND	

Table 11. Astoria 81-ball Lite SP WLCSP Package Pin Assignments

	Pin Name						Pin Description	Power Domain	
	Ball #	SRAM Interface		ADM (Address/Data Multi-plexing)	I/O	PNAND			I/O
P-Port	G9	CE#	I	CE#	I	CE#	I	CE#	PVDDQ VGND
	H5	A7	I	External Pull Up	I	A7 ≥ 1: SBD A7 ≥ 0: LBD	I	A7	
	J8	A6	I	SDA	I/O	SDA	I/O	A7 or SDA	
	H6	A5	I	SCL	I/O	SCL	I/O	A6 or SCL	
	H7	A4	I	External Pull Up	I	WP#	I	A4 or WP#	
	J9	A3	I	External Pull Low	I	External Pull Low	I	A3	
	H8	A2	I	External Pull Up	I	External Pull Low	I	A2	
	H9	A1	I	External Pull Up	I	R/B#	I	A1 or R/B#	
	G8	A0	I	External Pull Up	I	CLE	I	A0 or CLE	
	G6	DQ[15]	I/O	AD[15]	I/O	I/O[15]	I/O	D15, AD15, or IO15	
	F9	DQ[14]	I/O	AD[14]	I/O	I/O[14]	I/O	D14, AD14, or IO14	
	F8	DQ[13]	I/O	AD[13]	I/O	I/O[13]	I/O	D13, AD13, or IO13	
	F7	DQ[12]	I/O	AD[12]	I/O	I/O[12]	I/O	D12, AD12, or IO12	
	E9	DQ[11]	I/O	AD[11]	I/O	I/O[11]	I/O	D11, AD11, or IO11	
	E8	DQ[10]	I/O	AD[10]	I/O	I/O[10]	I/O	D10, AD10, or IO10	
	D9	DQ[9]	I/O	AD[9]	I/O	I/O[9]	I/O	D9, AD9, or IO9	
	D7	DQ[8]	I/O	AD[8]	I/O	I/O[8]	I/O	D8, AD8, or IO8	
	D8	DQ[7]	I/O	AD[7]	I/O	I/O[7]	I/O	D7, AD7, or IO7	
	C9	DQ[6]	I/O	AD[6]	I/O	I/O[6]	I/O	D6, AD6, or IO6	
	D6	DQ[5]	I/O	AD[5]	I/O	I/O[5]	I/O	D5, AD5, or IO5	
	B9	DQ[4]	I/O	AD[4]	I/O	I/O[4]	I/O	D4, AD4, or IO4	
	C8	DQ[3]	I/O	AD[3]	I/O	I/O[3]	I/O	D3, AD3, or IO3	
	C7	DQ[2]	I/O	AD[2]	I/O	I/O[2]	I/O	D2, AD2, or IO2	
	B8	DQ[1]	I/O	AD[1]	I/O	I/O[1]	I/O	D1, AD1, or IO1	
	A8	DQ[0]	I/O	AD[0]	I/O	I/O[0]	I/O	D01, AD0, or IO0	
	B7		I	ADV#	I	ALE	I	Address Valid	
B6	OE#	I	OE#	I	RE#	I	Output Enable		
A7	WE#	I	WE#	I	WE#	I	WE#		
Int	C1	INT#	O	INT#	O	INT#	O	INT Request	GVDDQ VGND
	D4	DRQ#	O	DRQ#	O	DRQ#	O	DMA Request	
	D3	DACK#	I	DACK#	I	DACK#	I	DMA ACK	
U-Port	A4	D+					I/O/Z	USB D+	UVDDQ UVSSQ
	A5	D-					I/O/Z	USB D-	
	C4	SWD+					I/O/Z	USB Switch DP	
	C5	SWD-					I/O/Z	USB Switch DM	

Table 11. Astoria 81-ball Lite SP WLCSP Package Pin Assignments (continued)

		S-Port Interface		I/O		
S-Port	F3	SD_D[7]		I/O	SD Data or GPIO	SSVDDQ VGND
	H1	SD_D[6]		I/O	SD Data or GPIO	
	G2	SD_D[5]		I/O	SD Data or PIO	
	E3	SD_D[4]		I/O	SD Data or GPIO	
	F2	SD_D[3]		I/O	SD Data or GPIO	
	F1	SD_D[2]		I/O	SD Data or GPIO	
	E2	SD_D[1]		I/O	SD Data or GPIO	
	E1	SD_D[0]		I/O	SD Data or GPIO	
	G1	SD_CLK		I/O	SD Clock or GPIO	
	J1	SD_CMD		I/O	SD CMD or GPIO	
	J5	PB[7] (GPIO)		I/O	GPIOI	
	J4	PB[6] (GPIO)		I/O	GPIOI	
	H4	PB[5] (GPIO)		I/O	GPIOI	
	J3	PB[4] (GPIO)		I/O	GPIOI	
	H3	PB[3] (GPIO)		I/O	GPIOI	
	G4	PB[2] (GPIO)		I/O	GPIOI	
	J2	PB[1] (GPIO)		I/O	GPIOI	
H2	PB[0] (GPIO)		I/O	GPIOI		
J7	GPIF_RDY		O	Test Mode		
J6	GPIF_CTL		I	Test Mode (Ext Pull-High)		
Other	D1	SD_CD		I	SD CD	GVDDQ VGND
	C2	RESET#		I	RESET	
	E5	WAKEUP		I	Wake Up Signal	
Conf	C3	TEST[2]		I	Test Cfg 2	GVDDQ VGND
	D5	TEST[1]		I	Test Cfg 1	
	B1	TEST[0]		I	Test Cfg 0	
CLK	A2	XTALIN		I	Clock IN	XVDDQ VGND
	A1	XTALOUT		O	Clock OUT	
Power	A9, F6	PVDDQ		Power	Processor I/F VDD	
	B5	UVDDQ		Power	USBVDD	
	E4	SSVDDQ		Power	SDIO VDD	
	D2	GVDDQ		Power	Misc I/O VDD	
	B3	AVDDQ		Power	Analog VDD	
	B4	XVDDQ		Power	Crystal VDD	
	E7, A6, C6, F5	VDD		Power	Core VDD	
	A3	UVSSQ		Power	USB GND	
	B2	AVSSQ		Power	Analog GND	
	G7, E6, G5, F4, G3	VGND		Power	Core GND	

Figure 9. Astoria 100-ball VFBGA Ball Map - Top View

	1	2	3	4	5	6	7	8	9	10	
A	ADV#	WE#	INT#	DRQ#	D+	D-	SWD+	XTALIN	AVSSQ	VDD33	A
B	DQ[1]	DQ[0]	OE#	DACK#	UVDDQ	UVSSQ	XVDDQ	XTALOUT	AVDDQ	RESETOUT	B
C	DQ[4]	DQ[3]	DQ[2]	XTALSCLC[0]	XTALSCLC[1]	SWD-	WAKEUP	TEST[1]	GPIO[1]	RESET#	C
D	DQ[7]	DQ[6]	DQ[5]	PVDDQ	VDD	GVDDQ	TEST[0]	GPIO[0]	SD_D[1]	SD_D[0]	D
E	DQ[10]	DQ[9]	DQ[8]	VGND	VGND	VGND	VGND	TEST[2]	SD_D[3]	SD_D[2]	E
F	DQ[13]	DQ[12]	DQ[11]	VGND	VGND	VGND	VDD	SD_CLK	SD_D[5]	SD_D[4]	F
G	CE#	DQ[15]	DQ[14]	VDD	VDD	VDD	VDD	SD_CMD	SD_D[7]	SD_D[6]	G
H	A[5]	A[6]	A[7]	PVDDQ	SNVDDQ	GPIF_CTL[0]	SSVDDQ	SD_POW	GPIF_DATA[2]	SD_WP	H
J	A[3]	CLK	A[4]	GPIF_RDY[0]	PC[0]	PA[7]	PA[5]	GPIF_DATA[5]	GPIF_DATA[3]	GPIF_DATA[0]	J
K	A[0]	A[1]	A[2]	GPIF_CTL[1]	PC[2]	PA[6]	GPIF_DATA[7]	GPIF_DATA[6]	GPIF_DATA[4]	GPIF_DATA[1]	K
	1	2	3	4	5	6	7	8	9	10	











POWER DOMAIN KEY	
	UVDDQ
	UVSSQ
	GVDDQ
	SSVDDQ
	VDDQ/AVDDQ
	VGND/AVSSQ
	PVDDQ
	SNVDDQ
	XVDDQ
	VDD33

Figure 10. Ball map_CYWB0216 - Top View

Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	P/U	P/U	N/C	N/C	D+	D-	SWD+	XTALIN	AVSSQ	VDD33	N/C	A
B	P/U	P/U	P/U	P/U	UVDDQ	UVSSQ	XVDDQ	XTALOUT	AVDDQ	RESETOUT	N/C	B
C	P/U	P/U	P/U	XTALSQC[0]	XTALSQC[1]	SWD-	WAKEUP	TEST[1]	GPIO[1]	RESET#	N/C	C
D	P/U	P/U	P/U	PVDDQ	VDD	GVDDQ	TEST[0]	GPIO[0]	SD_D[1]	SD_D[0]	N/C	D
E	P/U	P/U	P/U	VGND	VGND	VGND	VGND	TEST[2]	SD_D[3]	SD_D[2]	N/C	E
F	P/U	P/U	P/U	VGND	VGND	VGND	VDD	SD_CLK	SD_D[5]	SD_D[4]	N/C	F
G	P/U	P/U	P/U	VDD	VDD	VDD	VDD	SD_CMD	SD_D[7]	SD_D[6]	N/C	G
H	SCL	SDA	P/U	PVDDQ	SNVDDQ	GPIF_CTL [0]	SSVDDQ	SD_POW	GPIF_DATA[2]	SD_WP	N/C	H
J	P/U	P/D	P/U	GPIF_RDY [0]	PC [0]	PA [7]	PA [5]	GPIF_DATA[5]	GPIF_DATA[3]	GPIF_DATA[0]	N/C	J
K	P/U	P/U	P/D	GPIF_CTL [1]	PC [2]	PA [6]	GPIF_DATA[7]	GPIF_DATA[6]	GPIF_DATA[4]	GPIF_DATA[1]	N/C	K
L	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	L
	1	2	3	4	5	6	7	8	9	10	11	














POWER DOMAIN KEY	
	UVDDQ
	UVSSQ
	GVDDQ
	SSVDDQ
	VDDQ/AVDDQ
	VGND/AVSSQ
	PVDDQ
	SNVDDQ
	XVDDQ
	VDD33
	P/U
	P/D
	N/C

Figure 11. Ball map_CYWB0220 - Top View

Top View

	1	2	3	4	5	6	7	8	9	10	11	
A	ADV#	WE#	INT#	DRQ#	N/C	N/C	N/C	XTALIN	AVSSQ	VDD33	N/C	A
B	DQ[1]	DQ[0]	OE#	DACK#	UVDDQ	UVSSQ	XVDDQ	XTALOUT	AVDDQ	RESETOUT	N/C	B
C	DQ[4]	DQ[3]	DQ[2]	XTALSCLC[0]	XTALSCLC[1]	N/C	WAKEUP	TEST[1]	GPIO[1]	RESET#	N/C	C
D	DQ[7]	DQ[6]	DQ[5]	PVDDQ	VDD	GVDDQ	TEST[0]	GPIO[0]	SD_D[1]	SD_D[0]	N/C	D
E	DQ[10]	DQ[9]	DQ[8]	VGND	VGND	VGND	VGND	TEST[2]	SD_D[3]	SD_D[2]	N/C	E
F	DQ[13]	DQ[12]	DQ[11]	VGND	VGND	VGND	VDD	SD_CLK	SD_D[5]	SD_D[4]	N/C	F
G	CE#	DQ[15]	DQ[14]	VDD	VDD	VDD	VDD	SD_CMD	SD_D[7]	SD_D[6]	N/C	G
H	A[5]	A[6]	A[7]	PVDDQ	SNVDDQ	GPIF_CTL[0]	SSVDDQ	SD_POW	GPIF_DATA[2]	SD_WP	N/C	H
J	A[3]	CLK	A[4]	GPIF_RDY[0]	PC [0]	PA [7]	PA[5]	GPIF_DATA[5]	GPIF_DATA[3]	GPIF_DATA[0]	N/C	J
K	A[0]	A[1]	A[2]	GPIF_CTL[1]	PC [2]	PA [6]	GPIF_DATA[7]	GPIF_DATA[6]	GPIF_DATA[4]	GPIF_DATA[1]	N/C	K
L	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	L
	1	2	3	4	5	6	7	8	9	10	11	

POWER DOMAIN KEY	
	UVDDQ
	UVSSQ
	GVDDQ
	SSVDDQ
	VDDQ/AVDDQ
	VGND/AVSSQ
	PVDDQ
	SNVDDQ
	XVDDQ
	VDD33
	N/C

Figure 12. Ball map_CYWB0224 - Top View

Top View											
	1	2	3	4	5	6	7	8	9	10	11
A	ADV#	WE#	INT#	DRQ#	D+	D-	SWD+	XTALIN	AVSSQ	VDD33	N/C
B	DQ[1]	DQ[0]	OE#	DACK#	UVDDQ	UVSSQ	XVDDQ	XTALOUT	AVDDQ	RESETOUT	N/C
C	DQ[4]	DQ[3]	DQ[2]	XTALSQC[0]	XTALSQC[1]	SWD-	WAKEUP	TEST[1]	GPI0[1]	RESET#	N/C
D	DQ[7]	DQ[6]	DQ[5]	PVDDQ	VDD	GVDDQ	TEST[0]	GPI0[0]	SD_D[1]	SD_D[0]	N/C
E	DQ[10]	DQ[9]	DQ[8]	VGND	VGND	VGND	VGND	TEST[2]	SD_D[3]	SD_D[2]	N/C
F	DQ[13]	DQ[12]	DQ[11]	VGND	VGND	VGND	VDD	SD_CLK	SD_D[5]	SD_D[4]	N/C
G	CE#	DQ[15]	DQ[14]	VDD	VDD	VDD	VDD	SD_CMD	SD_D[7]	SD_D[6]	N/C
H	A[5]	A[6]	A[7]	PVDDQ	SNVDDQ	GPIF_CTL[0]	SSVDDQ	SD_POW	GPIF_DATA[2]	SD_WP	N/C
J	A[3]	CLK	A[4]	GPIF_RDY[0]	PC[0]	PA[7]	PA[5]	GPIF_DATA[5]	GPIF_DATA[3]	GPIF_DATA[0]	N/C
K	A[0]	A[1]	A[2]	GPIF_CTL[1]	PC[2]	PA[6]	GPIF_DATA[7]	GPIF_DATA[6]	GPIF_DATA[4]	GPIF_DATA[1]	N/C
L	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C	N/C

POWER DOMAIN KEY	
UVDDQ	UVSSQ
GVDDQ	SSVDDQ
VDDQ/AVDDQ	VGND/AVSSQ
PVDDQ	SNVDDQ
XVDDQ	VDD33
N/C	

Figure 13. Astoria 81-ball SP WLCSP Ball Map - Top View

	1	2	3	4	5	6	7	8	9	
A	XTALSLC	XTALIN	UVSSQ	D+	D-	VDD	WE#	IO[0]	PVDDQ	A
B	TEST[2]	AVSSQ	AVDDQ	TEST[0]	UVDDQ	RE#	ALE	IO[1]	IO[4]	B
C	INT#	RESETOUT	RESET#	SWD+	SWD-	TEST[1]	IO[2]	IO[3]	IO[5]	C
D	GPIO[0]	GPIO[1]	GVDDQ	WAKEUP	VGND	VDD	VGND	IO[6]	IO[7]	D
E	SD_WP	SD_D[0]	SD_D[1]	VGND	VDD	A[2]	SDA	PVDDQ	VGND	E
F	SSVDDQ	SD_D[3]	SD_D[2]	SD_CMD	VGND	VDD	PA[6]	CLE	CE#	F
G	SD_CLK	SD_D[4]	SD_D[5]	GPIF_DATA[2]	GPIF_DATA[5]	PA[5]	PC[0]	A[3]	R/B#	G
H	SD_D[6]	SD_D[7]	GPIF_DATA[1]	GPIF_DATA[4]	GPIF_DATA[7]	PA[7]	GPIF_RDY[0]	SCL	Pull-Low	H
J	POW	GPIF_DATA[0]	GPIF_DATA[3]	GPIF_DATA[6]	GPIF_CTL [0]	SNVDDQ	PC [2]	GPIF_CTL [1]	WP#	J
	1	2	3	4	5	6	7	8	9	


















POWER DOMAIN KEY	
	UVDDQ
	UVSSQ
	GVDDQ
	SSVDDQ
	VDDQ/AVDDQ
	VGND/AVSSQ
	PVDDQ
	SNVDDQ
	XVDDQ

Figure 14. Astoria 81-ball Lite SP WLCSP Ball Map - Top View

	1	2	3	4	5	6	7	8	9	
A	XTALOUT	XTALIN	UVSSQ	D+	D-	VDD	WE#	DQ[0]	PVDDQ	A
B	TEST[0]	AVSSQ	AVDDQ	XVDDQ	UVDDQ	OE#	ADV#	DQ[1]	DQ[4]	B
C	INT#	RESET#	TEST[2]	SWD+	SWD-	VDD	DQ[2]	DQ[3]	DQ[6]	C
D	GPIO[0]	GVDDQ	DACK#	DRQ#	TEST[1]	DQ[5]	DQ[8]	DQ[7]	DQ[9]	D
E	SD_D[0]	SD_D[1]	SD_D[4]	SSVDDQ	WAKEUP	VGND	VDD	DQ[10]	DQ[11]	E
F	SD_D[2]	SD_D[3]	SD_D[7]	VGND	VDD	PVDDQ	DQ[12]	DQ[13]	DQ[14]	F
G	SD_CLK	SD_D[5]	VGND	PB[2] (GPIO)	VGND	DQ[15]	VGND	A[0]	CE#	G
H	SD_D[6]	PB[0] (GPIO)	PB[3] (GPIO)	PB[5] (GPIO)	A[7]	A[5]	A[4]	A[2]	A[1]	H
J	SD_CMD	PB[1] (GPIO)	PB[4] (GPIO)	PB[6] (GPIO)	PB[7] (GPIO)	GPIF_RDY	GPIF_CTL	A[6]	A[3]	J
	1	2	3	4	5	6	7	8	9	

POWER DOMAIN KEY	
	UVDDQ
	UVSSQ
	GVDDQ
	SSVDDQ
	VDD/AVDDQ
	VGND/AVSSQ
	PVDDQ
	XVDDQ

Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power supplied (Industrial)	-40 °C to +85 °C
Supply voltage to ground potential VDD, AVDDQ	-0.5 V to +2.0 V
GVDDQ, PVDDQ, SSVDDQ, SNVDDQ, UVDDQ, and VDD33 and XVDDQ	-0.5 V to +4.0 V
DC input voltage to any input pin (Depends on I/O supply voltage. Inputs are not overvoltage tolerant.)	1.89 V to 3.6 V
DC voltage applied to outputs in High Z state	-0.5 V to VDDQ + 0.5 V
Static discharge voltage (ESD) from JESD22-A114	> 2000 V
Latch up current	> 200 mA
Maximum output short circuit current for all I/O configurations. (Vout = 0 V) [1]	-100 mA

Operating Conditions

T _A (ambient temperature under bias)	
Industrial	-40 °C to +85 °C
VDD, AVDDQ supply voltage	1.7 V to 1.9 V
UVDDQ supply voltage	3.0 V to 3.6 V
PVDDQ, GVDDQ, SNVDDQ, SSVDDQ supply voltage	1.7 V to 3.6 V
XVDDQ (Crystal I/O) supply voltage	3.0 V to 3.6 V
XVDDQ (Ext. Clock I/O) supply voltage	1.7 V to 1.9 V

Note

1. Do not test more than one output at a time. Duration of the short circuit must not exceed one second. Tested initially and after any design or process changes that may affect these parameters

DC Characteristics

Table 12. DC Specifications for All Voltage Supplies (Except USB Switch)

Parameter	Description	Conditions	Min	Typ	Max	Unit	
V _{DD}	Core voltage supply		1.7	1.8	1.9	V	
AVDDQ	Analog voltage supply		1.7	1.8	1.9	V	
XVDDQ	Crystal voltage supply		3.0	3.3	3.6	V	
XVDDQ	Clock voltage supply		1.7	1.8	1.9	V	
PVDDQ ^[4]	Processor interface I/O		1.7	1.8, 2.5, 3.3	3.6	V	
GVDDQ ^[4]	Miscellaneous I/O voltage supply		1.7	1.8, 2.5, 3.3	3.6	V	
SNVDDQ ^[3, 4]	S-Port GPIF voltage supply		1.7	1.8, 2.5, 3.3	3.6	V	
SSVDDQ ^[3, 4]	S-Port SD I/O voltage supply		1.7	1.8, 2.5, 3.3	3.6	V	
UVDDQ ^[6]	USB voltage supply		3.0	3.3	3.6	V	
VDD33	Power sequence control supply		3.0	3.3	3.6	V	
V _{IH1} ^[5]	Input HIGH voltage 1	All ports except USB, 2.0 V ≤ V _{CC} ≤ 3.6 V	0.625 × V _{CC}	–	V _{CC} + 0.3	V	
V _{IH2} ^[5]	Input HIGH voltage 2	All ports except USB, 1.7 V ≤ V _{CC} < 2.0 V	V _{CC} – 0.4	–	V _{CC} + 0.3		
V _{IL}	Input LOW voltage		–0.3	–	0.25 × V _{CC}	V	
V _{OH}	Output HIGH voltage	I _{OH} (MAX) = –0.1 mA	0.9 × V _{CC}	–		V	
V _{OL}	Output LOW voltage	I _{OL} (MIN) = 0.1 mA		–	0.1 × V _{CC}	V	
I _{IX}	Input leakage current	All I/O signals held at VDDQ	–1	–	1	μA	
I _{OZ}	Output leakage current	All I/O signals held at VDDQ	–1	–	1	μA	
I _{CC} Core	Operating current of core voltage supply (V _{DD}) and analog voltage supply (AVDDQ)	VFBGA package outputs tri-stated	–	–	110	mA	
		WLCSP package outputs tri-stated	–	–	115	mA	
I _{CC} Crystal	Operating current of crystal voltage supply (XVDDQ) ^[8]	VFBGA package XTALOUT floating	–	–	5	mA	
		WLCSP package	–	–	N/A		
I _{CC} USB	Operating current of USB voltage supply (UVDDQ) ^[8]	Operating and terminated for high speed mode	–	–	25	mA	
I _{SB1} (For 100-ball VFBGA and 81-ball SP WLCSP-Packages)	Total standby current of Astoria when device is in suspend mode	1. *VDDQ = 3.3 V nominal (3.0–3.6 V) 2. Outputs and Bidirs high or floating ^[7] 3. XTALOUT floating 4. D+ floating, D–grounded 5. Device in suspend mode	25 °C	–	300 ^[2]	–	μA
			85 °C	–	–	3000	μA

Notes

- I_{SB1} typical value is not a maximum specification but a typical value. I_{SB1} maximum current value specified for 85°C.
- The SSVDDQ I/O voltage can be dynamically changed (for example, from high range to low range) as long as the supply voltage undershoot does not surpass the lower minimum voltage limit. SSVDDQ and SNVDDQ levels for SD modes: 2.0 V–3.6 V, MMC modes: 1.7 V–3.6 V.
- Interfaces with a voltage range are adjustable with respect to the I/O voltage and supports multiple I/O voltages.
- V_{CC} = pertinent VDDQ value.
- When U-Port is in a disabled state, UVDDQ can go down to 2.4 V, provided UVDDQ is still the highest supply voltage level.
- The Outputs and Bidirs that are forced low in standby mode can increase I/O supply standby current beyond specified value.
- Active Current Conditions:
 -UVDDQ: USB transmitting 50% of the time, receiving 50% of the time.
 -PVDDQ/SNVDDQ/SSVDDQ/GVDDQ: Active current depends on I/O activity, bus load and supply level.
 -XVDDQ: Assume highest frequency clock (48 MHz) or crystal (26 MHz).

Table 12. DC Specifications for All Voltage Supplies (Except USB Switch) (continued)

Parameter	Description	Conditions	Min	Typ	Max	Unit	
I _{SB1} (For 81-ball Lite SP WLCSP)	Total standby current of Astoria when device is in suspend mode	6. *VDDQ = 3.3 V nominal (3.0–3.6 V) 7. Outputs and Bidirs high or floating ^[7] 8. XTALOUT floating 9. D+ floating, D– grounded 10. Device in suspend mode	25 °C	TBD	TBD	TBD	μA
			85 °C	TBD	TBD	TBD	μA
I _{SB2}	Total standby current of Astoria when device is in standby mode	1. *VDDQ = 3.3 V Nominal (3.0–3.6 V) 2. Outputs and Bidirs High or Floating ^[7] 3. XTALOUT Floating 4. D+ Floating, D– Grounded	25 °C	–	–	52	μA
			85 °C	–	–	450	μA
I _{SB3}	Total standby current of Astoria when device is in core power-down mode	1. Outputs and Bidirs High or Floating ^[7] 2. XTALOUT Floating 3. D+ Floating, D– Grounded 4. Core Powered Down	25 °C	–	–	28	μA
			85 °C	–	–	139	μA

Table 13. USB Switch DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{IH}	Input voltage HIGH		1.6	–	–	V
V _{IL}	Input voltage LOW		–	–	0.8	V
R _{ON}	On resistance		4.5	7	10	Ω
R _{OFF}	Off resistance		1M	–	–	Ω
C _{DP/DM_ON}	D+/D– on capacitance (with Full-Speed switch On)		–	–	25	pF
C _{DP/DM_OFF}	D+/D– off capacitance		–	–	20	pF

Table 14. Capacitance

Parameter	Description	Conditions	Typ	Max	Unit
C _{IN}	Input pin capacitance, except D+/D–	TA = 25 °C, f = 1 MHz, V _{CC} = V _{CCIO}	–	9	pF
	Input pin capacitance, D+/D–		–	15	pF
C _{OUT}	Output pin capacitance		–	10	pF

AC Timing Parameters

P Port Interface

PCRAM Non Multiplexing Asynchronous Mode

Table 15. Asynchronous Mode Timing Parameters

Parameter	Description	Min	Max	Unit
Read Timing Parameters				
	Interface bandwidth (MBPS)	–	66.7	MBps
tAA	Address to data valid	–	30	ns
tOH	Data output hold from address change	3	–	ns
tEA	Chip enable to data valid	–	30	ns
tAADV	ADV# to data valid access time	–	30	ns
tAVS	Address valid to ADV# HIGH	5	–	ns
tAVH	ADV# HIGH to address hold	2 ^[10]	–	ns
tCVS	CE# low setup time to ADV# HIGH	5	–	ns
tVPH	ADV# HIGH time	15 ^[9]	–	ns
tVP	ADV# pulse width LOW	7.5	–	ns
tOE	OE# LOW to data valid	–	22.5	ns
tOLZ	OE# LOW to Low Z	3	–	ns
tOHZ	OE# HIGH to High Z	0	22.5	ns
tLZ	CE# LOW to Low Z	3	–	ns
tHZ	CE# HIGH to High Z	–	22.5	ns
Write Timing Parameters				
tCW	CE# LOW to write end	30	–	ns
tAW	Address Valid to write end	30	–	ns
tAS	Address setup to write start	0	–	ns
tADVS	ADV# setup to write start	0	–	ns
tWP	WE# pulse width	22	–	ns
tWPH	WE# HIGH time	10	–	ns
tCPH	CE# HIGH time	10	–	ns
tAVS	Address valid to ADV# HIGH	5	–	ns
tAVH	ADV# HIGH to address hold	2 ^[10]	–	ns
tCVS	CE# LOW setup time to ADV# HIGH	5	–	ns
tVPH	ADV# HIGH time	15 ^[9]	–	ns
tVP	ADV# pulse width LOW	7.5	–	ns
tVS	ADV# LOW to end of write	30	–	ns
tDW	Data setup to write end	18	–	ns
tDH	Data hold from write end	0	–	ns
tWHZ	Write to DQ High Z output	–	22.5	ns
tOW	End of write to Low Z output	3	–	ns

Notes

9. In applications where access cycle time is at least 60 ns, t_{VPH} can be relaxed to 12 ns.

10. In applications where back-to-back accesses are not performed on different endpoint addresses, the minimum t_{AVH} spec. can be relaxed to 0 ns.

Figure 15. Non Multiplexing Asynchronous Pseudo CRAM Mode Single Read Time Parameters

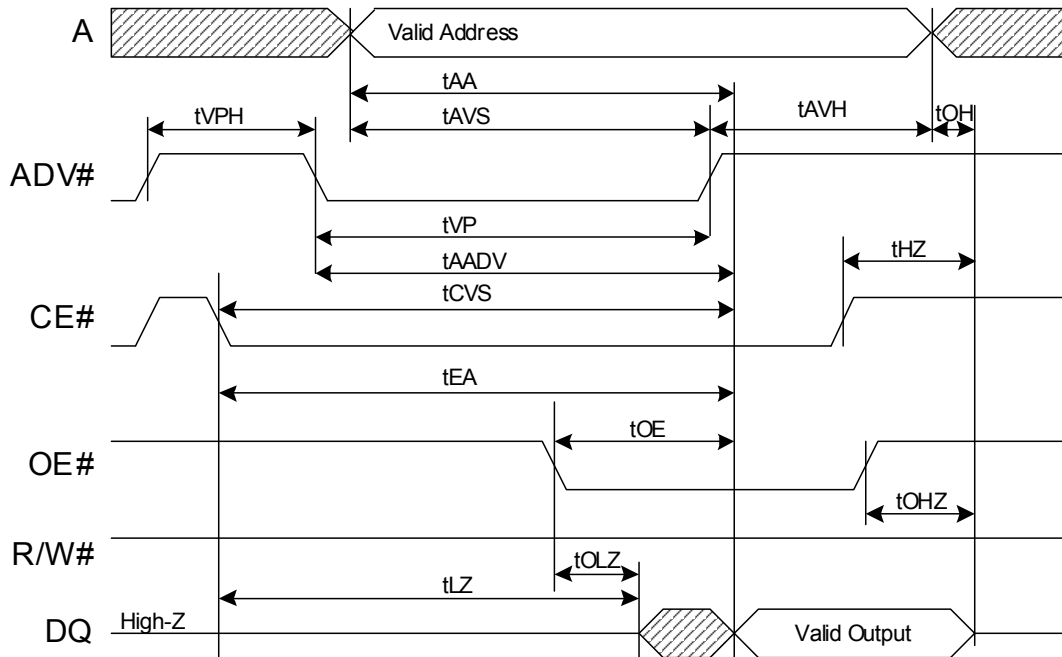


Figure 16. Non Multiplexing Asynchronous Pseudo CRAM mode Back to Back Read Timing Parameters

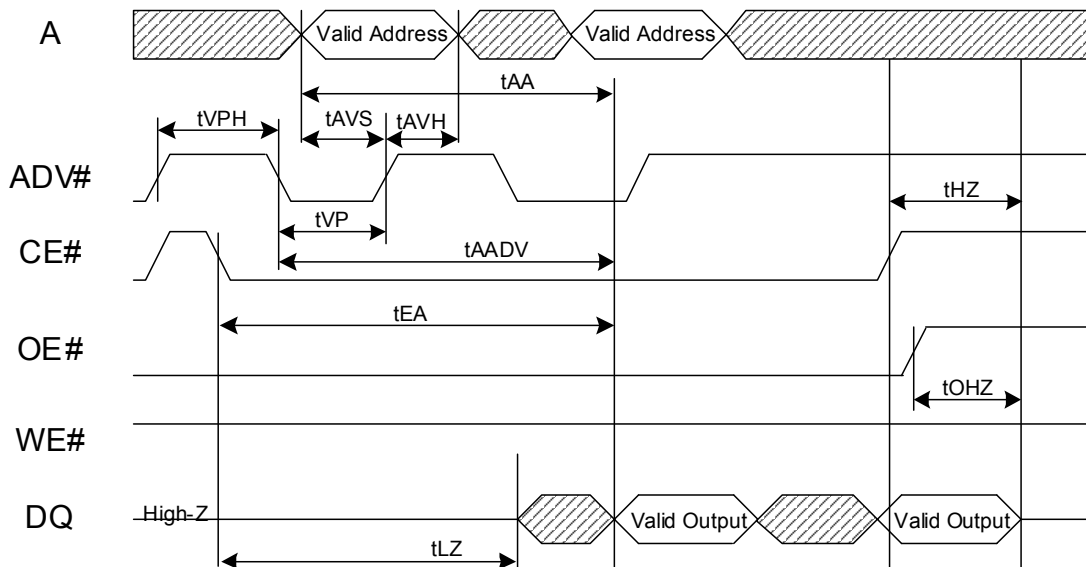


Figure 17. Non Multiplexing Asynchronous Pseudo CRAM Mode Back to Back Write Timing Parameters

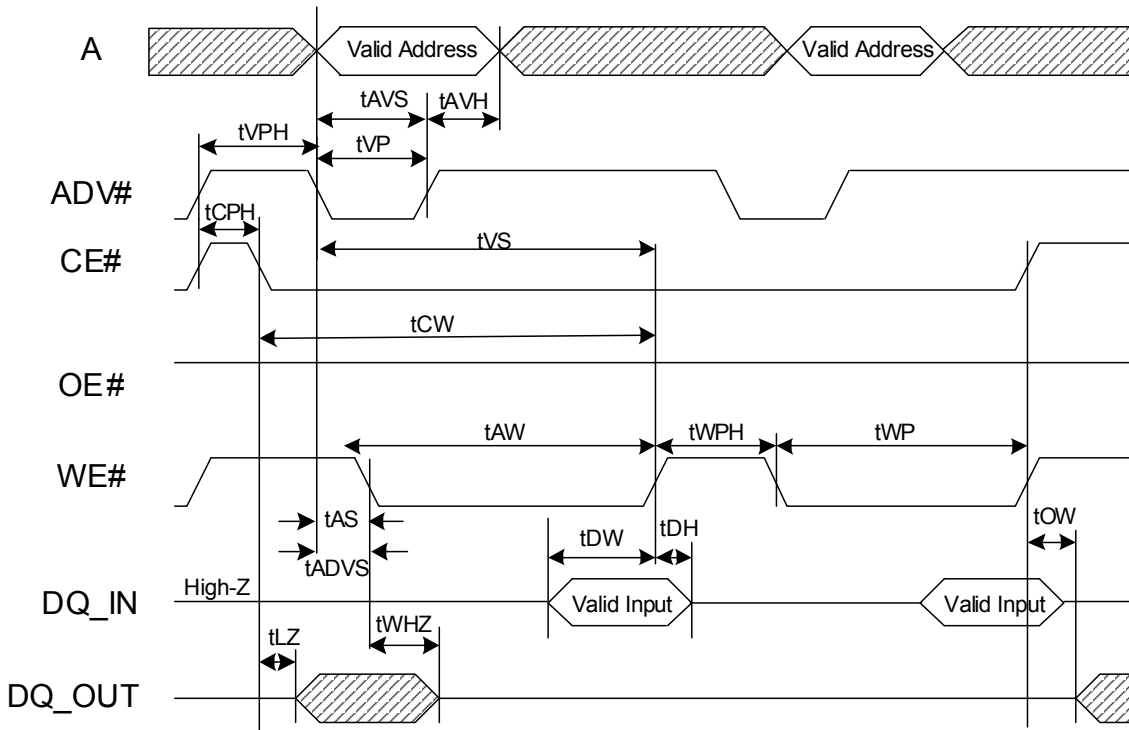


Figure 18. Non Multiplexing Asynchronous Pseudo CRAM Mode Read to Write Timing Parameters

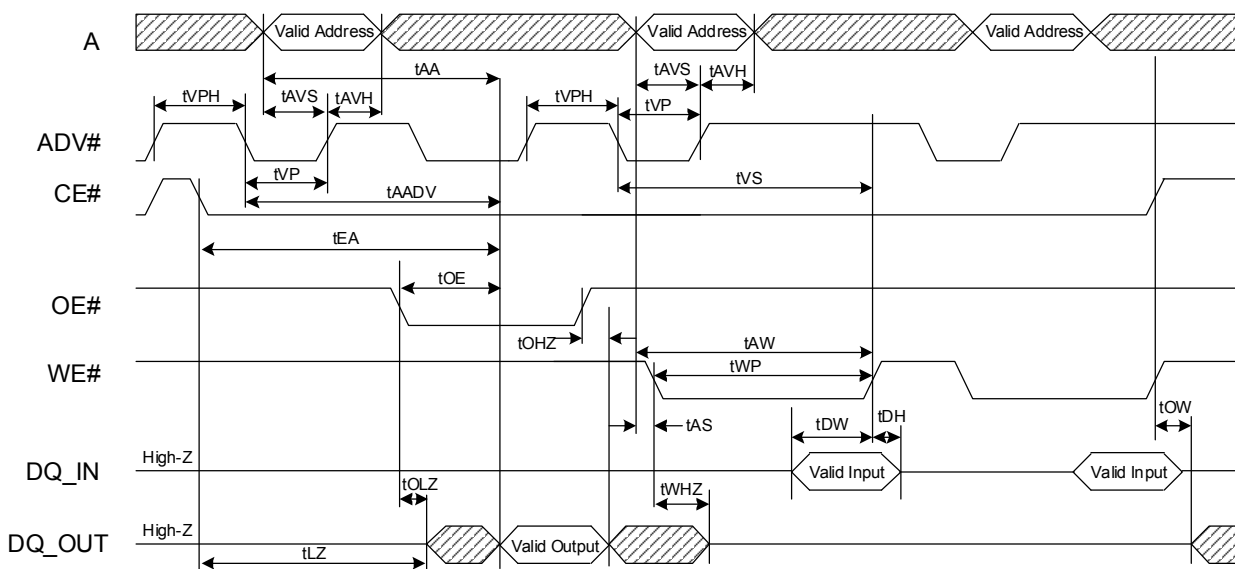
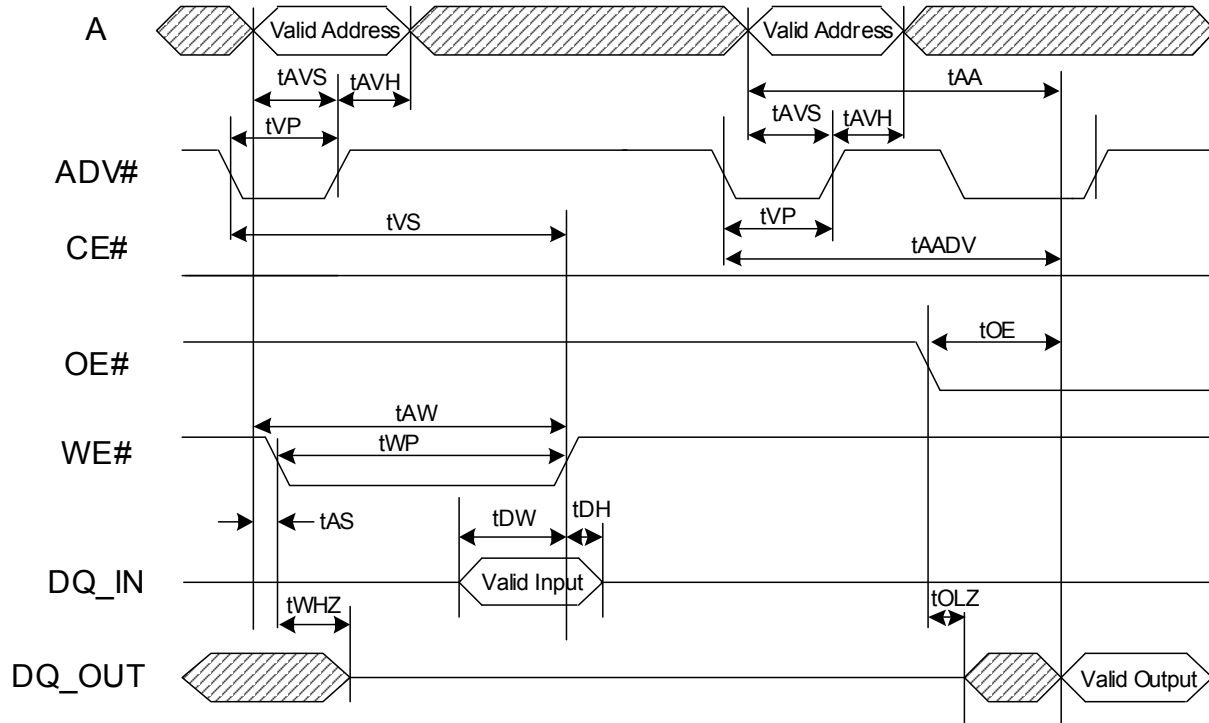


Figure 19. Non Multiplexing Asynchronous Pseudo CRAM Mode Write to Read Timing Parameters



Address Data Multiplexing Asynchronous Mode

Table 16. Address Data Multiplexing Asynchronous Mode Timing Parameters

Parameter	Description	Min	Max	Unit
Read Timing Parameters				
	Interface bandwidth	–	50	MBps
tAA	Address to data valid	–	30	ns
tEA	Chip enable access time	–	30	ns
tAADV	ADV# to data valid access time	–	30	ns
tAVS	Address valid to ADV# HIGH	5	–	ns
tAVH	ADV# HIGH to address hold	2	–	ns
tCVS	CE# LOW setup time to ADV# HIGH	5	–	ns
tVPH	ADV# HIGH time	15	–	ns
tVP	ADV# pulse width LOW	7.5	–	ns
tAVDOE	ADV# HIGH to OE# LOW	0	–	ns
tOE	OE# LOW to data valid	–	22.5	ns
tOLZ	OE# LOW to Low Z	3	–	ns
tOHZ	OE# HIGH to High Z	–	22.5	ns
tLZ	CE# LOW to Low Z	3	–	ns
tHZ	CE# HIGH to High Z	–	22.5	ns
Write Timing Parameters				
tCW	CE# LOW to write end	30	–	ns

Table 16. Address Data Multiplexing Asynchronous Mode Timing Parameters (continued)

Parameter	Description	Min	Max	Unit
tAW	Address valid to write end	30	–	ns
tAVDWE	ADV# HIGH to write start	0	–	ns
tWp	WE# pulse width	22	–	ns
tAVS	Address valid to ADV# HIGH	5	–	ns
tAVH	ADV# HIGH to address hold	2	–	ns
tCVS	CE# LOW setup time to ADV# HIGH	5	–	ns
tVPH	ADV# HIGH time	15	–	ns
tVP	ADV# pulse width LOW	7.5	–	ns
tVS	ADV# LOW to end of write	30	–	ns
tDS	Data setup to write end	18	–	ns
tDH	Data hold from write end	0	–	ns

Figure 20. Address Data Multiplexing Asynchronous Single Read Timing Parameters

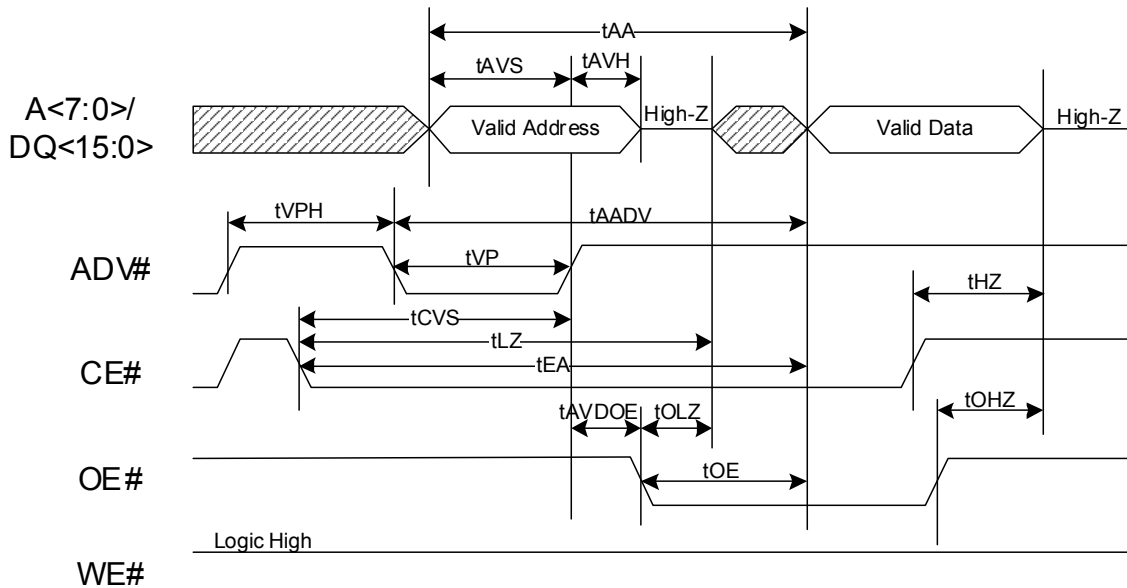
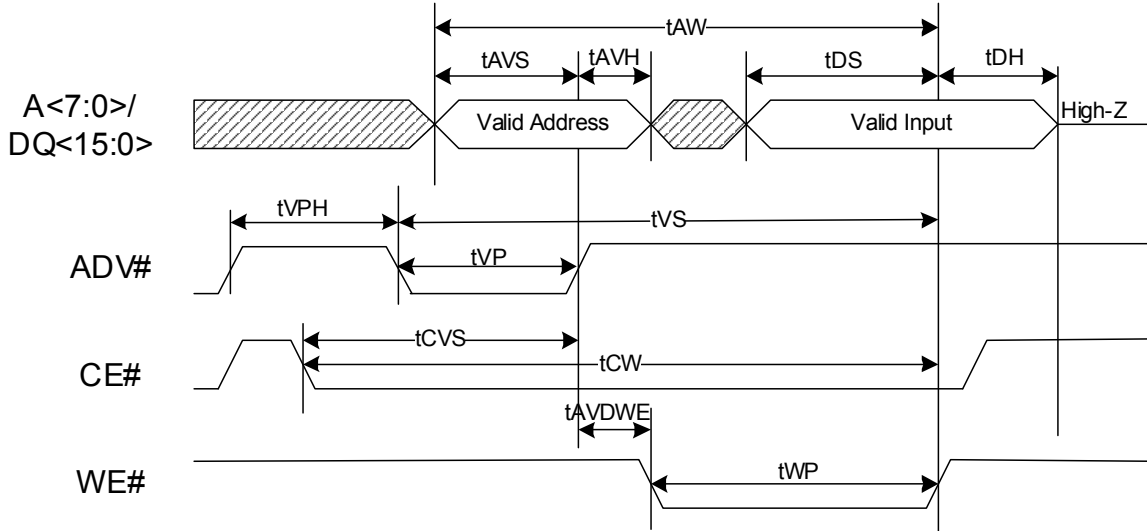


Figure 21. Address Data Multiplexing Asynchronous Single Write Timing Parameters

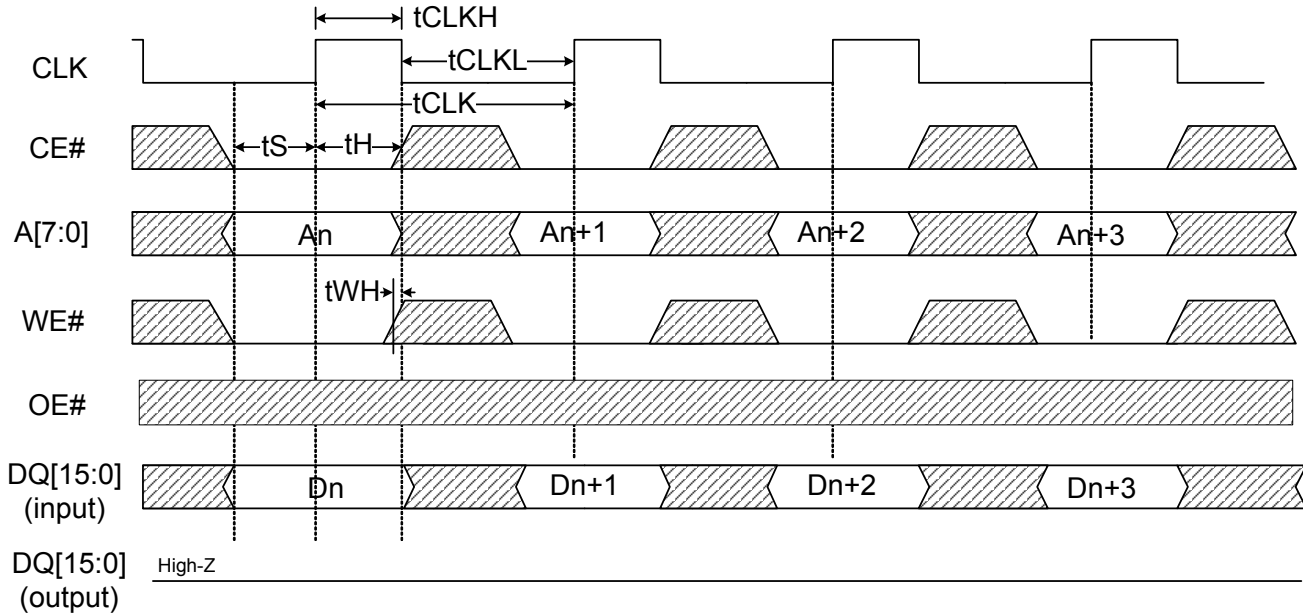


Non Multiplexing Synchronous Mode Timing Parameters

Table 17. Non Multiplexing Synchronous Mode Timing Parameters

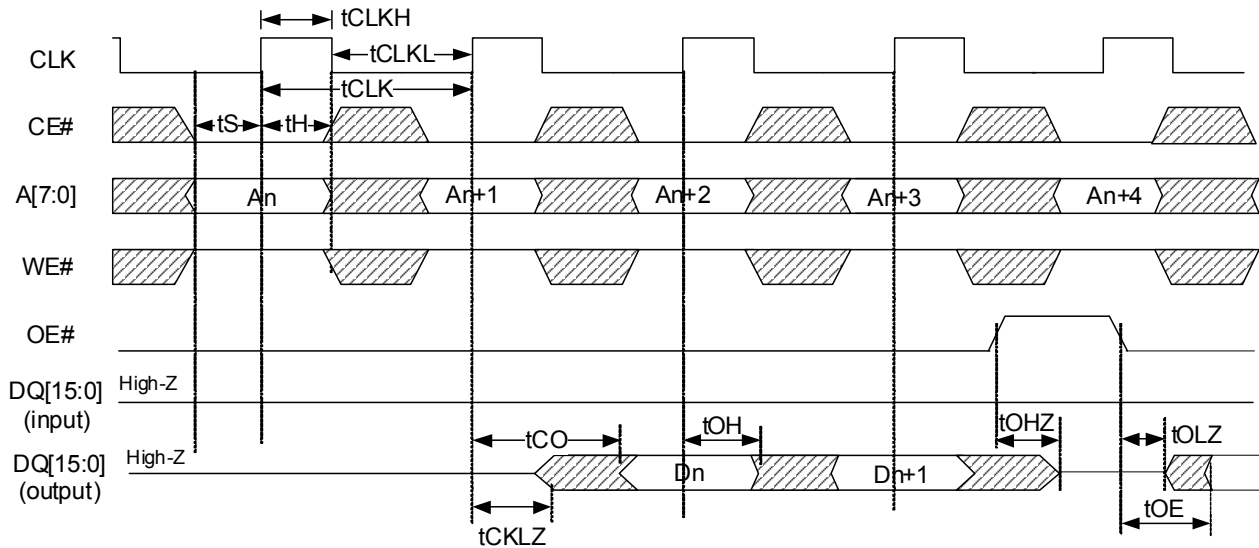
Parameter	Description	Min	Max	Unit
FREQ	Interface clock frequency	–	33	MHz
tCLK	Clock period	30	–	ns
tCLKH	Clock HIGH time	12	–	ns
tCLKL	Clock LOW time	12	–	ns
tWH	Address hold time (write to the register) for the first time that processor configures the P-Port from non-ADM asynchronous mode to non-ADM synchronous mode	0	–	ns
tS	CE#/WE#/ADDR/DQ setup time	7.5	–	ns
tH	CE#/WE#/ADDR/DQ hold time	1.5	–	ns
tCO	Clock to valid data	–	18	ns
tOH	Clock to data hold time	2	–	ns
tOLZ	OE# LOW to data Low Z	3	–	ns
tOHZ	OE# HIGH to data High Z	–	22.5	ns
tOE	OE# LOW to data valid	–	22.5	ns
tCKHZ	Clock to data High Z	–	18	ns
tCKLZ	Clock to data Low Z	3	–	ns

Figure 22. Non Multiplexing Synchronous Pseudo CRAM Mode Write Timing Parameters



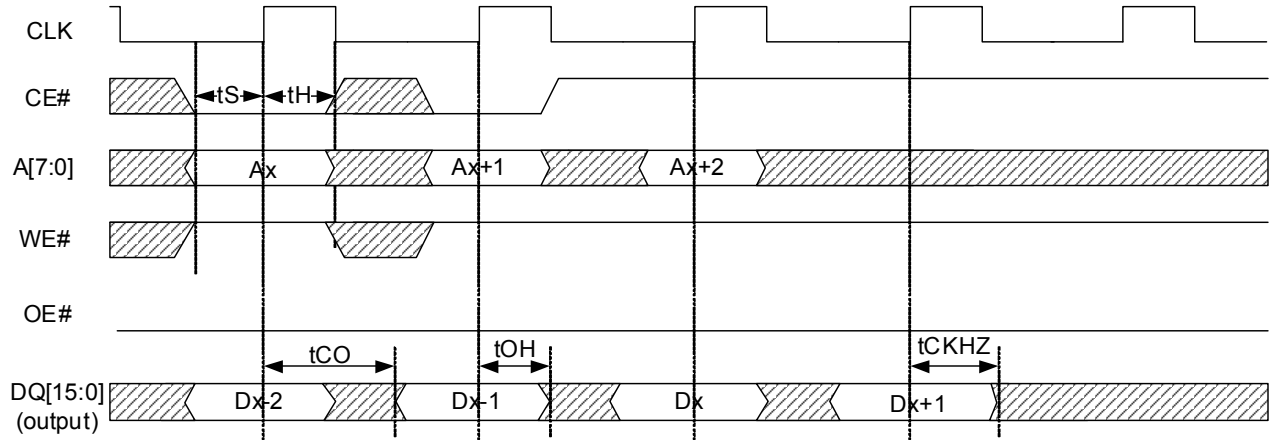
Note:
 - Assumes previous cycle had CE# deselected
 - OE# is don't care during write operations

Figure 23. Non Multiplexing Synchronous Pseudo CRAM Mode Read Timing Parameters



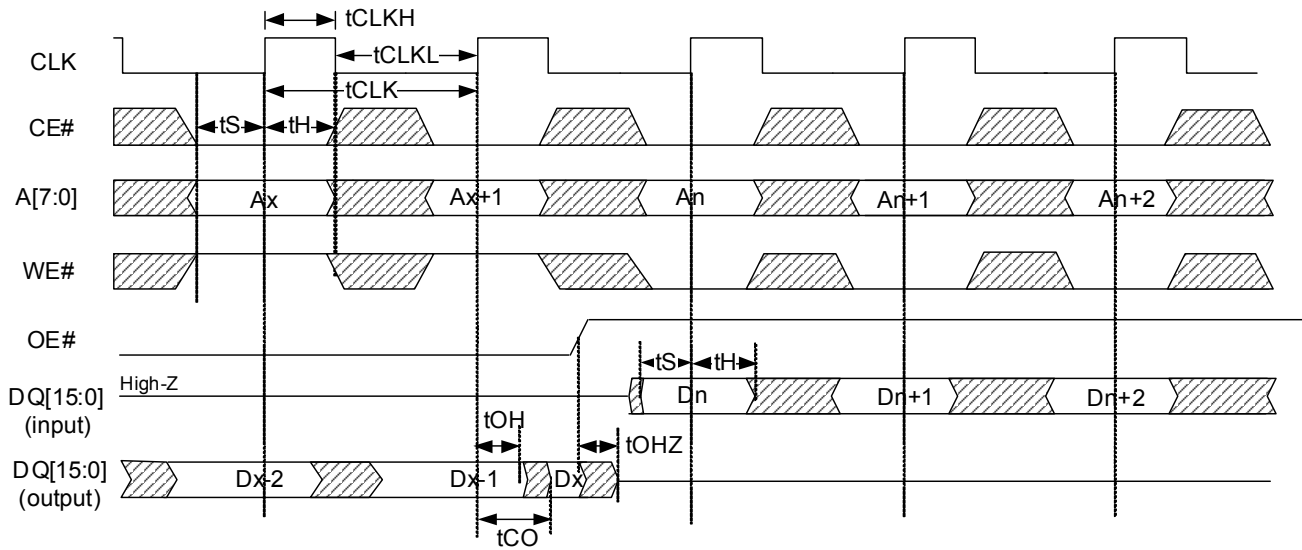
Note:
 - Assumes previous cycle had CE# deselected

Figure 24. Non Multiplexing Synchronous Mode Read (OE# Fixed LOW) Timing Parameters



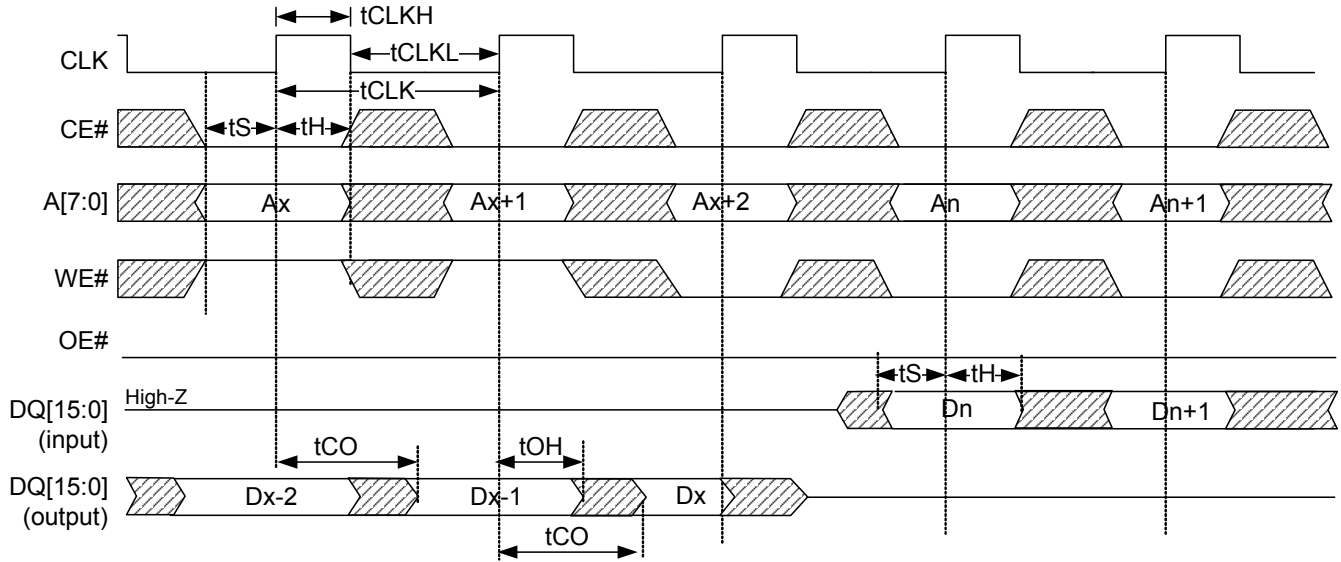
Note:
- Assumes previous several cycles were Read

Figure 25. Non Multiplexing Synchronous Mode Read to Write (OE# Controlled) Timing Parameters



Note:
- Assumes previous several cycles were Read
- (Ax) and (Ax+1) cycles are turnaround. (Ax+1) operation does not cross pipeline.

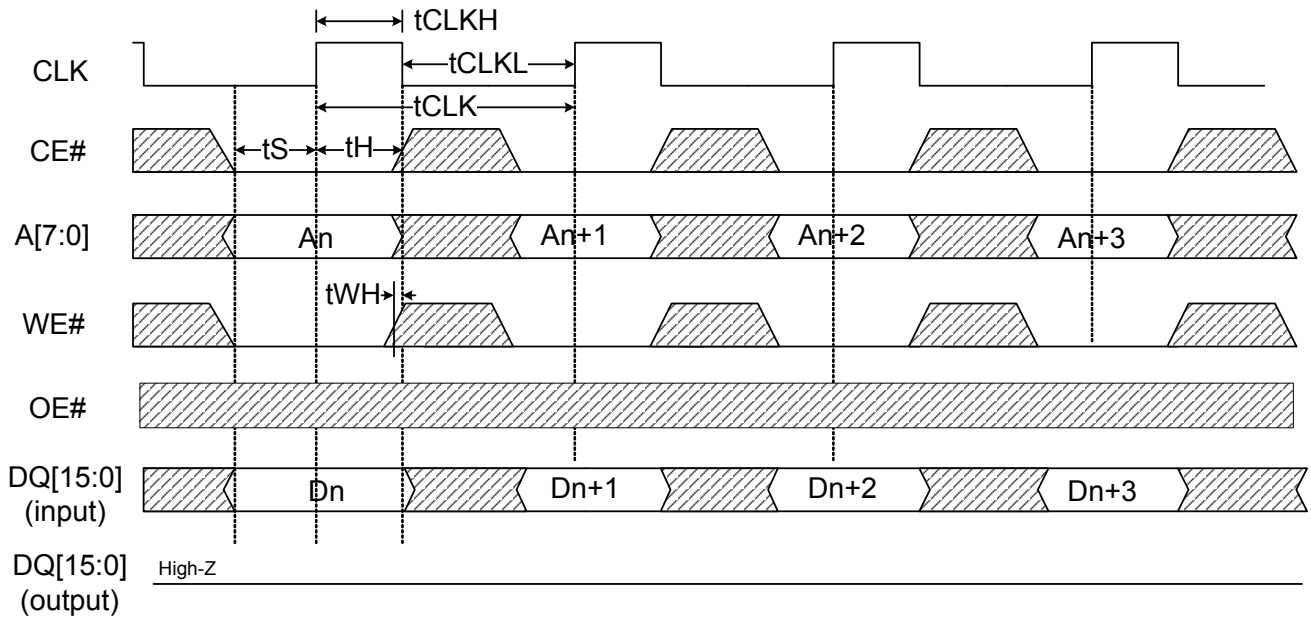
Figure 26. Non Multiplexing Synchronous Mode Read to Write (OE# Fixed LOW) Timing Parameters



Note:

- Assumes previous several cycles were Read
- In this scenario, OE# is held LOW
- (Ax) and (Ax+1) cycles are turnaround. (Ax+1) operation does not cross pipeline.
- No operation is performed during the Ax+2 cycle (true turnaround operation)

Figure 27. Non Multiplexing Synchronous Mode Write to Read Timing Parameters



Note:

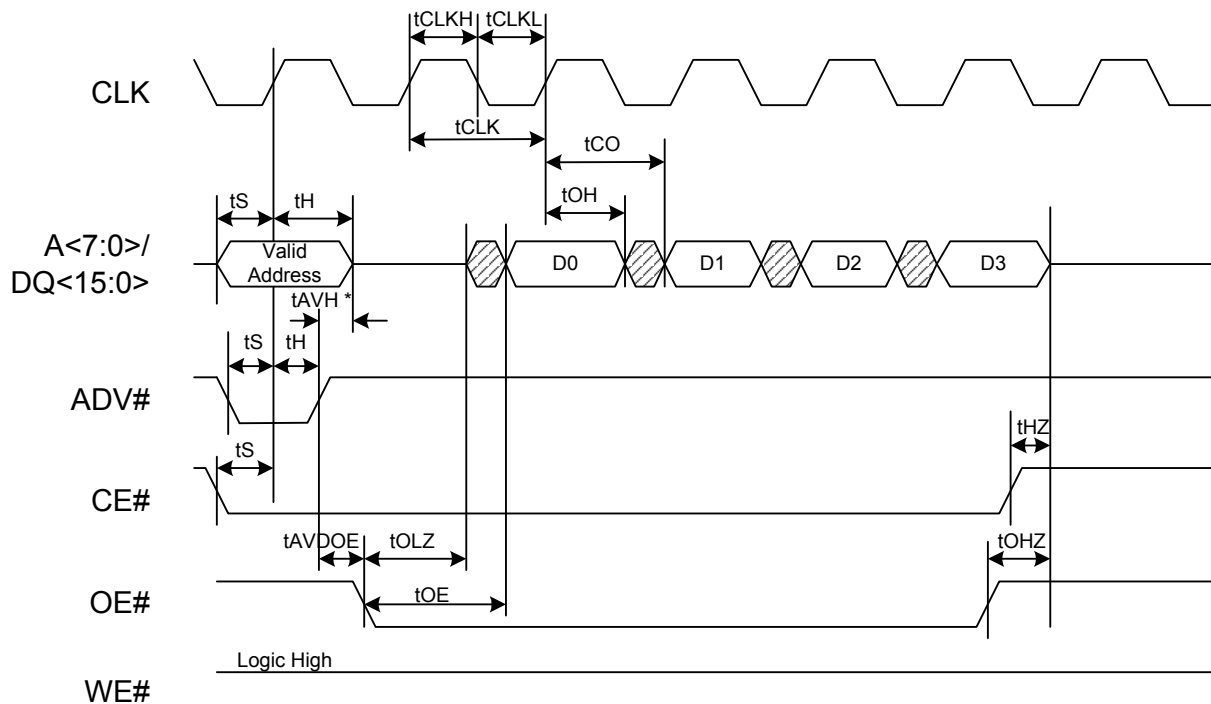
- Assumes previous cycle had CE# deselected
- OE# is don't care during write operations

Address Data Multiplexing Synchronous Mode

Table 18. Address Data Multiplexing Synchronous Mode Parameters

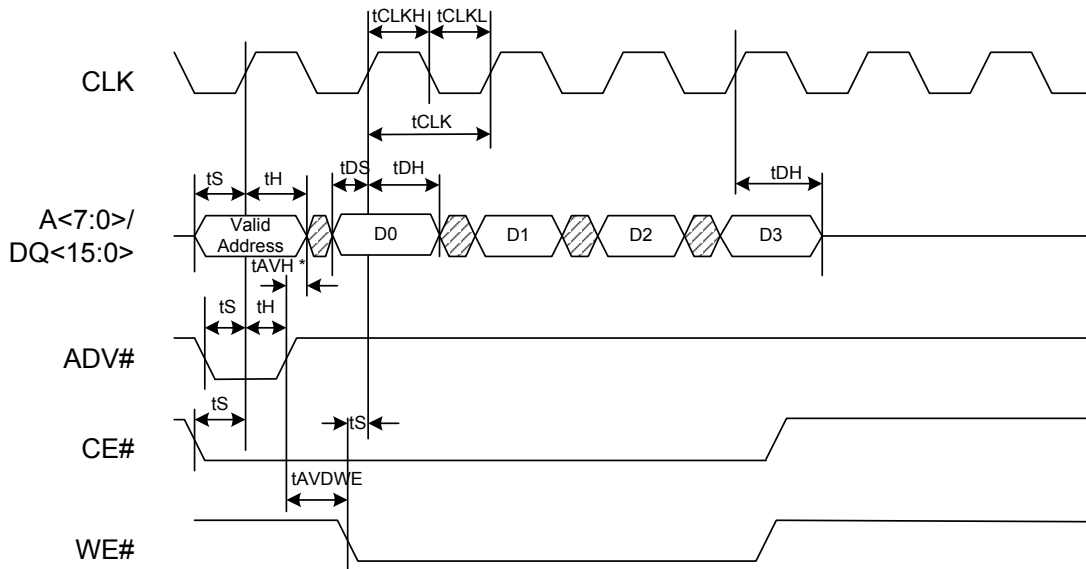
Parameter	Description	Min	Max	Unit
FREQ	Interface clock frequency	–	33	MHz
tAVH	Address hold time (write to the register) for the first time that processor configures the P-Port from ADM asynchronous mode to ADM synchronous mode	2	–	ns
tCLK	Clock period	30	–	ns
tCLKH	Clock High time	12	–	ns
tCLKL	Clock Low time	12	–	ns
tS	CE#/WE#/DQ setup time	7.5	–	ns
tH	CE#/WE#/DQ hold time	1.5	–	ns
tCO	Clock to valid data	–	18	ns
tOH	Clock to data hold time	2	–	ns
tAVDOE	ADV# HIGH to OE# LOW	0	–	ns
tAVDWE	ADV# HIGH to WE# LOW	0	–	ns
tHZ	CE# HIGH to data High Z	–	22.5	ns
tOHZ	OE# HIGH to data High Z	–	22.5	ns
tOLZ	OE# LOW to data Low Z	3	–	ns
tOE	OE# LOW to data Valid	–	22.5	ns

Figure 28. Address Data Multiplexing Synchronous Burst Read Timing Parameters (Burst of 4 with Latency=2, WE#=HIGH)



* tAVH is the ADM address hold time (write to the register) for the first time that Processor configure the P-Port Astoria from ADM Async mode to ADM Sync mode

Figure 29. Address Data Multiplexing Synchronous Burst Write Timing Parameters (Burst of 4 with Latency=2, OE# is Ignored)



* tAVH is the ADM address hold time (write to the register) for the first time that Processor configure the P-Port Astoria from ADM Async mode to ADM Sync mode

Table 19. Asynchronous SRAM Mode Timing Parameters

Parameter	Description	Min	Max	Unit
	Interface bandwidth (MBPS)	–	66.7	MBPS
Read Timing Parameters				
tRC	Read cycle time	30	–	ns
tAA	Address to data valid	–	30	ns
tOH	Data output hold from address change	3	–	ns
tEA	Chip enable to data valid	–	30	ns
tOE	OE# LOW to data valid	–	22.5	ns
tOLZ	OE# LOW to Low Z	3	–	ns
tOHZ	OE# HIGH to High Z	0	22.5	ns
tLZ	CE# LOW to Low Z	3	–	ns
tHZ	CE# HIGH to High Z	–	22.5	ns
Write Timing Parameters				
tWC	Write cycle time	30	–	ns
tCW	CE# LOW to write end	30	–	ns
tAW	Address valid to WE# end	30	–	ns
tAS	Address setup to WE# or CE# start	0	–	ns

Table 19. Asynchronous SRAM Mode Timing Parameters (continued)

Parameter	Description	Min	Max	Unit
tAH	Address hold time from WE# or CE# end for PCRAM to SRAM changes (Astoria is default in the PCRAM mode after RESET. This timing is the requirement for the first time to access the P-Port Interface Configuration Register to change the Astoria to PSRAM mode)	2	–	ns
	Address hold time from WE# or CE# end for PSRAM mode	0	–	
tWP	WE# pulse width	22	–	ns
tWPH	WE# HIGH time	10	–	ns
tCPH	CE# HIGH time	10	–	ns
tDS	Data setup to write end	18	–	ns
tDH	Data hold from write end	0	–	ns
tWHZ	Write to DQ High Z output	–	22.5	ns
tOW	End of write to Low Z output	3	–	ns
tDPW	DRQ# pulse width	110	–	ns

Non Multiplexing Asynchronous SRAM Mode

Figure 30. Non Multiplexing Asynchronous SRAM Read Timing Parameters

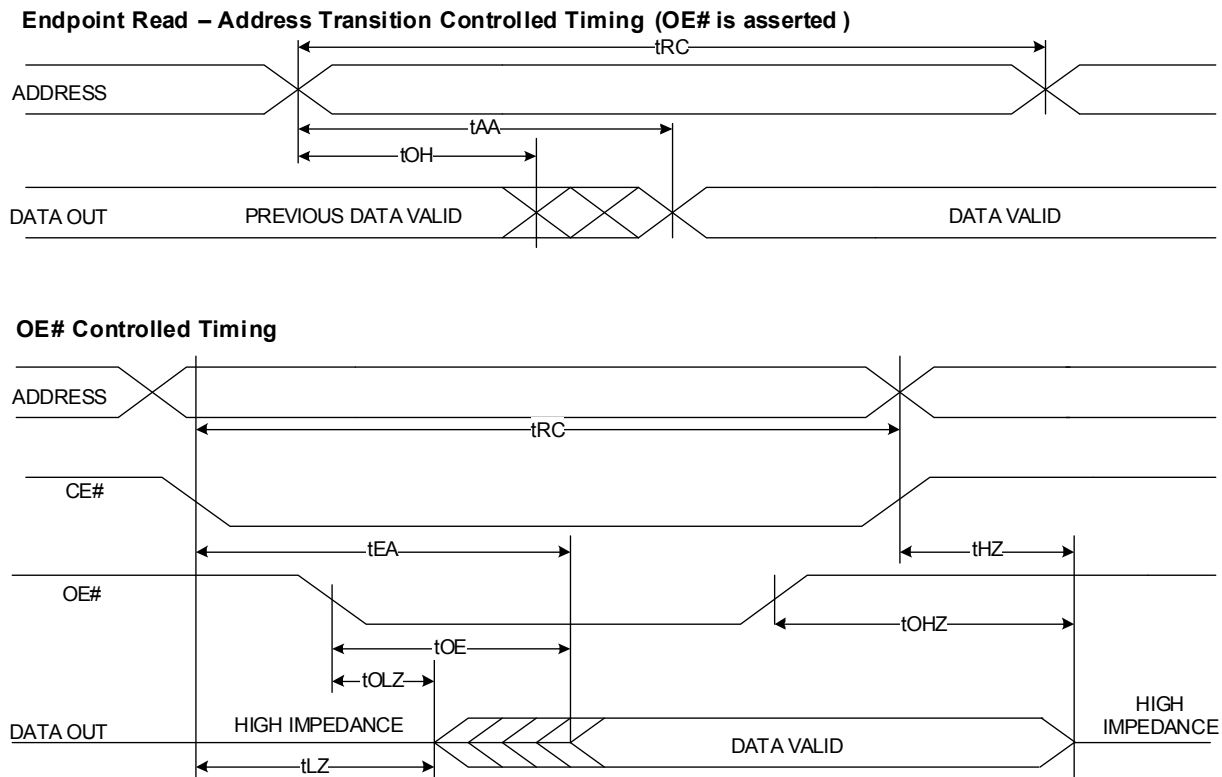
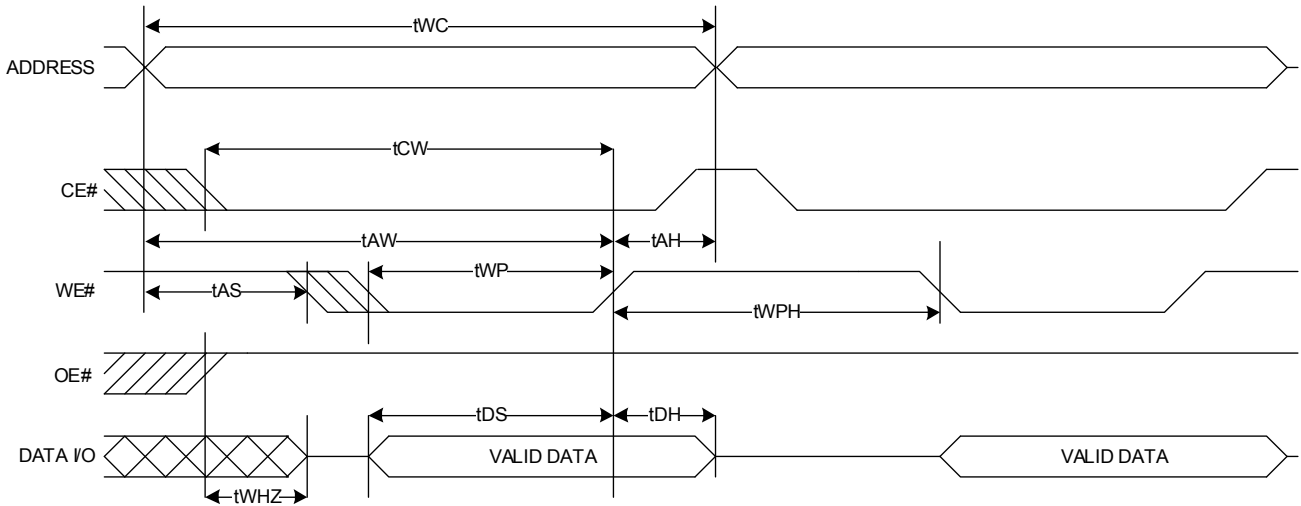


Figure 31. Non Multiplexing Asynchronous SRAM Write Timing (WE# and CE# Controlled)

Write Cycle 1 WE# Controlled, OE# High During Write



Write Cycle 2 CE# Controlled, OE# High During Write

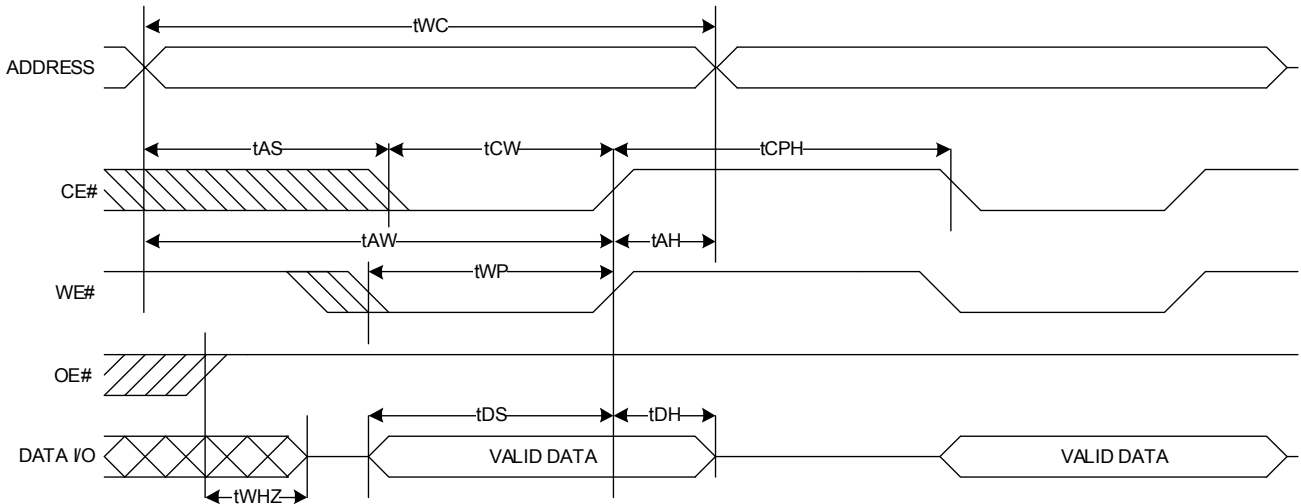
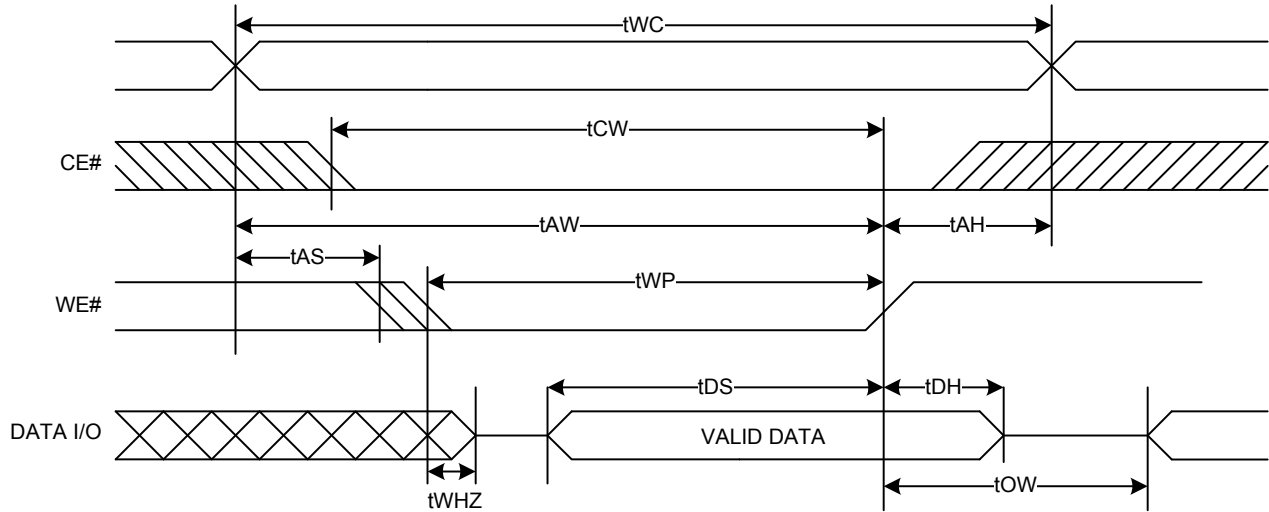


Figure 32. Non Multiplexing Asynchronous SRAM Write Timing (WE# Controlled, OE# LOW)

Write Cycle 3 WE# Controlled. OE# Low



Pseudo NAND (PNAND) Mode

Table 20. PNAND Mode Parameters

Parameter	Description	Min	Max	Unit	
tADL	Address to data loading time	Non LNA Mode Register Write	100	–	ns
		Non LNA Mode EP Write	100	–	ns
		LNA Mode	450	–	ns
tALH	ALE hold time	5	–	ns	
tALS	ALE setup time	15	–	ns	
tAR	ALE to RE# delay	10	–	ns	
tBERS	Block erase time	MCU/S-Port NAND dependent			
tCEA	CE# access time	–	35	ns	
tCH	CE# hold time	5	–	ns	
tCHZ	CE# HIGH to O/P HI-Z	–	40	ns	
tCLH	CLE hold time	5	–	ns	
tCLR	CLE to RE# time	10	–	ns	
tCLS	CLE setup time	15	–	ns	
tCS	CE# setup time	20	–	ns	
tDH	Data hold time	5	–	ns	
tDS	Data setup time	15	–	ns	
tOH	Data output hold time	15	–	ns	

Table 20. PNAND Mode Parameters (continued)

Parameter	Description	Min	Max	Unit
tPROG	Program time for LNA mode	Depends on MCU/S-Port/NAND		ns
	Program time for register write in non LNA mode	130	–	ns
	Program time for EP write in non LNA mode	130	–	ns
tR	Busy duration during Non LNA register read using page read	130	–	ns
	Busy duration during non LNA EP read using page read	130	–	ns
	Busy duration during LNA page read (SBD/SLD)	Depends on MCU/S-Port/NAND		ns
tRC	Read cycle time (VFBGA Package)	30	–	ns
	Read cycle time (WLCSP package)	33	–	
tREA	RE# for register access time	–	30	ns
	RE# for EP access time	–	30	ns
tREH	RE# HIGH hold time	10	–	ns
tRHW	RE# HIGH to WE LOW	40	–	ns
tRHZ	RE# HIGH to output High Z	–	40	ns
tRP	RE# pulse width	15	–	ns
tRR	Ready to RE LOW	20	–	ns
tRST	Device reset time	Depends on MCU/S-Port/NAND		ns
tWB	WE# HIGH to busy	–	100	ns
tWC	Write cycle time (VFBGA package)	30	–	ns
	Write Cycle Time (WLCSP package)	33	–	
tWH	WE# HIGH hold time	10	–	ns
tWHR	WE# HIGH to RE LOW in non LNA mode	30	–	ns
	WE# HIGH to RE LOW in LNA mode	450	–	
tWP	WE# pulse width	15	–	ns

Figure 33. PNAND Mode Command Latch Cycle

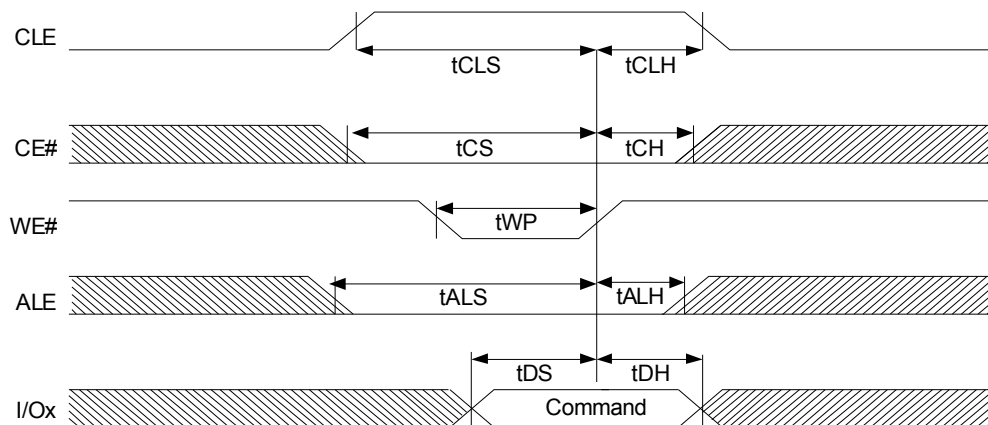


Figure 34. PNAND Mode Address Latch Cycle

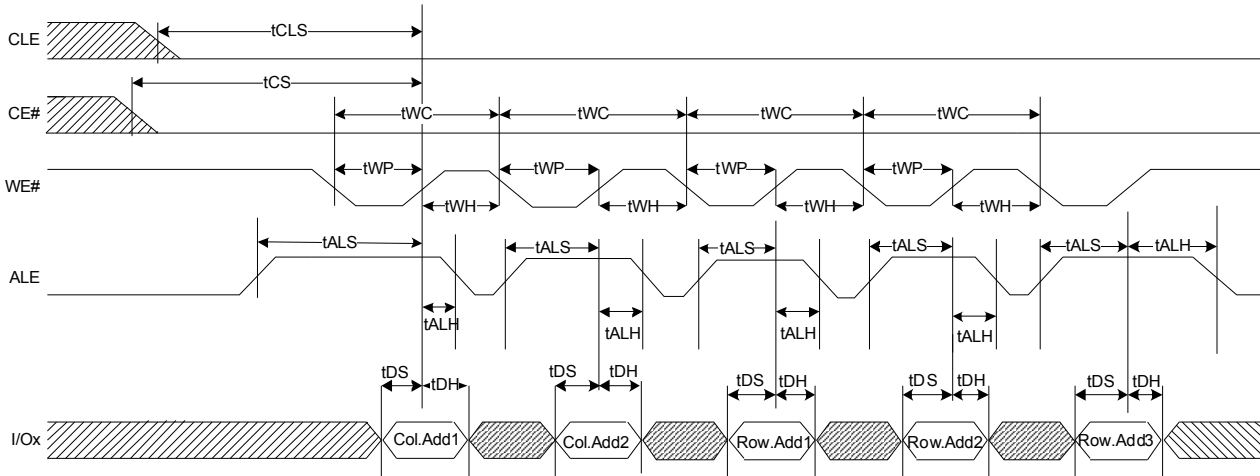


Figure 35. PNAND Mode Input Data Latch Cycle

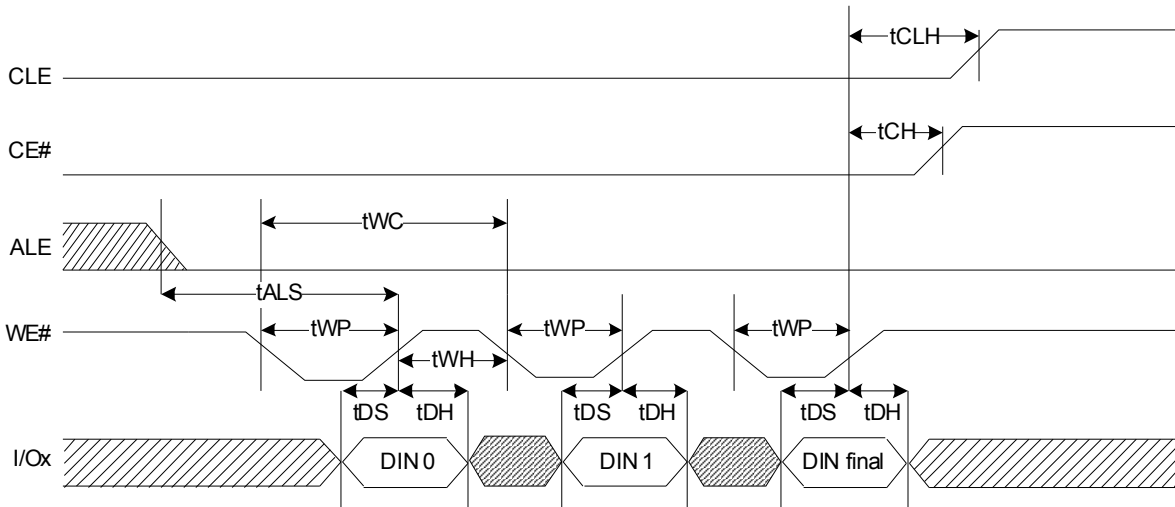


Figure 36. PNAND Mode Serial Access Cycle After Read

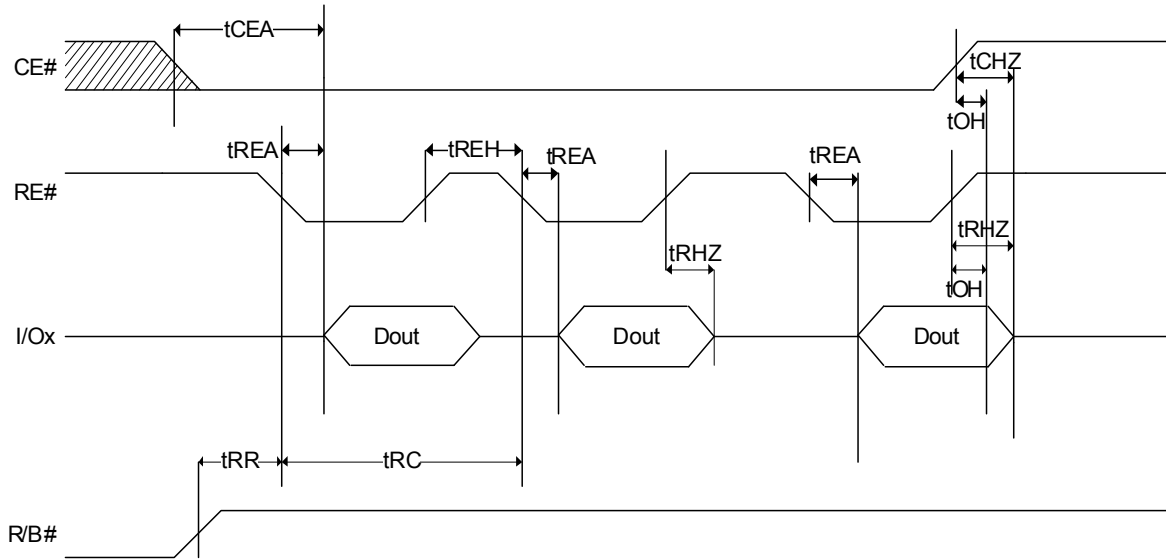


Figure 37. PNAND Mode Status Read Cycle

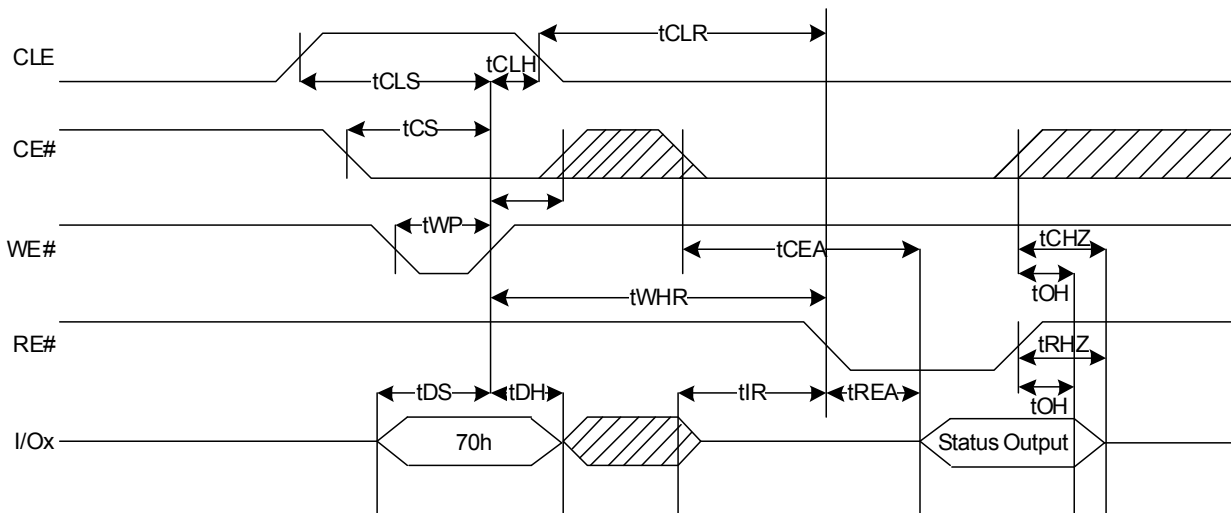


Figure 38. PNAND LBD Read Operation

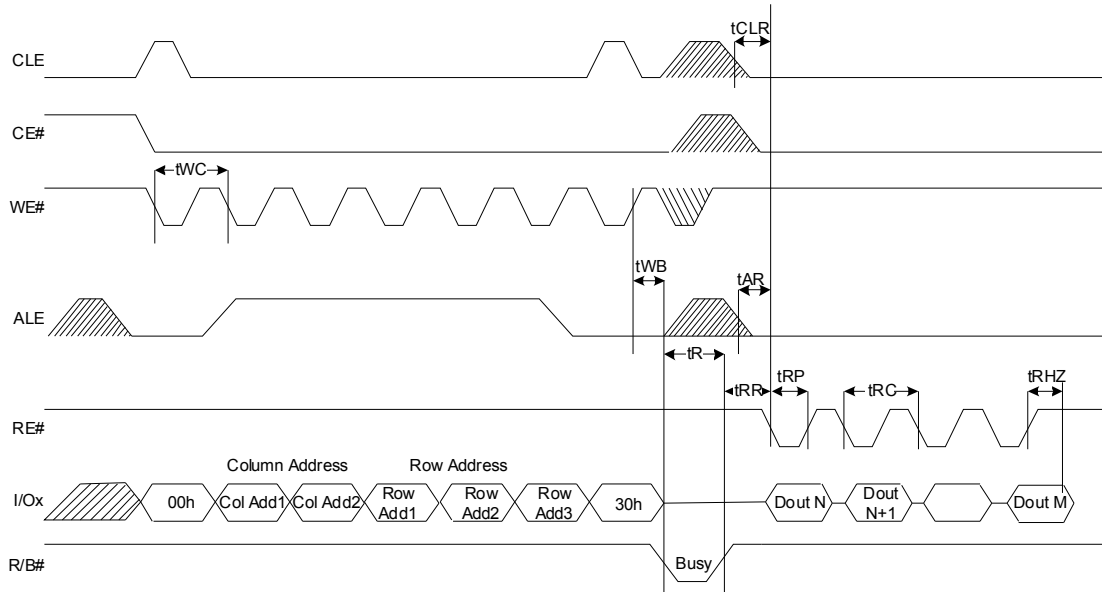


Table 21. Page-Read Command Sequence for Large-Block Devices

Cycle type	IO bus	Comments
CMD0	00h	Page-read command - 1 st cycle
CA0	EP_Offset[7:0]/ REG_Addr[7:0]	REG_Sel field determines how the two column address cycles are interpreted EP_Offset[11:10] = REG_Sel = 2'b11 ‡ Register EP_Offset[11:10] = REG_Sel = 2'b0x, 2'b10 ‡EP buffer offset EP_Offset[11:0] = EP buffer offset
CA1	{4'b0000, EP_Offset[11:8]}	
RA0	Row address byte 0	
RA1	Row address byte 1	The number row-address bytes present in Page-read command depend on RA_COUNT configuration parameter setting. LNA row addresses are interpreted by firmware;
RA2	Row address byte 2	
RA3	Row address byte 3	
CMD1	30h	Page-read command - 2 nd cycle
Data[0-2111]	Data	Data is returned by Astoria delay t _{IR} beyond the second command.

Figure 39. PNAND LBD Read Operation

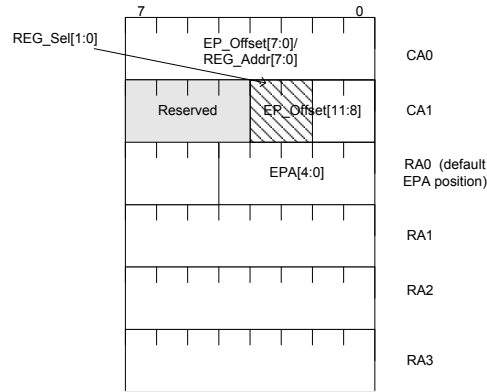


Figure 40. PNAND SBD Read Operation

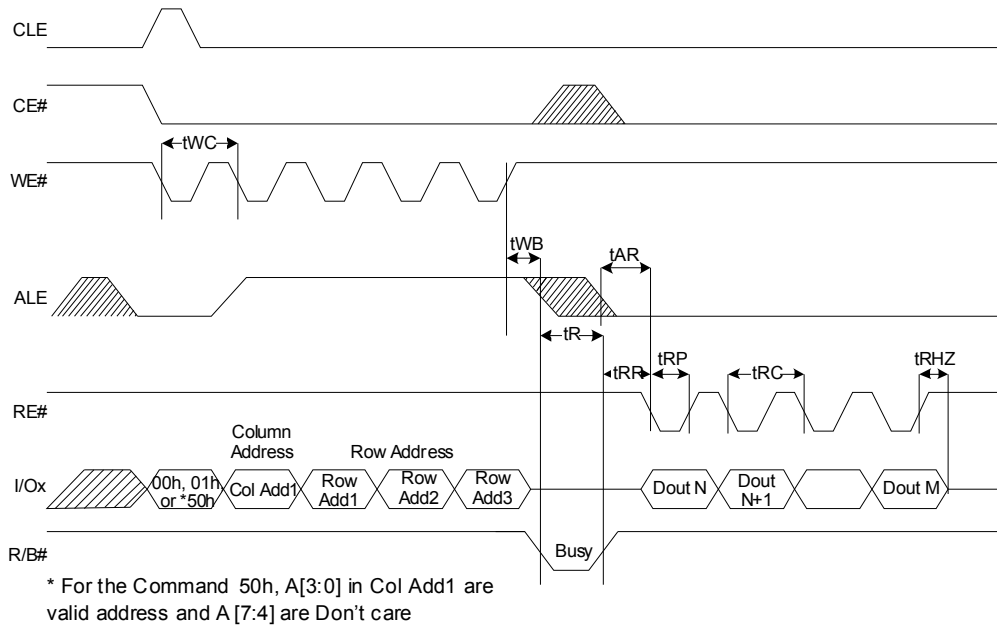


Table 22. Page-Read Command Sequence for Small-Block Devices

Cycle type	IO bus	Comments
CMD0	00h/01h/50h	Sets base-address within page as 0, 256, or 512, for read operation.
CA0	EP_Offset[7:0]/ REG_Addr[7:0]	EP_Offset[7:0] = EP buffer offset for non-register accesses. REG_Addr[7:0] specifies register address when EPA[4:0] field = 5'b10000.
RA0	Row address byte 0	First row-address cycle RA0[4:0] = default EPA – Endpoint address EPA may be specified in any other row-address byte.
RA1	Row address byte 1	The number row-address bytes present in Page-read command depend on RA_COUNT configuration parameter setting. LNA row addresses are interpreted by firmware;
RA2	Row address byte 2	
RA3	Row address byte 3	
Data[0-527]	Data	Data is returned by Astoria delay tR beyond the second command.

Figure 41. Small Block Device Mode Address Cycles

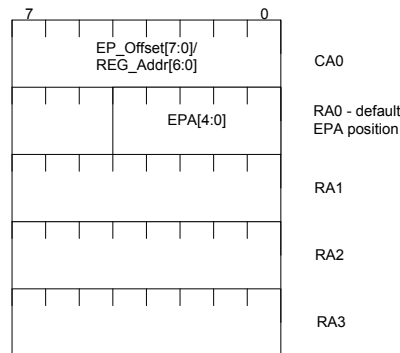


Figure 42. PNAND Mode LBD Random Data Operation (CASDO)

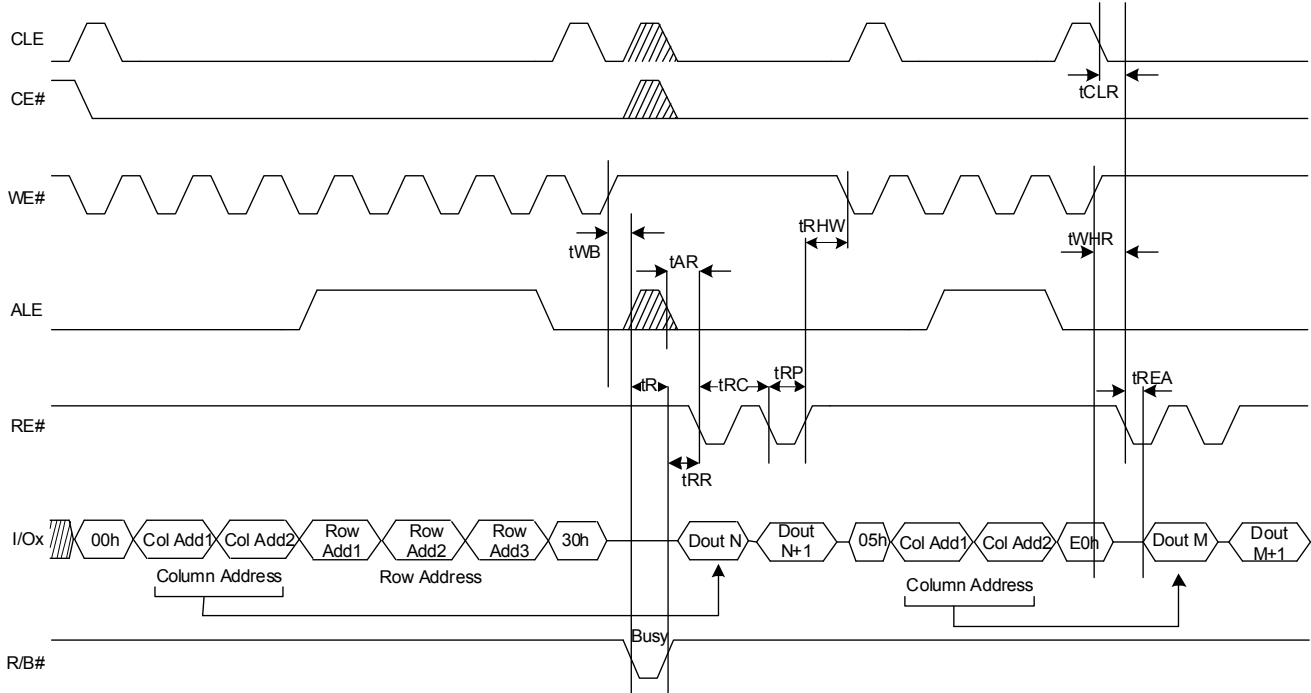
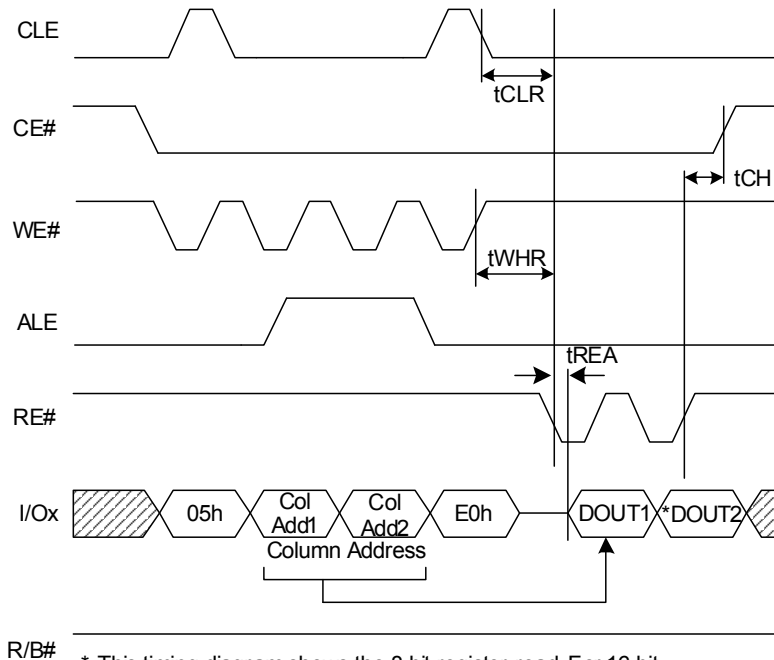


Figure 43. PNAND Mode Register Read Using CASDO in 8-Bit Mode



R/B# * This timing diagram shows the 8-bit register read. For 16-bit register read, DOUT2 is not available

Figure 44. PNAND Mode LBD Read Operation (With CE# Don't Care)

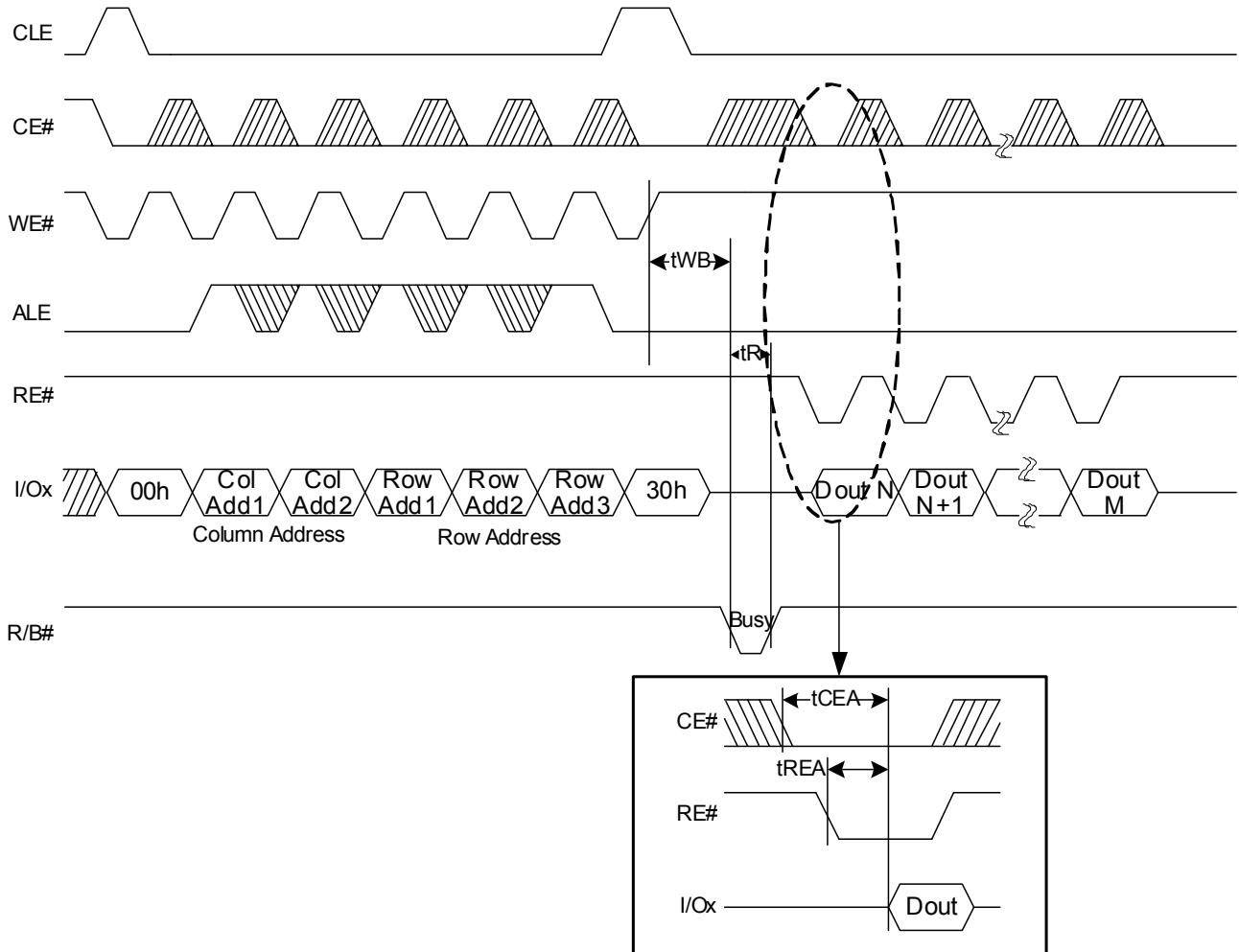


Figure 45. PNAND Mode SBD Read Operation (With CE# Don't Care)

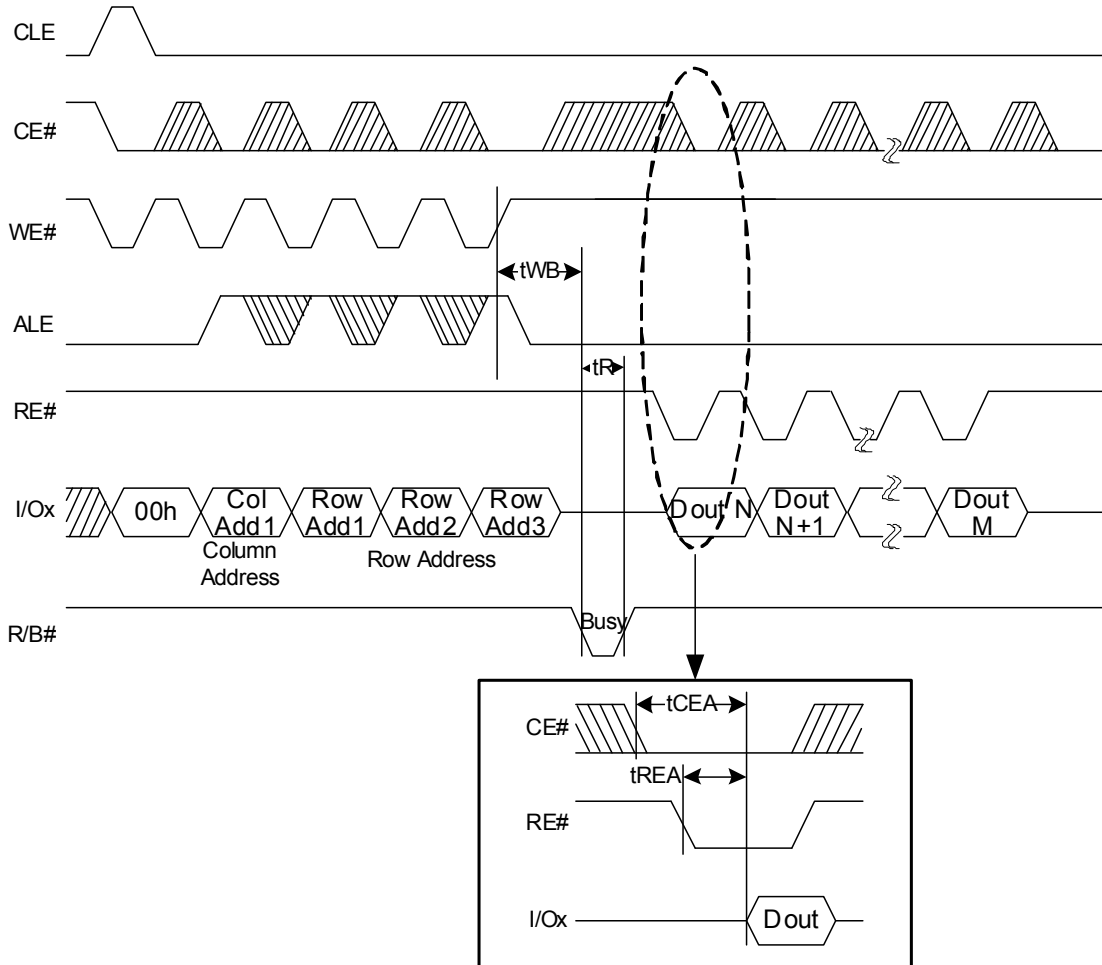
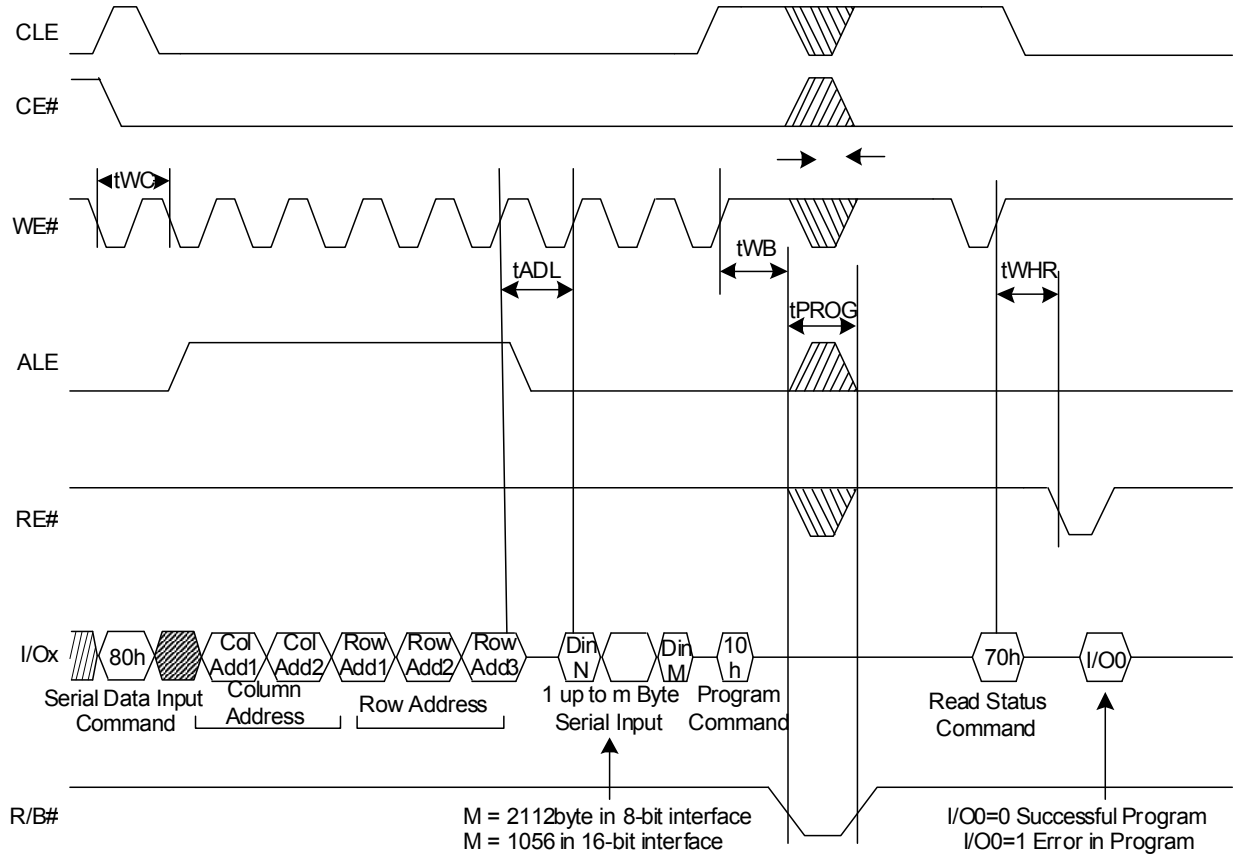


Figure 46. PNAND Mode LBD Page Program Operation



Note: t_{ADL} is the time from WE rising edge of final address cycle to the WE rising edge of first data cycle

Figure 47. PNAND Mode SBD Page Program Operation

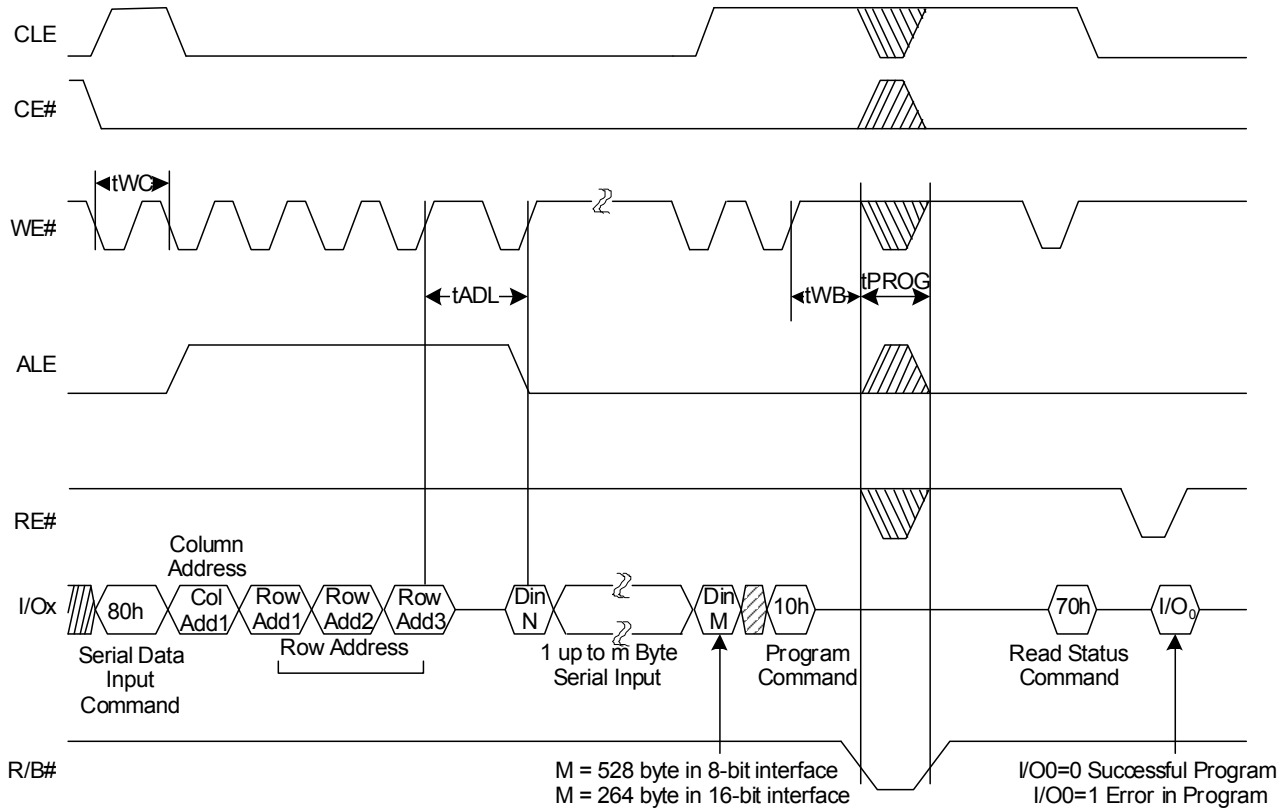
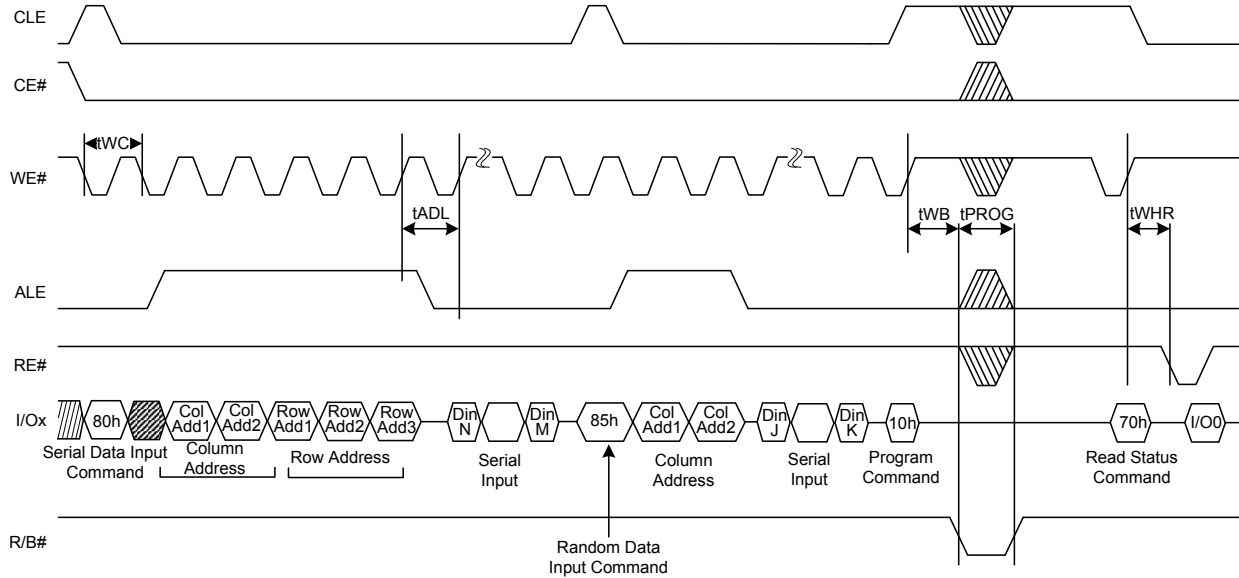
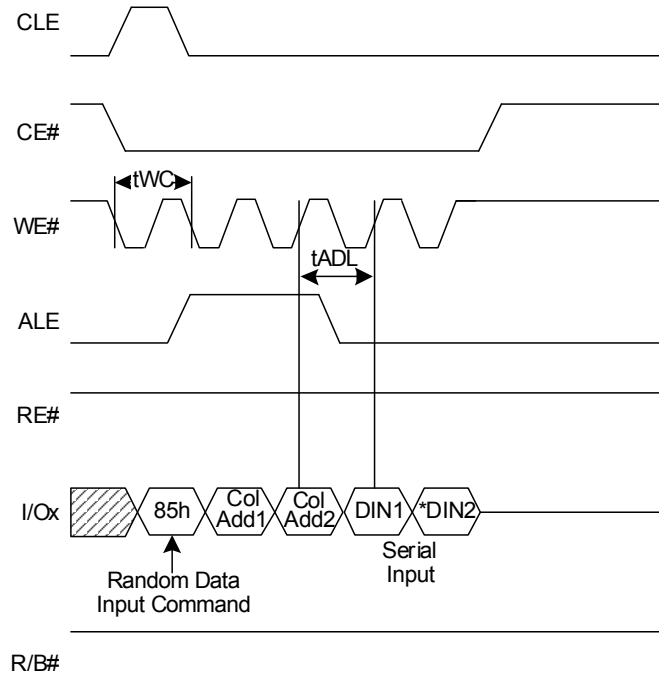


Figure 48. PNAND Mode LBD Page Program Operation with Random Data Input (CASDI)



*Random Programming (CASDI) to endpoint is only supported during logical NAND emulation (LNA mode) of LBD device. Partial page programming is not supported

Figure 49. PNAND Mode Register Write Using CASDI in 8-Bit Mode



* This timing diagram shows the 8-bit register write. For 16-bit register write, DIN2 should not be available

Figure 50. PNAND Mode LBD Page Program Operation (With CE# Don't Care)

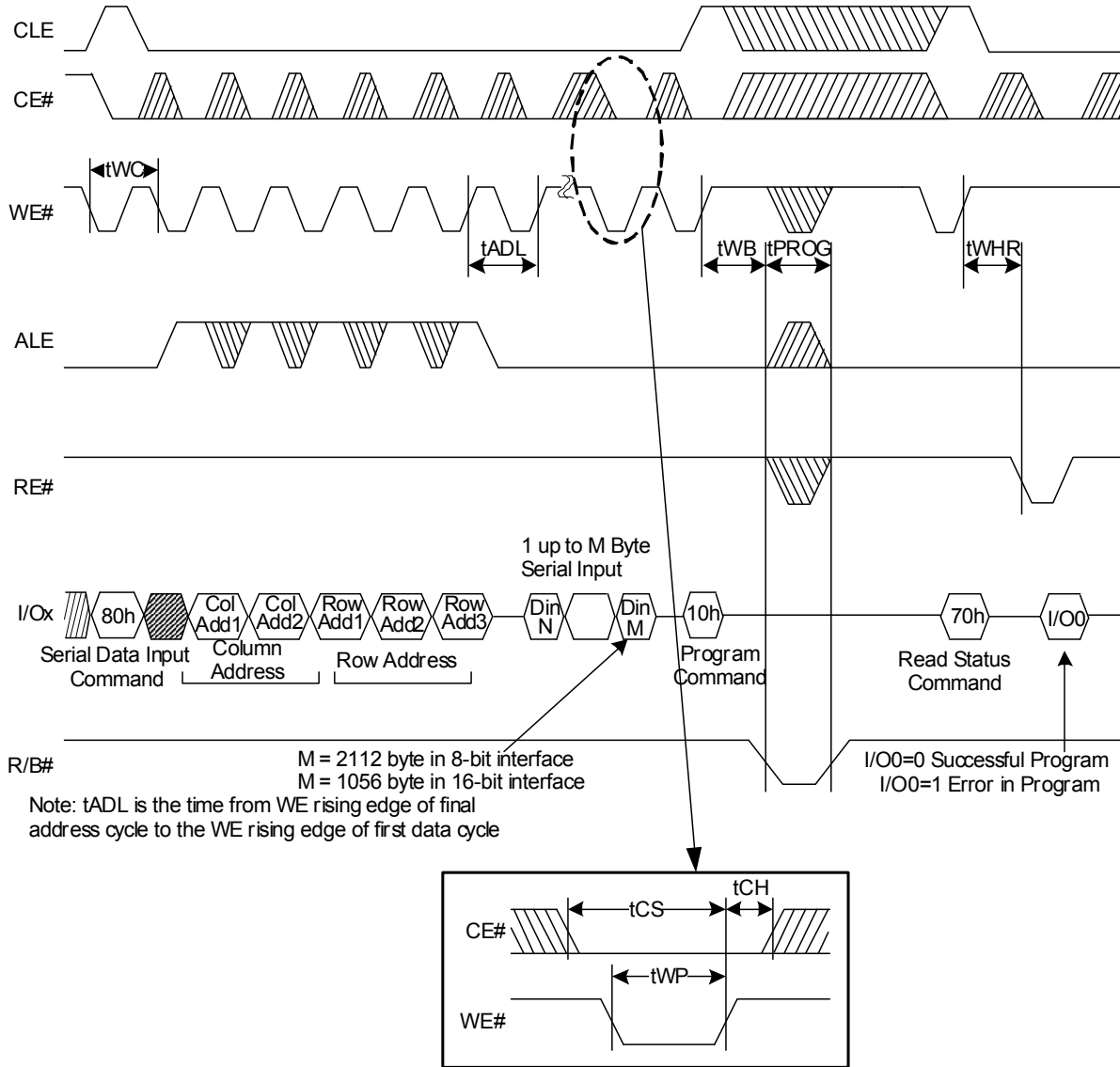


Figure 51. PNAND Mode SBD Page Program Operation (With CE# Don't Care)

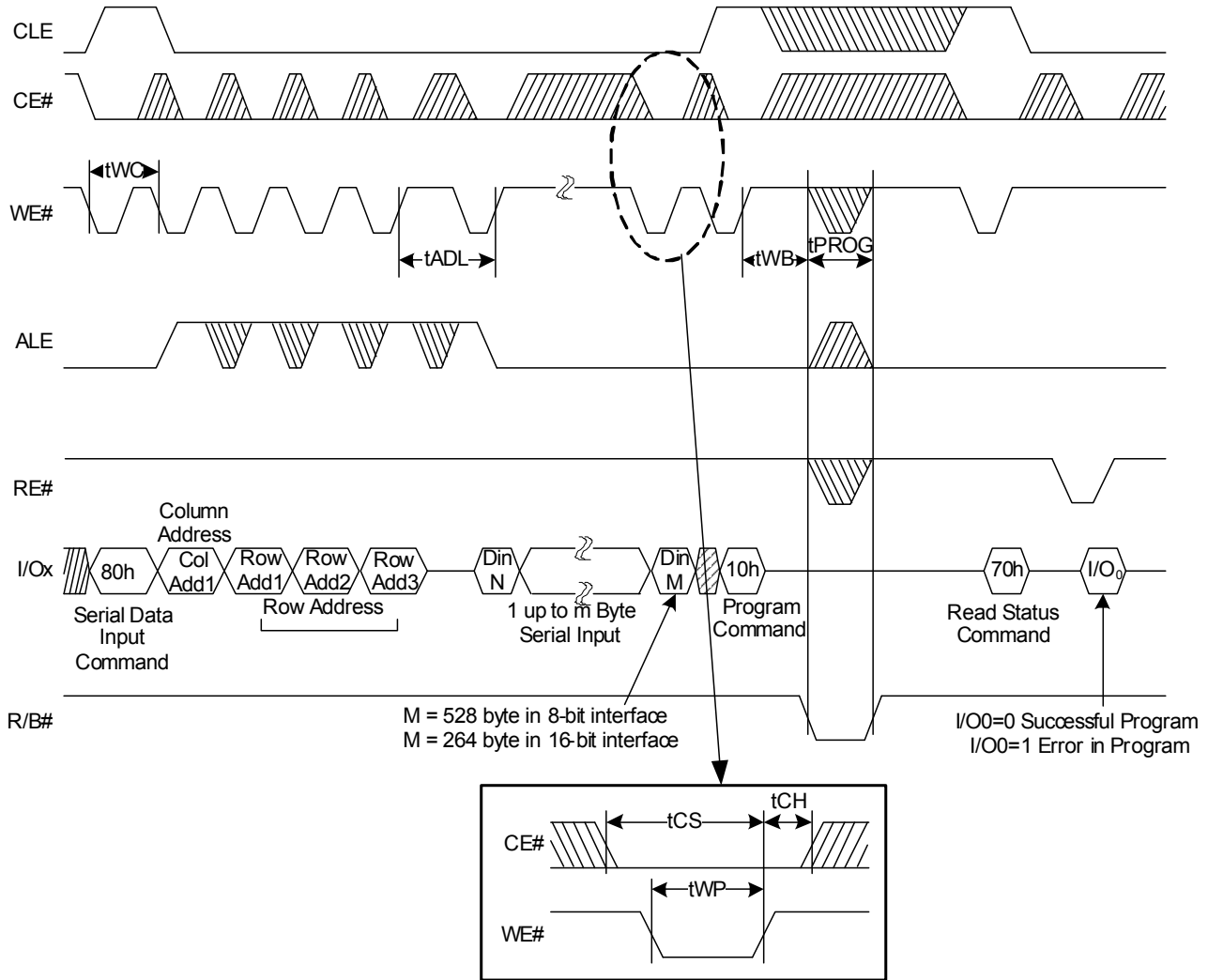


Figure 52. PNAND Mode Block Erase Operation

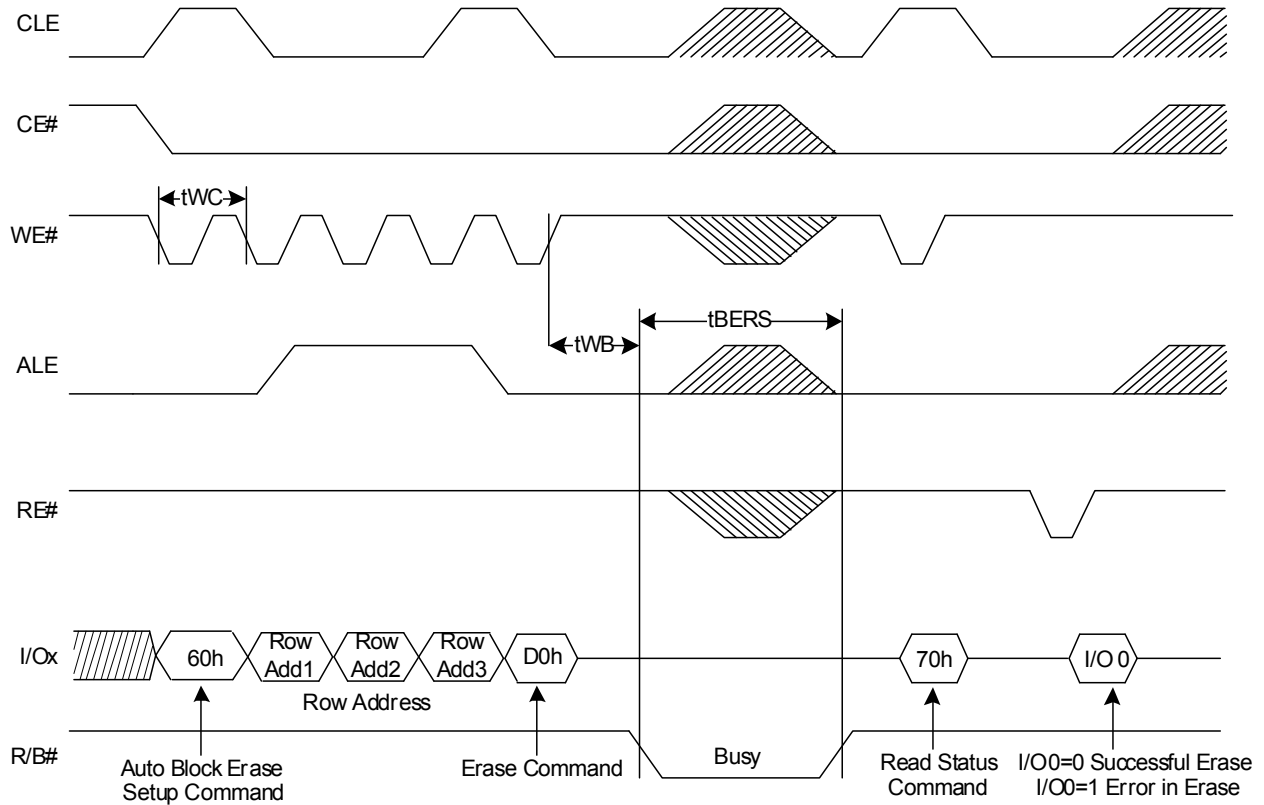
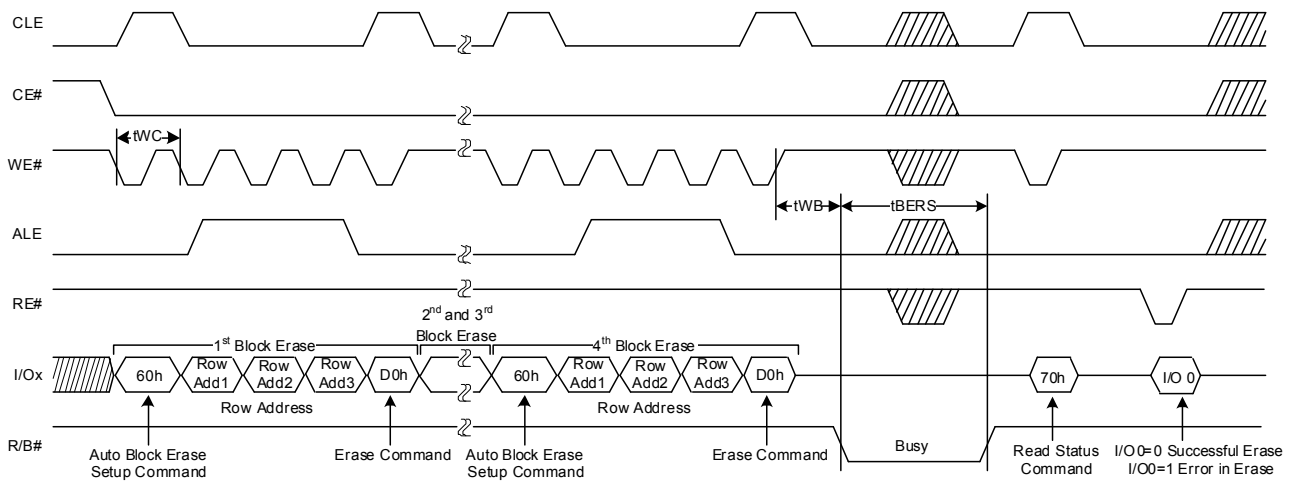


Figure 53. PNAND Mode Multi-Blocks (up to 4) Erase



Note: The multi-block erase can support up to 4 blocks erase

Figure 54. PNAND Mode Read ID Operation

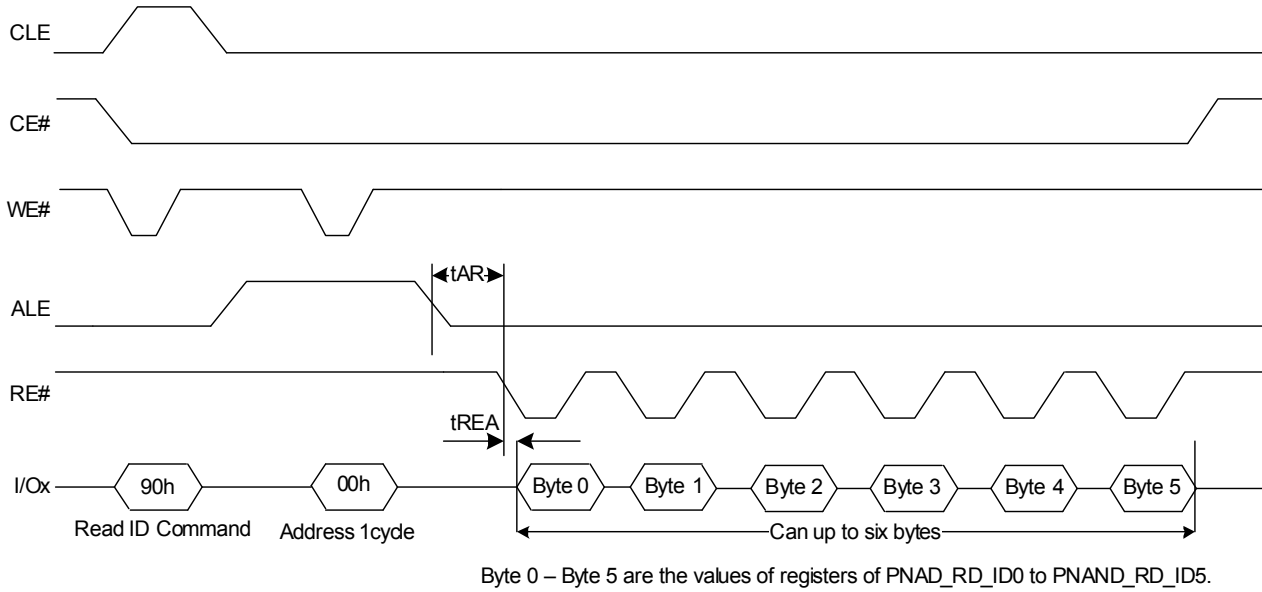


Figure 55. PNAND Mode Read ID2 Operation

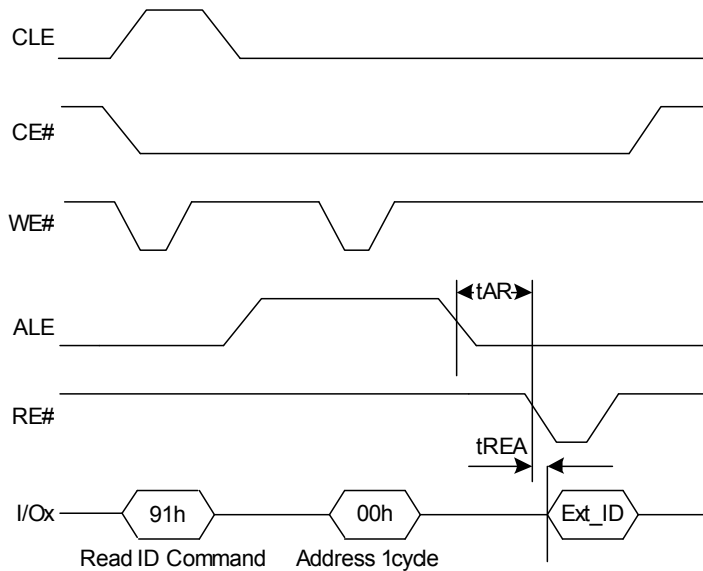
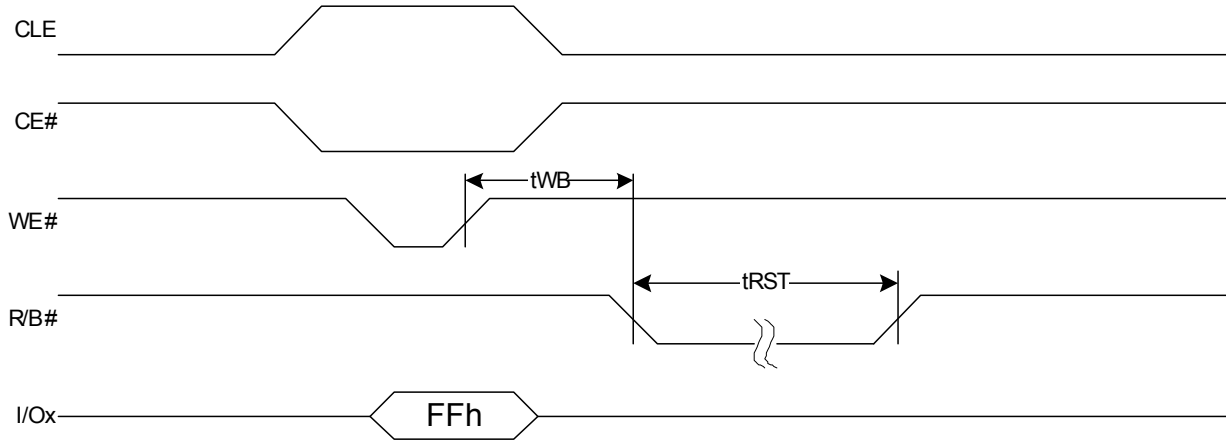


Figure 56. PNAND Mode Reset Operation

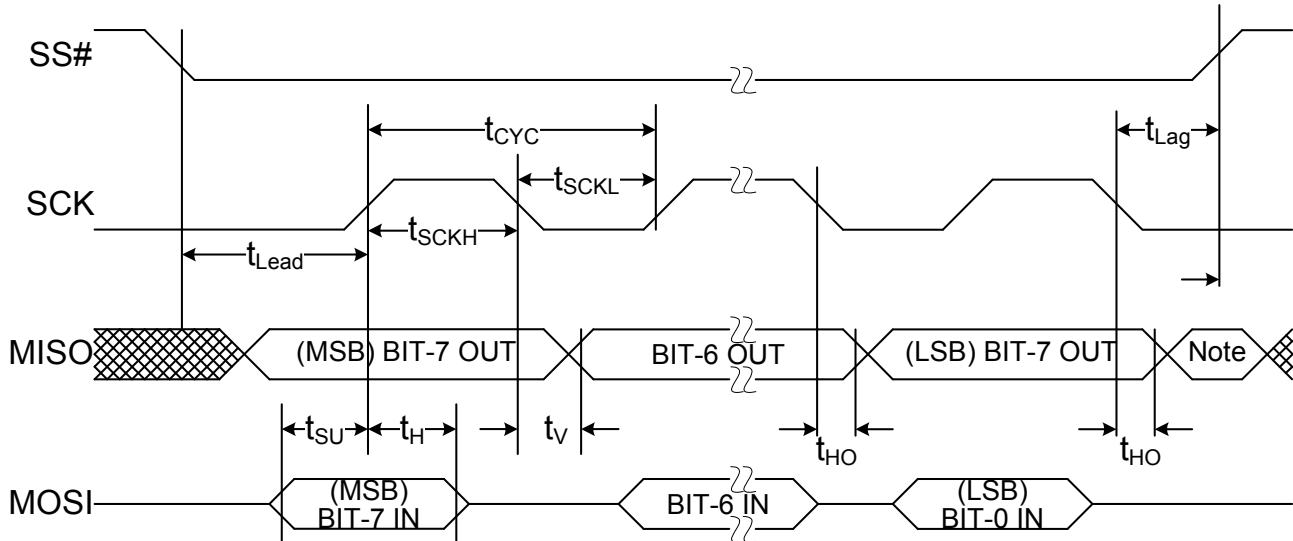


SPI and PI2C Interface

Table 23. SPI Mode Parameters

Parameter	Description	Min	Max	Units
f_{OP}	Operating frequency	0	26	MHz
t_{CYC}	Cycle time	38.5	–	ns
t_{Lead}	Enable lead time	19.23	–	ns
t_{Lag}	Enable lag time	19.23	–	ns
t_{SCKH}	Clock high time	17.33	–	ns
t_{SCKL}	Clock low time	17.33	–	ns
t_{SU}	Data setup time (inputs)	–	7	ns
t_H	Data hold time (inputs)	–	7	ns
t_V	Data valid time, after enable edge	–	18	ns
t_{HO}	Data hold time, after enable edge	0	–	ns

Figure 57. SPI Timing Diagram



Note: Not defined but normal MSB of character just received

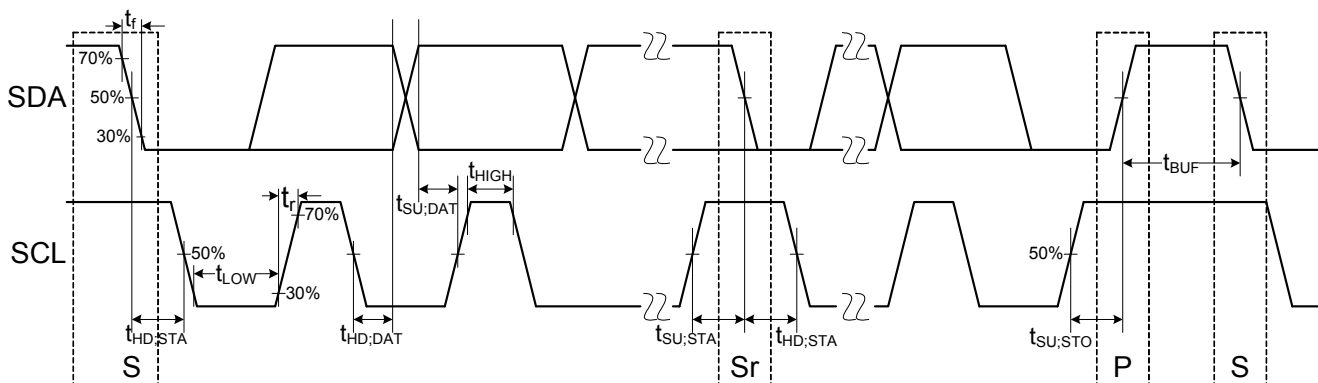
Table 24. I2C Interface Standard Mode Parameters

Parameter	Description	Min	Max	Units
F	Operating frequency	0	82	kHz
t _{BUF}	Bus free time (between stop and start conditions)	4.7	–	μs
t _{HD:STA}	Hold time after (Repeated) start condition. After this period the first clock is generated	4.0	–	μs
t _{SU:STA}	Repeated start condition setup time	4.7	–	μs
t _{SU:STO}	Stop condition setup time	4.0	–	μs
t _{HD:DAT}	Data hold time	0	–	ns
t _{SU:DAT}	Data setup time	250	–	ns
t _{TIMEOUT}	Detect clock low timeout	NA		ms
t _{LOW}	Clock low period	4.7	–	μs
t _{HIGH}	Clock high period	4.0	–	μs
t _{LOW:SEXT}	Cumulative clock low extend time (slave device)	NA		ms
t _r	Rise time	–	1000	ns
t _f	Fall time	–	300	ns

Table 25. I2C Interface Fast Mode Parameters

Parameter	Description	Min	Max	Units
F	Operating frequency	0	312	kHz
t _{BUF}	Bus free time (between stop and start condition)	1.3	–	μs
t _{HD:STA}	Hold time after (Repeated) start condition. After this period the first clock is generated	0.6	–	μs
t _{SU:STA}	Repeated start condition setup time	0.6	–	μs
t _{SU:STO}	Stop condition setup time	0.6	–	μs
t _{HD:DAT}	Data hold time	0	0.9	ns
t _{SU:DAT}	Data setup time	100	–	ns
t _{TIMEOUT}	Detect clock low timeout	NA		ms
t _{LOW}	Clock low period	1.3	–	μs
t _{HIGH}	Clock high period	0.6	–	μs
t _{LOW:SEXT}	Cumulative clock low extend time (slave device)	NA		ms
t _r	Rise time	–	300	ns
t _f	Fall time	–	300	ns

Figure 58. I2C Timing Diagram



Other P-Port Timings

DRQ# Min Pulse Width (tDPW): The minimum duration that DRQ# is deasserted following a DRQ acknowledgement (clear of DMAVAL) is 110 ns in Async mode or five P-Port clock (CLK) cycles in Sync mode.

Same Register Write-to-Read Holdoff (tWRHO): A read of a particular register must wait for a holdoff period following a write operation to that same register address to ensure that valid updated data is read. In Async mode, this holdoff time is 150 ns.

In Sync mode, this holdoff time is seven P-Port clock (CLK) cycles.

Register Update-to-Read Holdoff (tURHO): Same status registers are updated as side effect from accesses to other registers. For example, clearing the DMAVAL field automatically clears the associated endpoint buffer bit within the DRQ status register. A holdoff time must elapse from the first register access before the update is reflected in a subsequent read operation. This holdoff time is identical to the tWRHO.

S Port Interface AC Timing Parameters

SD/MMC/MMC+/CE-ATA Timing Parameters

For all conditions, SD/MMC data is driven and sampled on the rising edge of SD_CLK. Note that CE-ATA electrical and timing parameters are equivalent to MMC.

Figure 59. SD/MMC/CE-ATA Timing Waveform – All Modes

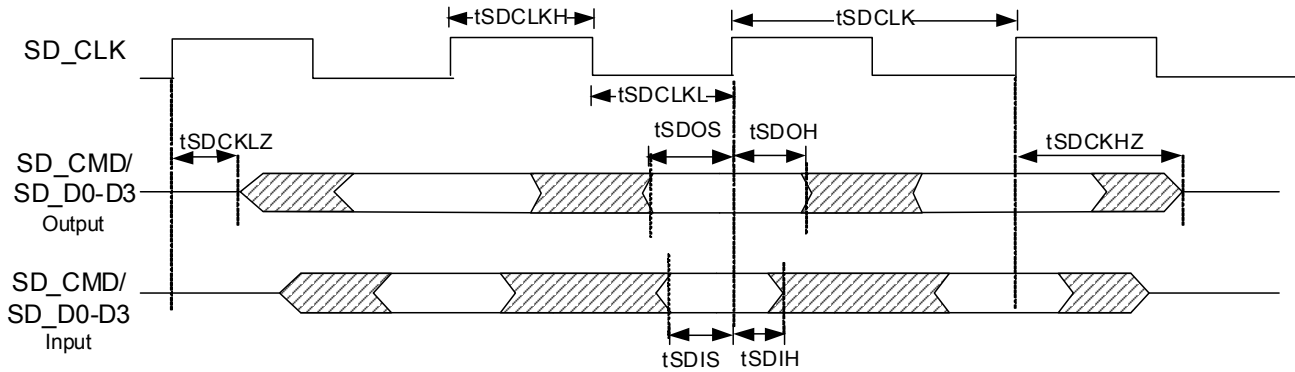


Table 26. Common Timing Parameters for SD/MMC/CE-ATA – During Identification Mode

Parameter	Description	Min	Max	Units
SDFREQ	SD_CLK interface clock frequency	0	400	kHz
tSDCLK	Clock period	2.5	–	μs
tSDCLKH	Clock high time	1.0	–	μs
tSDCLKL	Clock low time	1.0	–	μs

Table 27. Common Timing Parameters for SD/MMC/CE-ATA – During Data Transfer Mode

Parameter	Description	Min	Max	Units
SDFREQ	SD_CLK interface clock frequency	5	48	MHz
tSDCLK	Clock period	20.8	200	ns
tSDCLKOD	Clock duty cycle	40	60	%
tSCLKR	Clock rise time	–	3	ns
tSCLKF	Clock fall time	–	3	ns

Table 28. Timing Parameters for SD – All Modes

Parameter	Description	Min	Max	Units
tSDIS	Input setup time	4	–	ns
tSDIH	Input hold time	2.5	–	ns
tSDOS	Output setup time	7	–	ns
tSDOH	Output hold time	6	–	ns
tSDCKHZ	Clock to data High Z	–	18	ns
tSDCKLZ	Clock to data Low Z	3	–	ns

Table 29. Timing Parameters for MMC/CE-ATA – All Modes

Parameter	Description	Min	Max	Units
tSDIS	Input setup time	4	–	ns
tSDIH	Input hold time	4	–	ns
tSDOS	Output setup time	6	–	ns
tSDOH	Output hold time	6	–	ns
tSDCKHZ	Clock to data High Z	–	18	ns
tSDCKLZ	Clock to data Low Z	3	–	ns

Reset and Standby Timing Parameters

The Astoria reset mechanism and the standby mode are described in this section.

Sleep Time (tSLP): The maximum time from deassertion of WAKEUP to when Astoria enters low power state (sleep mode) is 1 ms.

Wakeup Time (tWU): The minimum time from assertion of WAKEUP pin (or initial power on with WAKEUP HIGH) to when any register operation is conducted is 1 ms if an external clock is present, or 5 ms if a crystal is used. The CY_AN_MEM_PWR_MAGT_STAT.WAKEUP field can only be polled after wakeup time following reset deassertion or WAKEUP assertion.

Minimum RESET# pulse width (tRPW): 5 ms when a crystal is used as clock or 1 ms when an external clock is used.

Minimum WAKEUP pulse width (tWPW): 5 ms.

Minimum HIGH on RESET# and WAKEUP (tRH, TWH): The WAKEUP and RESET# pins must be held HIGH for a minimum of 5 ms.

Reset Recovery Time (tRR): A minimum 1 ms reset recovery time must be allowed before Astoria registers can be accessed for read or write.

Figure 60. Reset and Standby Timing Diagram

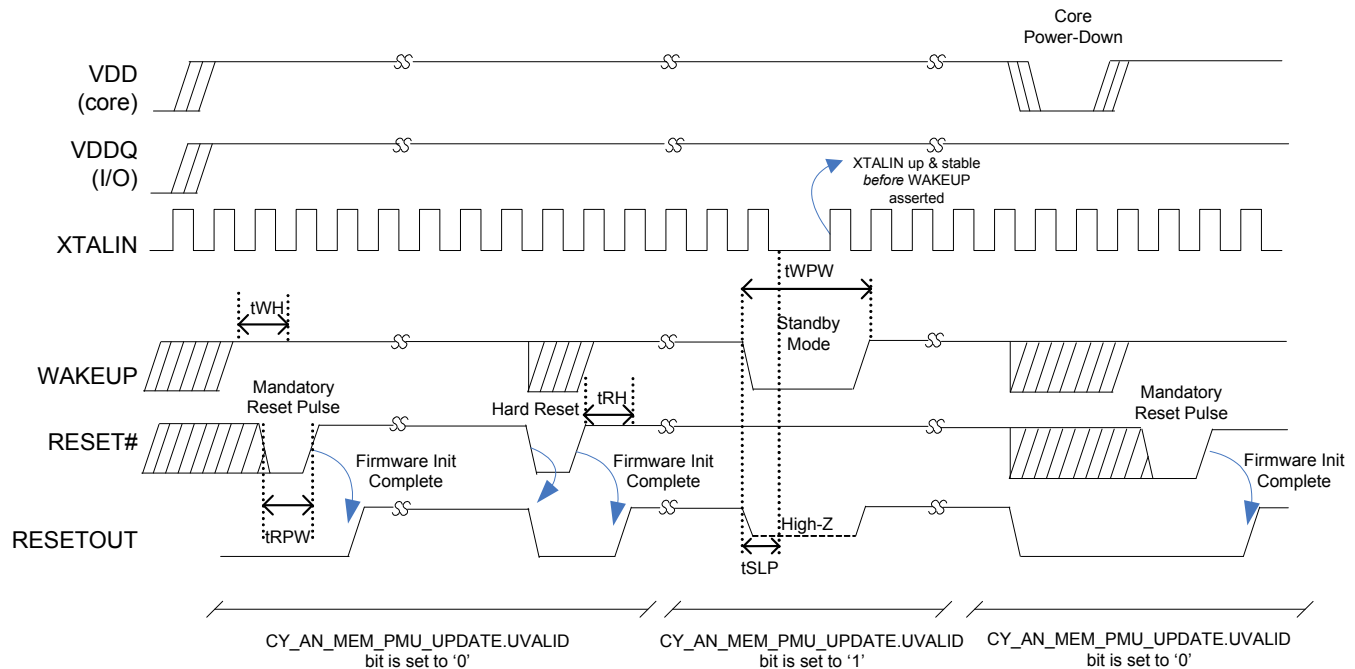
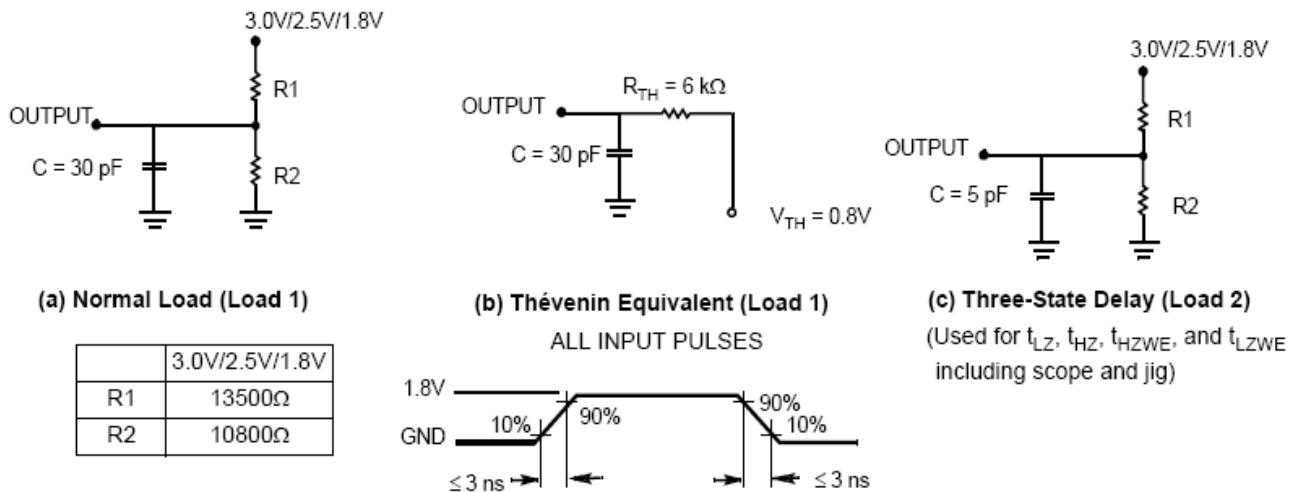


Table 30. Reset and Standby Timing Parameters

Parameter	Description	Conditions	Min	Max	Units
tSLP	Sleep time		–	1	ms
tWU	Wakeup time from standby mode	Clock on XTALIN	1	–	ms
		Crystal on XTALIN-XTALOUT	5	–	ms
tWH	WAKEUP high time		5	–	ms
tWPW	WAKEUP pulse width		5	–	ms
tRH	RESET# high time		5	–	ms
tRPW	RESET# pulse width	Clock on XTALIN	1	–	ms
		Crystal on XTALIN-XTALOUT	5	–	ms
tRP	RESET# recovery time		1	–	ms

Figure 61. AC Test Loads and Waveforms (Except SD and MMC, SD and MMC are comply with the SD/MMC specification)

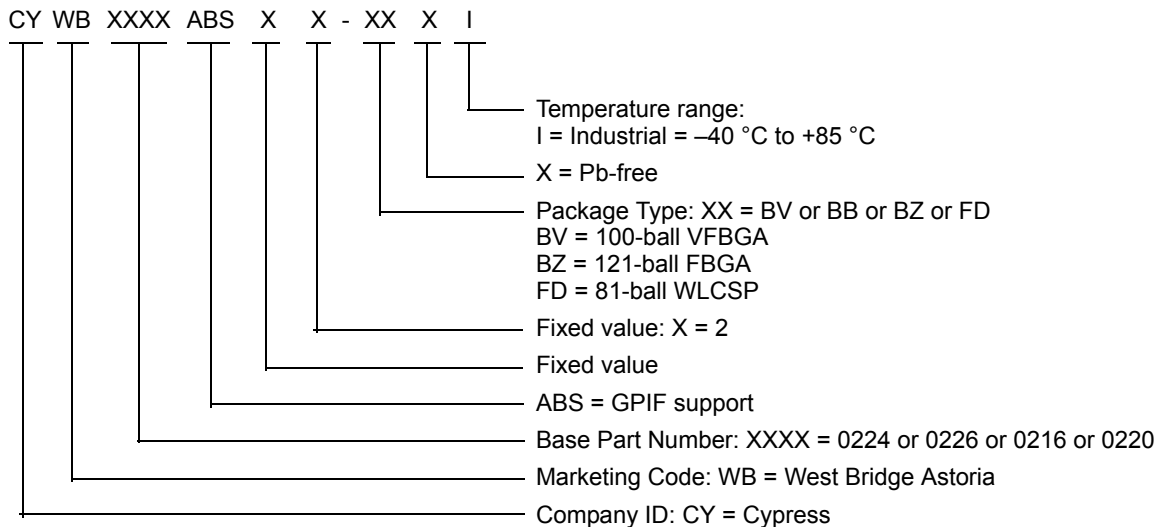


Ordering Information

Astoria provides many options with multiple ordering part numbers as shown in the following table:

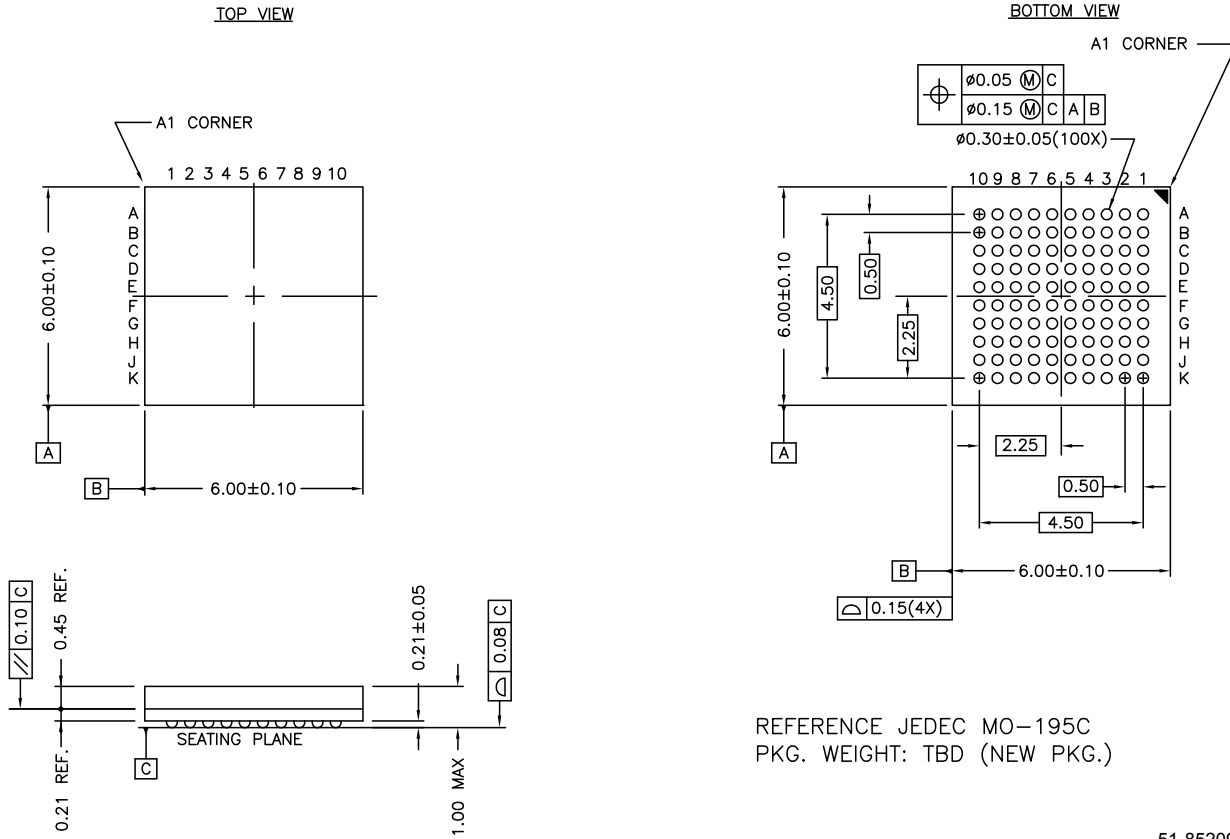
Ordering Code	Package Type	Optional Features			Clock Input Frequencies (MHz)	Status
		FlexBoot™	USB Switch	Turbo MTP		
CYWB0220ABSX2-FDXIT	81-ball WLCSP (Pb-free)		√		26	Sample
CYWB0224ABM-BVXIES	100-ball VFBGA (Pb-free)				19.2, 24, 26, 48	Sample
CYWB0224ABS-BZXI	121-ball FBGA (Pb-free)				19.2, 24, 26, 48	Production
CYWB0224ABS-BVXI	100-ball VFBGA (Pb-free)				19.2, 24, 26, 48	Production
CYWB0224ABS-BVXIT	100-ball VFBGA (Pb-free)				19.2, 24, 26, 48	Production
CYWB0224ABS-BVXIES	100-ball VFBGA (Pb-free)				19.2, 24, 26, 48	Sample
CYWB0224ABSX-FDXI	81-ball WLCSP (Pb-free)				19.2, 26	Sample
CYWB0224ABSX-FDXIT	81-ball WLCSP (Pb-free)				19.2, 26	Production
CYWB0226ABS-BVXI	100-ball VFBGA (Pb-free)		√		19.2, 24, 26, 48	Production
CYWB0226ABS-BVXIT	100-ball VFBGA (Pb-free)		√		19.2, 24, 26, 48	Production
CYWB0226ABSX-FDXI	81-ball WLCSP (Pb-free)		√		19.2, 26	Sample
CYWB0226ABSX-FDXIT	81-ball WLCSP (Pb-free)		√		19.2, 26	Production

Ordering Code Definitions



Package Diagram

Figure 62. 100-ball VFBGA (6 × 6 × 1.0 mm) BZ100 Package Outline, 51-85209

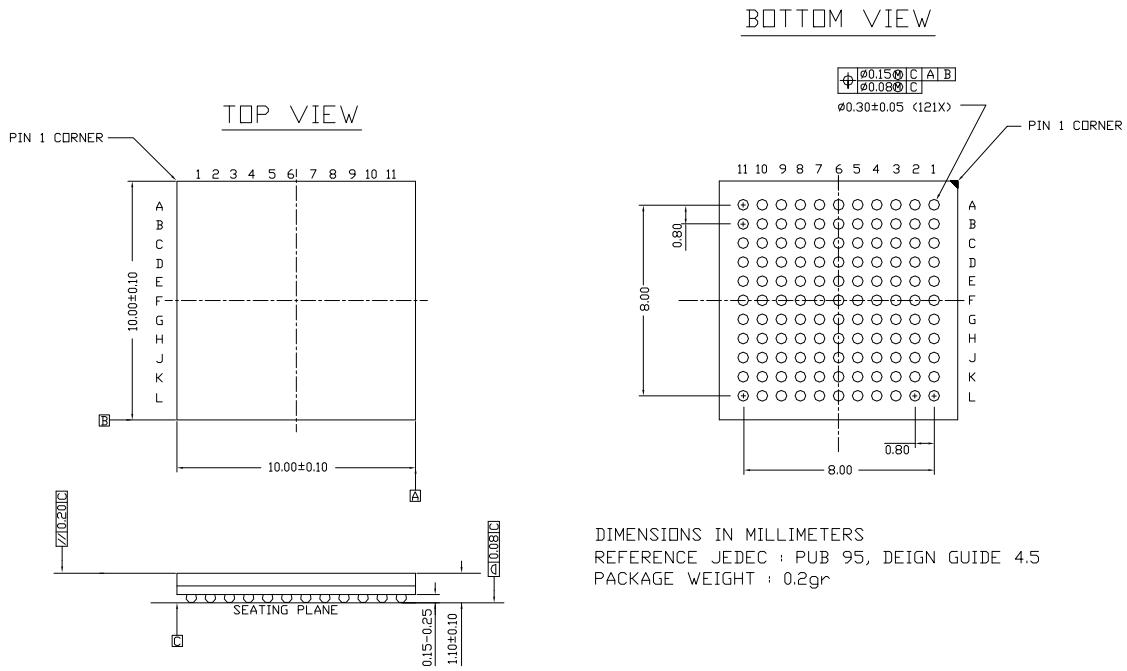


REFERENCE JEDEC MO-195C
 PKG. WEIGHT: TBD (NEW PKG.)

51-85209 *D

100-ball VFBGA Package Outline Number	Revision	Date Released
51-85209	*D	02/07/2011

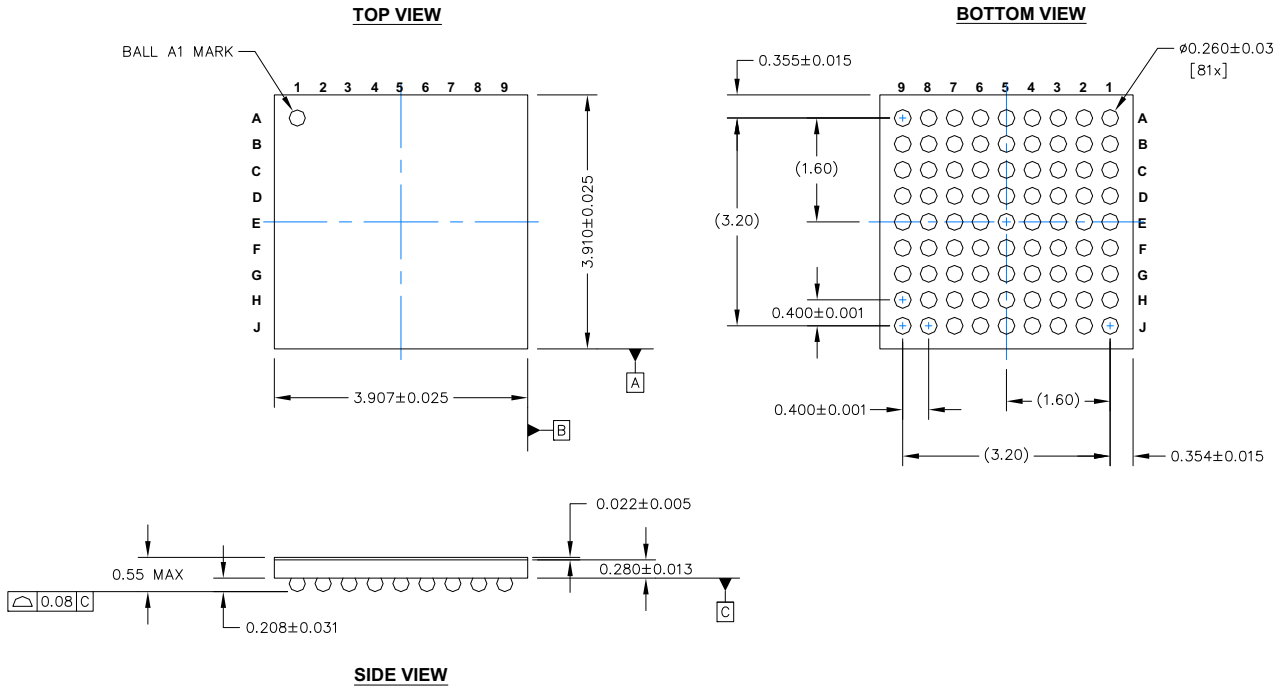
Figure 63. 121-ball FBGA (10 × 10 × 1.20 mm) (0.30 Ball Diameter) Package Outline, 001-54471



001-54471 *C

121-ball FBGA Package Outline Number	Revision	Date Released
001-54471	*C	05/30/2011

Figure 64. Astoria WLCSP (3.91 × 3.91 × 0.55 mm) FN81B Package Outline, 001-45618



NOTES:

1. ALL DIMENSION ARE IN MM
2. PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress Web
3. JEDEC – Publication 95; Design Guide 4.18

001-45618 *C

Astoria WLCSP Package Outline Number	Revision	Date Released
001-45618	*C	02/23/2012

Acronyms

Acronym	Description
CRAM	cellular random access memory
DMA	direct memory access
ECC	error correction code
GPIF	General purpose Interface
MMC	multimedia card
MTP	media transfer protocol
PLL	phase-locked loop
SD	secure digital
SD	secure digital
SDIO	secure digital input / output
SLC	single-level cell
SPI	serial peripheral interface
USB	universal serial bus
VFBGA	very fine ball grid array
WLCSP	wafer level chip scale package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
μA	microampere
μs	microsecond
mA	milliampere
Mbps	mega bytes per second
MHz	megahertz
ms	millisecond
ns	nanosecond
Ω	ohm
pF	picofarad
V	volt

Document History Page

Document Title: CYWB022XX Family, West Bridge [®] : Astoria™ USB and Mass Storage Peripheral Controller				
Document Number: 001-13805				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	866960	VSO / PSZ	See ECN	New datasheet
*A	2208371	JYEE / VSO	See ECN	<p>1) Corrected the Pin name (R/B#) in Table 2, Updated I_{SB1} to I_{SB3} in Table 3, Updated Table 5, Updated Figure 14 to Figure 18 (timing diagrams), In Table 6, moved "Interface Bandwidth" to first row, Updated Table 7, Updated Figure 22, Added Figure 23 (new), Updated Figure 24 to 26, Updated Table 8, Updated Figure 27, Added Table 9 (Async SRAM mode Timing), Updated Figure 29 - 31, Updated Table 10, Updated Figure 32 - 43, Updated Table 11, Updated Table 12, Updated Figure 45, Updated Table 14, Added Table 16, and 21. Updated Figure 47.</p> <p>2) Added two part numbers (CYWB0226ABS and CYWB0226ABM) in the title, Modified Feature list (same as Astoria Advance Information), Updated Features to include "Integrated USB Switch", Updated Figure 1, Updated USB Interface (U-Port), Added Figure 2, Updated section 3.6, Updated Table 2, Updated Figure 14, Added Table 4, Updated Table 5-6, Updated Figure 15-19, Updated Table 7, Updated Figure 20-21, Updated Table 8, Updated Figure 22-27, Updated Table 9, Update Figure 28-29, Updated Table 10, Updated Figure 30-32, Updated Table 11, Updated Figure 33-54, Updated Table 12, Updated Figure 55, Updated Table 13-14, Updated Figure 56-58, Updated Table 15-16, Added Table 17-18, Updated Table 19, Updated Figure 59, and Added two part numbers (CYWB0226ABS and CYWB0226ABM) in the order information (section 9).</p>
*B	2503171	VSO / AESA	See ECN	<p>1. "Features" - added 3.91x3.91 mm 81-ball WLCSP to Small footprint bullet.</p> <p>2. "Processor Interface (P-Port)" - added "The P-Port of the WLCSP package only supports PNAND and SPI interface" and "The 81-ball WLCSP package only supports interrupt."</p> <p>3. "Clocking" - added "The 81-ball WLCSP only supports 19.2 and 26 MHz external clock input." and Tables 1 and 2</p> <p>4. Table 4 - added the column of "Ball #"</p> <p>5. Table 5 - added a new table for WLCSP pin assignment</p> <p>6. Figure 13 - removed the grid line</p> <p>7. Figure 14 - new ball map for WLCSP package</p> <p>8. Table 14 - add 33ns for t_{RC} and t_{WC} timing for WLCSP package</p> <p>9. Figure 55 - updated the SPI timing diagram</p> <p>10. "Ordering Information" - added WLCSP package ordering code to the table</p> <p>11. Add CYWB0224ABSX, CYWB0224ABMX CYWB0226ABSX, CYWB0226ABMX.</p>
*C	2521024	VSO / AESA	See ECN	<p>1. This version is final - Removed status "Preliminary"</p> <p>2. Update the section of "Core Power Down Mode"</p> <p>3. Note 3 of Table 6 has added the requirement of SSVDDQ and SNVDDQ in SD/MMC modes</p> <p>4. SNVDDQ in Table 6 added Note 3</p> <p>5. Table 17, add parameter t_{WH}</p> <p>6. Figure 22 and Figure 27 have been updated</p> <p>7. Table 18, add parameter t_{AVH}</p> <p>8. Figure 28 and Figure 29 have been updated</p> <p>9. Table 20, the value of parameters "t_{PROG}" and "t_R" have been updated</p> <p>10. Table 23, removed parameter of "t_A"</p> <p>11. Figure 58 I2C timing diagram has been updated</p>

Document History Page (continued)

Document Title: CYWB022XX Family, West Bridge®: Astoria™ USB and Mass Storage Peripheral Controller Document Number: 001-13805				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*D	2663942	VSO / AESA	02/24/2009	1. Feature list - add (SP and Lite SP) to WLCSP 2. Update the section of "Clocking" (add description of "SP" and "Lite SP") 3. Add Table 3 4. Add section of "Packages and Interface Options" 5. Add Table 5 6. Add "SP" to the title of Table 7 7. Add Table 8 (pin assignment for Lite SP) 8. Figure 14, change the color of AVDDQ 9. Add Figure 15 for Lite SP ball map 10. Remove some of note [2] in table 6. 11. Update the description of Note [2] 12. Update the table in "Order Information" section.
*E	2905597	VSO	04/05/2010	Removed part CYWB0224ABM-BVXI. Updated package diagrams.
*F	2920278	VSO / AESA	04/21/2010	Added I _{SB1} parameter in DC Specifications for All Voltage Supplies (Except USB Switch) . Added Contents Updated links in Sales, Solutions, and Legal Information .
*G	2954592	ESH	06/17/10	Removed inactive parts from the ordering information table
*H	3057588	ODC	10/13/2010	Removed references to MLC NAND flash. Removed MLC NAND parts from Ordering Information . Added Ordering Code Definitions .
*I	3164752	ANOP	02/07/2011	In 'D3' row in Table 8, added '#' to DACK in the 'SRAM Interface', 'ADM' and 'PNAND' columns. In 'D4' row in Table 8, added '#' to DRQ in the 'SRAM Interface', 'ADM' and 'PNAND' columns.
*J	3191625	ANOP	03/09/2011	Added Table 18 (Page-read command sequence for large-block devices) and Figure 40 (LBD mode address cycles) Added Table 19 (Page-read command sequence for small-block devices) and Figure 42 (SBD mode address cycles) Updated Package Diagram .
*K	3465771	SIRK	12/22/2011	Changed status from Confidential to Final. Updated Mass Storage Support (S-Port) . Updated Pin Assignments . Updated Package Diagram .
*L	3539318	SIRK	03/01/2012	Updated Package Diagram (001-45618 from Rev *B to *C). Moving document to external web.
*M	3665980	AASI	07/06/2012	Updated Features (Removed 100-ball BGA package related information). Updated Ordering Information (Updated part numbers). Updated Package Diagram (Removed 100-ball BGA package related information (spec 51-85107)).

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