# AM186ED, ‘EDLV

## *High Performance 16-Bit Embedded Microcontrollers*

The AM186ED/EDLV microcontrollers are part of the AMD E86 family of embedded microcontrollers and microprocessors based on the x86 architecture. The AM186ED/EDLV microcontrollers are the ideal upgrade for 80C186/188 designs requiring 80C186/188 compatibility, increased performance, serial communications, a direct bus interface, and more than 64K of memory.

The AM186ED/EDLV microcontrollers have been designed to meet the most common requirements of embedded products developed for the communications, office automation, mass storage, and general embedded markets. Specific applications include PBXs, multiplexers, modems, disk drives, hand-held and desktop terminals, fax machines, printers, photocopiers, and industrial controls.

### Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

### Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer’s datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. ‘Typical’ values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

PRELIMINARY

AMD

# Am186™ED/EDLV

## High Performance, 80C186- and 80C188-Compatible, 16-Bit Embedded Microcontrollers

## DISTINCTIVE CHARACTERISTICS

- **E86™ family 80C186- and 80C188-compatible microcontroller with enhanced bus interface**
  - Lower system cost with higher performance
  - 3.3-V ± 0.3-V operation (Am186EDLV microcontrollers)
- **Programmable DRAM Controller**
  - Supports zero-wait-state operation with 50-ns DRAM at 40 MHz, 60-ns @ 33 MHz, 70-ns @ 25 MHz
  - Includes programmable $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh capability
- **High performance**
  - 20-, 25-, 33-, and 40-MHz operating frequencies
  - Zero-wait-state operation at 40 MHz with 70-ns static memory
  - 1-Mbyte memory address space
  - 64-Kbyte I/O space
- **Enhanced features provide improved memory access and remove the requirement for a 2x clock input**
  - Nonmultiplexed address bus
  - Processor operates at the clock input frequency
  - 8-bit or 16-bit programmable bus sizing including 8-bit boot option
- **Enhanced integrated peripherals**
  - 32 programmable I/O (PIO) pins
  - Two full-featured asynchronous serial ports allow full-duplex, 7-bit, 8-bit, or 9-bit data transfers
  - Serial port hardware handshaking with $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{ENRX}}$, and $\overline{\text{RTR}}$ selectable for each port
  - Improved serial port operation enhances 9-bit DMA support
  - Independent serial port baud rate generators
  - DMA to and from the serial ports
  - Watchdog timer can generate NMI or reset
  - A pulse-width demodulation option
  - A data strobe, true asynchronous bus interface option included for $\overline{\text{DEN}}$
  - Reset configuration register
- **Familiar 80C186 peripherals**
  - Two independent DMA channels
  - Programmable interrupt controller with up to 8 external and 8 internal interrupts
  - Three programmable 16-bit timers
  - Programmable memory and peripheral chip-select logic
  - Programmable wait state generator
  - Power-save clock divider
- **Software-compatible with the 80C186 and 80C188 microcontrollers with widely available native development tools, applications, and system software**
- **A compatible evolution of the Am186EM, Am186ES, and Am186ER microcontrollers**
- **Available in the following packages:**
  - 100-pin, thin quad flat pack (TQFP)
  - 100-pin, plastic quad flat pack (PQFP)

## GENERAL DESCRIPTION

The Am186™ED/EDLV microcontrollers are part of the AMD E86™ family of embedded microcontrollers and microprocessors based on the x86 architecture. The Am186ED/EDLV microcontrollers are the ideal upgrade for 80C186/188 designs requiring 80C186/188 compatibility, increased performance, serial communications, a direct bus interface, and more than 64K of memory.

The Am186ED/EDLV microcontrollers integrate a complete DRAM controller to take advantage of low DRAM costs. This reduces memory subsystem costs while maintaining SRAM performance.The Am186ED/EDLV microcontrollers also integrate the functions of a CPU, nonmultiplexed address bus, three timers, watchdog timer, chip selects, interrupt controller, two DMA controllers, two asynchronous serial ports, programmable bus sizing, and programmable I/O (PIO) pins on one chip. Compared to the 80C186/188 microcontrollers, the Am186ED/EDLV microcontrollers enable designers to reduce the size, power consumption, and cost of embedded systems, while increasing reliability, functionality, and performance.

The Am186ED/EDLV microcontrollers have been designed to meet the most common requirements of embedded products developed for the communications, office automation, mass storage, and general embedded markets. Specific applications include PBXs, multiplexers, modems, disk drives, hand-held and desktop terminals, fax machines, printers, photocopiers, and industrial controls.



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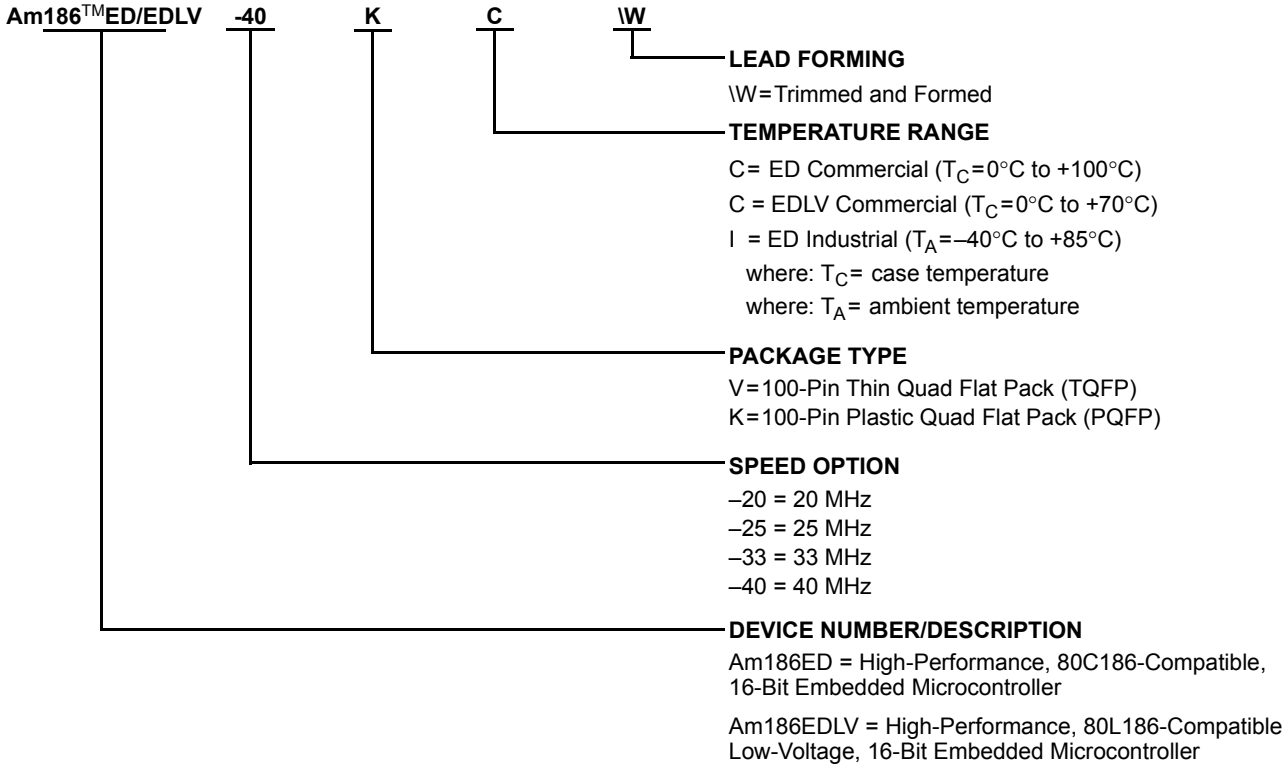
Issue Date: **May 1997**

# ORDERING INFORMATION

## Standard Products

AMD standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the elements below.




| Valid Combinations | |
|---|---|
| Am186ED–20<br>Am186ED–25<br>Am186ED–33<br>Am186ED–40 | VC\W or<br>KC\W |
| Am186ED–20<br>Am186ED–25 | KI\W[1] |
| Am186EDLV–20<br>Am186EDLV–25 | VC\W or<br>KC\W |

***Note:***
*The industrial version of the Am186ED is offered only in the PQFP package.*

**Valid Combinations**

Valid combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

***Note:*** *The industrial version of the Am186ED as well as the Am186EDLV are available in 20 and 25 MHz operating frequencies only.*

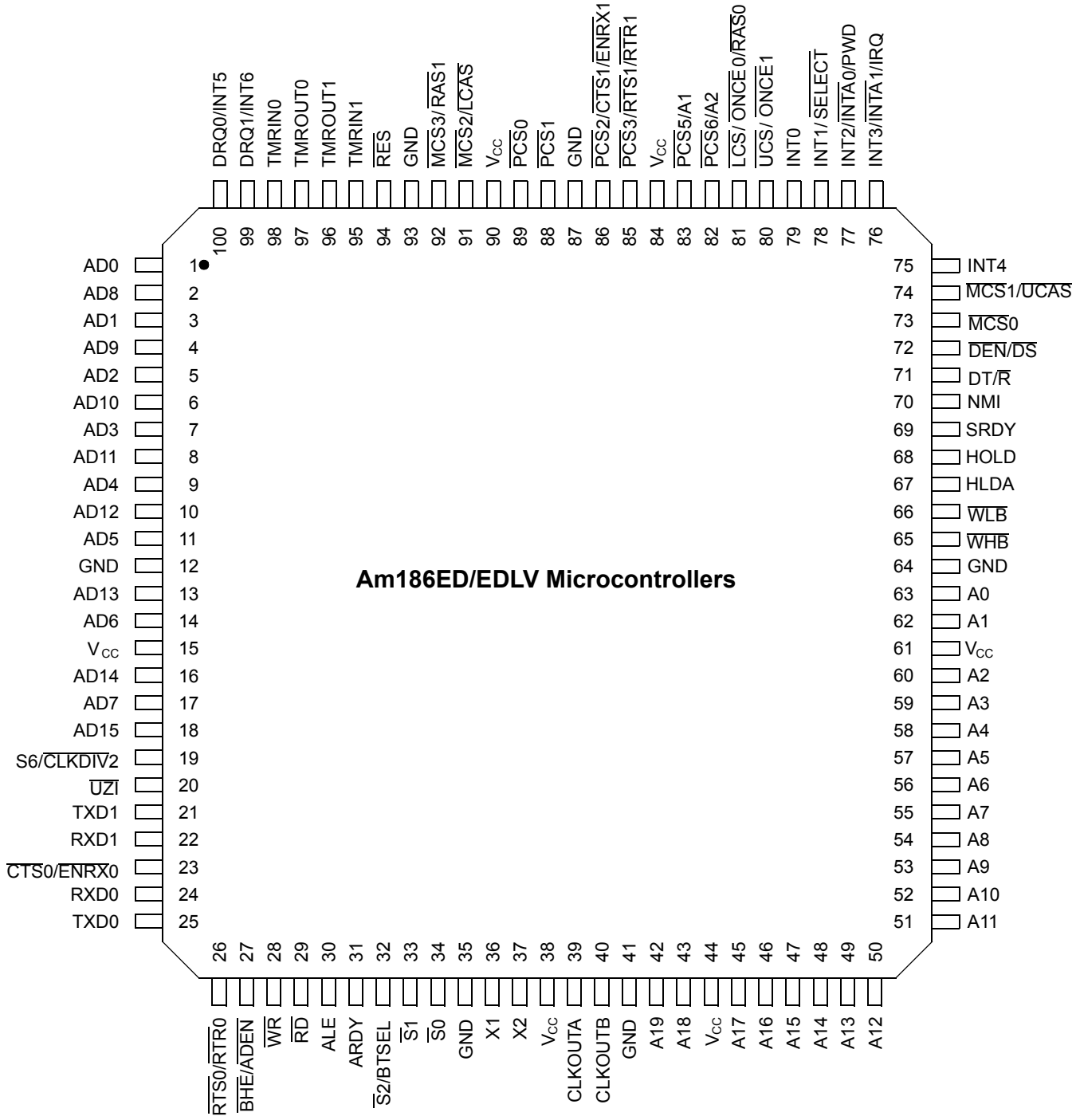
*The Am186ED and Am186EDLV microcontrollers are all functionally the same except for their DC characteristics and available frequencies.*

***Note:*** *There is no 188 version of the Am186ED/EDLV. The same 8-bit external bus capabilities can be achieved using the 8-bit boot capability and programmable bus sizing options.*

## TQFP CONNECTION DIAGRAMS AND PINOUTS

### Am186ED/EDLV Microcontrollers

### Top Side View—100-Pin Thin Quad Flat Pack (TQFP)

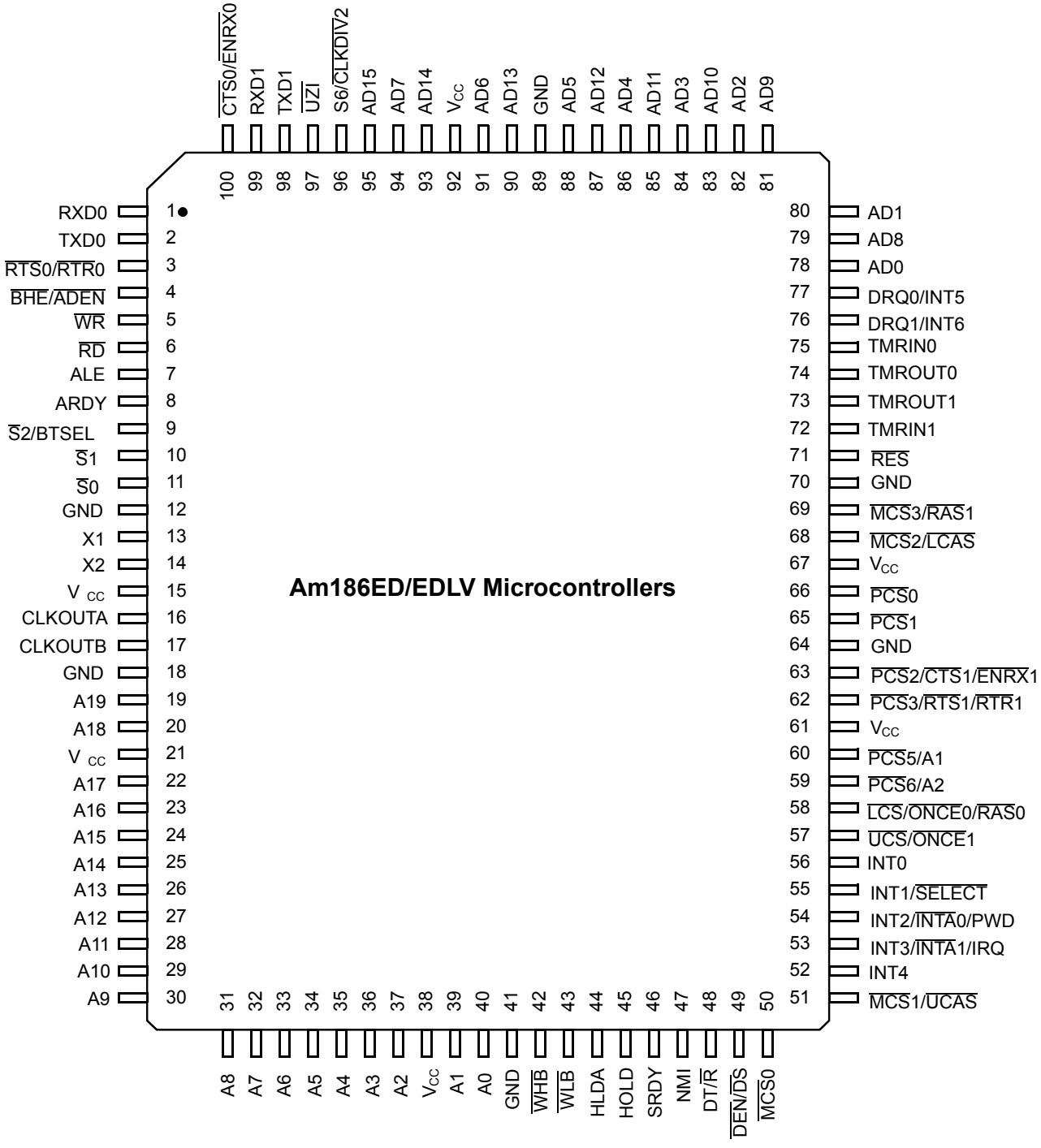



***Note:***
*Pin 1 is marked for orientation.*

## PQFP CONNECTION DIAGRAMS AND PINOUTS

### Am186ED/EDLV Microcontrollers

### Top Side View—100-Pin Plastic Quad Flat Pack (PQFP)




***Note:***
*Pin 1 is marked for orientation.*

## ABSOLUTE MAXIMUM RATINGS

**Storage temperature**

Am186ED.....–65°C to +125°C
Am186EDLV.....–65°C to +125°C

**Voltage on any pin with respect to ground**

Am186ED.....–0.5 V to $V_{cc}$ +0.5 V
Am186EDLV.....–0.5 V to $V_{cc}$ +0.5 V

***Note:*** *Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

**Am186ED Microcontroller**

Commercial ($T_C$).....0°C to +100°C
Industrial* ($T_A$).....–40°C to +85°C
Supply voltage ($V_{CC}$) .....5 V ± 10%

**Am186EDLV Microcontroller**

Commercial ($T_A$) ..... 0°C to +70°C
$V_{CC}$ up to 25 MHz..... 3.3 V ± 0.3 V

Where: $T_C$ = case temperature
$T_A$ = ambient temperature

**Industrial versions of Am186ED microcontrollers are available in 20 and 25 MHz operating frequencies only.*

## DC CHARACTERISTICS OVER COMMERCIAL AND INDUSTRIAL OPERATING RANGES

| Symbol | Parameter Description | Test Conditions | Preliminary Min | Preliminary Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage (Except X1) | | –0.5 | $0.2V_{CC}$ –0.3 | V |
| $V_{IL1}$ | Clock Input Low Voltage (X1) | | –0.5 | 0.8 | V |
| $V_{IH}$ | Input High Voltage (Except $\overline{RES}$ and X1) | | 2.0 | $V_{CC}$ +0.5 | V |
| $V_{IH1}$ | Input High Voltage ($\overline{RES}$) | | 2.4 | $V_{CC}$ +0.5 | V |
| $V_{IH2}$ | Clock Input High Voltage (X1) | | $V_{CC}$ –0.8 | $V_{CC}$ +0.5 | V |
| $V_{OL}$ | **Output Low Voltage** | | | | |
| | Am186ED | $I_{OL}$= 2.5 mA ($\overline{S2}$–$\overline{S0}$)<br>$I_{OL}$= 2.0 mA (others) | | 0.45 | V |
| | Am186EDLV | $I_{OL}$= 1.5 mA ($\overline{S2}$–$\overline{S0}$)<br>$I_{OL}$= 1.0 mA (others) | | 0.45 | V |
| $V_{OH}$ | **Output High Voltage**[a] | | | | |
| | Am186ED | $I_{OH}$= –2.4 mA @ 2.4 V | 2.4 | $V_{CC}$ +0.5 | V |
| | | $I_{OH}$= –200 µA @ $V_{CC}$–0.5 | $V_{CC}$ –0.5 | $V_{CC}$ | V |
| | Am186EDLV | $I_{OH}$= –200 µA @ $V_{CC}$–0.5 | $V_{CC}$ –0.5 | $V_{CC}$ | V |
| $I_{CC}$ | Power Supply Current @ 0°C | $V_{CC}$ = 5.5 V [b]<br>$V_{CC}$ = 3.6 V [b] | | 5.9<br>4.0 | mA/MHz |
| $I_{LI}$ | Input Leakage Current @ 0.5 MHz | 0.45 V≤$V_{IN}$≤$V_{CC}$ | | ±10 | µA |
| $I_{LO}$ | Output Leakage Current @ 0.5 MHz | 0.45 V≤$V_{OUT}$≤$V_{CC}$ [c] | | ±10 | µA |
| $V_{CLO}$ | Clock Output Low | $I_{CLO}$= 4.0 mA | | 0.45 | V |
| $V_{CHO}$ | Clock Output High | $I_{CHO}$= –500 µA | $V_{CC}$ –0.5 | | V |

***Notes:***

*a The $\overline{LCS}$/$\overline{ONCE0}$/$\overline{RAS0}$ and $\overline{UCS}$/$\overline{ONCE1}$ pins have weak internal pullup resistors. Loading the $\overline{LCS}$/$\overline{ONCE0}$/$\overline{RAS0}$ and $\overline{UCS}$/$\overline{ONCE1}$ pins in excess of $I_{OH}$ = –200 µA during reset can cause the device to go into ONCE mode.*

*b Current is measured with the device in RESET with X1 and X2 driven and all other non-power pins open but held High or Low.*

*c Testing is performed with the pins floating, either during HOLD or by invoking the ONCE mode.*

## CAPACITANCE

| Symbol | Parameter Description | Test Conditions | Preliminary | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| $C_{IN}$ | Input Capacitance | @ 1 MHz | | 10 | pF |
| $C_{IO}$ | Output or I/O Capacitance | @ 1 MHz | | 20 | pF |

***Note:***
*Capacitance limits are guaranteed by characterization.*

## POWER SUPPLY CURRENT

For the following typical system specification shown in Figure 11, $I_{CC}$ has been measured at 4.0 mA per MHz of system clock. For the following typical system specification shown in Figure 12, $I_{CC}$ has been measured at 5.9 mA per MHz of system clock. The typical system is measured while the system is executing code in a typical application with nominal voltage and maximum case temperature. Actual power supply current is dependent on system design and may be greater or less than the typical $I_{CC}$ figure presented here.

Typical current in Figure 11 is given by:

$I_{CC} = 4.0\ mA \cdot freq(MHz)$

Typical current in Figure 12 is given by:

$I_{CC} = 5.9\ mA \cdot freq(MHz)$

Please note that dynamic $I_{CC}$ measurements are dependent upon chip activity, operating frequency, output buffer logic, and capacitive/resistive loading of the outputs. For these $I_{CC}$ measurements, the devices were set to the following modes:

- No DC loads on the output buffers
- Output capacitive load set to 35 pF
- AD bus set to data only
- PIOs are disabled
- Timer, serial port, refresh, and DMA are enabled

Table 10 shows the variables that are used to calculate the typical power consumption value for the Am186EDLV microcontroller.

**Table 10. Typical Power Consumption Calculation for the Am186EDLV Microcontroller**

| MHz · $I_{CC}$ · Volts / 1000 = P | | | Typical Power in Watts |
|---|---|---|---|
| MHz | Typical $I_{CC}$ | Volts | |
| 20 | 4.0 | 3.6 | 0.288 |
| 25 | 4.0 | 3.6 | 0.360 |

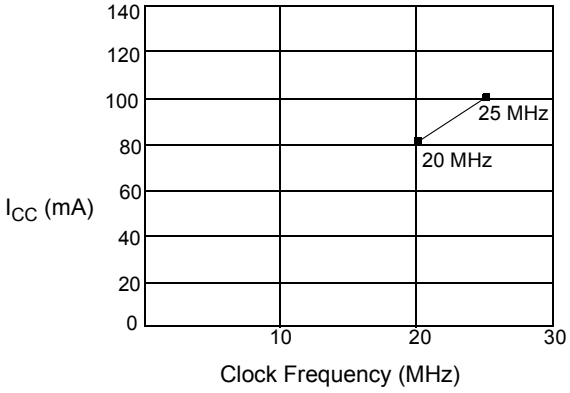



**Figure 11. Typical $I_{cc}$ Versus Frequency for Am186EDLV Microcontroller**

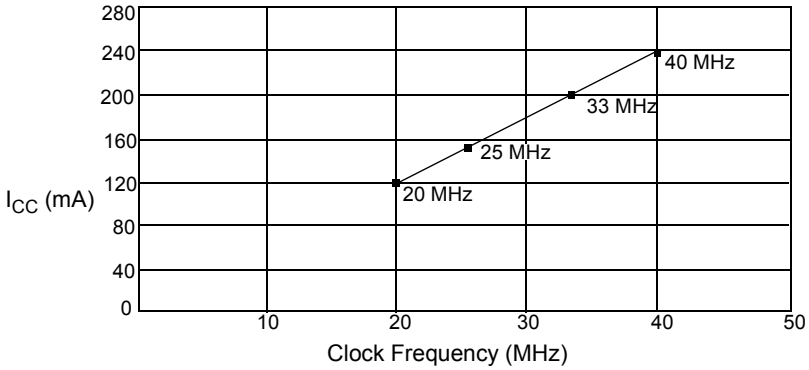



**Figure 12. Typical $I_{cc}$ Versus Frequency for Am186ED Microcontroller**

## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

## Read Cycle (20 MHz and 25 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 20 MHz | | 25 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **General Timing Requirements** | | | | | | | |
| 1 | $t_{DVCL}$ | Data in Setup | 10 | | 10 | | ns |
| 2 | $t_{CLDX}$ | Data in Hold[c] | 3 | | 3 | | ns |
| **General Timing Responses** | | | | | | | |
| 3 | $t_{CHSV}$ | Status Active Delay | 0 | 25 | 0 | 20 | ns |
| 4 | $t_{CLSH}$ | Status Inactive Delay | 0 | 25 | 0 | 20 | ns |
| 5 | $t_{CLAV}$ | AD Address Valid Delay and BHE | 0 | 25 | 0 | 20 | ns |
| 6 | $t_{CLAX}$ | Address Hold | 0 | 25 | 0 | 20 | ns |
| 8 | $t_{CHDX}$ | Status Hold Time | 0 | | 0 | | ns |
| 9 | $t_{CHLH}$ | ALE Active Delay | | 25 | | 20 | ns |
| 10 | $t_{LHLL}$ | ALE Width | $t_{CLCL}-10=40$ | | $t_{CLCL}-10=30$ | | ns |
| 11 | $t_{CHLL}$ | ALE Inactive Delay | | 25 | | 20 | ns |
| 12 | $t_{AVLL}$ | AD Address Valid to ALE Low[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 13 | $t_{LLAX}$ | AD Address Hold from ALE Inactive[a] | $t_{CHCL}-2$ | | $t_{CHCL}-2$ | | ns |
| 14 | $t_{AVCH}$ | AD Address Valid to Clock High | 0 | | 0 | | ns |
| 15 | $t_{CLAZ}$ | AD Address Float Delay | $t_{CLAX}=0$ | 25 | $t_{CLAX}=0$ | 20 | ns |
| 16 | $t_{CLCSV}$ | $\overline{MCS}/\overline{PCS}$ Active Delay | 0 | 25 | 0 | 20 | ns |
| 17 | $t_{CXCSX}$ | $\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 18 | $t_{CHCSX}$ | $\overline{MCS}/\overline{PCS}$ Inactive Delay | 0 | 25 | 0 | 20 | ns |
| 19 | $t_{DXDL}$ | $\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a] | 0 | | 0 | | ns |
| 20 | $t_{CVCTV}$ | Control Active Delay 1[b] | 0 | 25 | 0 | 20 | ns |
| 21 | $t_{CVDEX}$ | $\overline{DEN}$ Inactive Delay | 0 | 25 | 0 | 20 | ns |
| 22 | $t_{CHCTV}$ | Control Active Delay 2[b] | 0 | 25 | 0 | 20 | ns |
| 23 | $t_{LHAV}$ | ALE High to Address Valid | 20 | | 15 | | ns |
| 99 | $t_{PLAL}$ | $\overline{PCS}$ Active to ALE Inactive | 15 | 28 | 15 | 24 | ns |
| **Read Cycle Timing Responses** | | | | | | | |
| 24 | $t_{AZRL}$ | AD Address Float to $\overline{RD}$ Active | 0 | | 0 | | ns |
| 25 | $t_{CLRL}$ | $\overline{RD}$ Active Delay | 0 | 25 | 0 | 20 | ns |
| 26 | $t_{RLRH}$ | $\overline{RD}$ Pulse Width | $2t_{CLCL}-15=85$ | | $2t_{CLCL}-15=65$ | | ns |
| 27 | $t_{CLRH}$ | $\overline{RD}$ Inactive Delay | 0 | 25 | 0 | 20 | ns |
| 28 | $t_{RHLH}$ | $\overline{RD}$ Inactive to ALE High[a] | $t_{CLCH}-3$ | | $t_{CLCH}-3$ | | ns |
| 29 | $t_{RHAV}$ | $\overline{RD}$ Inactive to AD Address Active[a] | $t_{CLCL}-10=40$ | | $t_{CLCL}-10=30$ | | ns |
| 41 | $t_{DSHLH}$ | $\overline{DS}$ Inactive to ALE Active | $t_{CLCH}-2=21$ | | $t_{CLCH}-2=16$ | | ns |
| 59 | $t_{RHDX}$ | $\overline{RD}$ High to Data Hold on AD Bus[c] | 0 | | 0 | | ns |
| 66 | $t_{AVRL}$ | A Address Valid to $\overline{RD}$ Low[a] | $t_{CLCL}+t_{CHCL}-3$ | | $t_{CLCL}+t_{CHCL}-3$ | | ns |
| 67 | $t_{CHCSV}$ | CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid | 0 | 25 | 0 | 20 | ns |
| 68 | $t_{CHAV}$ | CLKOUTA High to A Address Valid | 0 | 25 | 0 | 20 | ns |

***Notes:***

*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a Equal loading on referenced pins.*

*b This parameter applies to the $\overline{DEN}$, $\overline{DS}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.*

*c If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

## Read Cycle (33 MHz and 40 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 33 MHz | | 40 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **General Timing Requirements** | | | | | | | |
| 1 | $t_{DVCL}$ | Data in Setup | 8 | | 5 | | ns |
| 2 | $t_{CLDX}$ | Data in Hold[c] | 3 | | 2 | | ns |
| **General Timing Responses** | | | | | | | |
| 3 | $t_{CHSV}$ | Status Active Delay | 0 | 15 | 0 | 12 | ns |
| 4 | $t_{CLSH}$ | Status Inactive Delay | 0 | 15 | 0 | 12 | ns |
| 5 | $t_{CLAV}$ | AD Address Valid Delay and BHE | 0 | 15 | 0 | 12 | ns |
| 6 | $t_{CLAX}$ | Address Hold | 0 | 15 | 0 | 12 | ns |
| 8 | $t_{CHDX}$ | Status Hold Time | 0 | | 0 | | ns |
| 9 | $t_{CHLH}$ | ALE Active Delay | | 15 | | 12 | ns |
| 10 | $t_{LHLL}$ | ALE Width | $t_{CLCL}-10=20$ | | $t_{CLCL}-5=20$ | | ns |
| 11 | $t_{CHLL}$ | ALE Inactive Delay | | 15 | | 12 | ns |
| 12 | $t_{AVLL}$ | AD Address Valid to ALE Low[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 13 | $t_{LLAX}$ | AD Address Hold from ALE Inactive[a] | $t_{CHCL}-2$ | | $t_{CHCL}-2$ | | ns |
| 14 | $t_{AVCH}$ | AD Address Valid to Clock High | 0 | | 0 | | ns |
| 15 | $t_{CLAZ}$ | AD Address Float Delay | $t_{CLAX}=0$ | 15 | $t_{CLAX}=0$ | 12 | ns |
| 16 | $t_{CLCSV}$ | $\overline{MCS}/\overline{PCS}$ Active Delay | 0 | 15 | 0 | 12 | ns |
| 17 | $t_{CXCSX}$ | $\overline{MCS}/\overline{PCS}$ Hold from Command Inactive[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 18 | $t_{CHCSX}$ | $\overline{MCS}/\overline{PCS}$ Inactive Delay | 0 | 15 | 0 | 12 | ns |
| 19 | $t_{DXDL}$ | $\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a] | 0 | | 0 | | ns |
| 20 | $t_{CVCTV}$ | Control Active Delay 1[b] | 0 | 15 | 0 | 12 | ns |
| 21 | $t_{CVDEX}$ | $\overline{DEN}$ Inactive Delay | 0 | 15 | 0 | 12 | ns |
| 22 | $t_{CHCTV}$ | Control Active Delay 2[b] | 0 | 15 | 0 | 12 | ns |
| 23 | $t_{LHAV}$ | ALE High to Address Valid | 10 | | 7.5 | | ns |
| 99 | $t_{PLAL}$ | $\overline{PCS}$ Active to ALE Inactive | 12 | 20 | 10 | 18 | ns |
| **Read Cycle Timing Responses** | | | | | | | |
| 24 | $t_{AZRL}$ | AD Address Float to $\overline{RD}$ Active | 0 | | 0 | | ns |
| 25 | $t_{CLRL}$ | $\overline{RD}$ Active Delay | 0 | 15 | 0 | 10 | ns |
| 26 | $t_{RLRH}$ | $\overline{RD}$ Pulse Width | $2t_{CLCL}-15=45$ | | $2t_{CLCL}-10=40$ | | ns |
| 27 | $t_{CLRH}$ | $\overline{RD}$ Inactive Delay | 0 | 15 | 0 | 12 | ns |
| 28 | $t_{RHLH}$ | $\overline{RD}$ Inactive to ALE High[a] | $t_{CLCH}-3$ | | $t_{CLCH}-2$ | | ns |
| 29 | $t_{RHAV}$ | $\overline{RD}$ Inactive to AD Address Active[a] | $t_{CLCL}-10=20$ | | $t_{CLCL}-5=20$ | | ns |
| 41 | $t_{DSHLH}$ | $\overline{DS}$ Inactive to ALE Active | $t_{CLCH}-2=11.5$ | | $t_{CLCH}-2=9.25$ | | |
| 59 | $t_{RHDX}$ | $\overline{RD}$ High to Data Hold on AD Bus[c] | 0 | | 0 | | ns |
| 66 | $t_{AVRL}$ | A Address Valid to $\overline{RD}$ Low[a] | $t_{CLCL}+t_{CHCL}-3$ | | $t_{CLCL}+t_{CHCL}-1.25$ | | ns |
| 67 | $t_{CHCSV}$ | CLKOUTA High to $\overline{LCS}/\overline{UCS}$ Valid | 0 | 15 | 0 | 10 | ns |
| 68 | $t_{CHAV}$ | CLKOUTA High to A Address Valid | 0 | 15 | 0 | 10 | ns |

***Notes:***

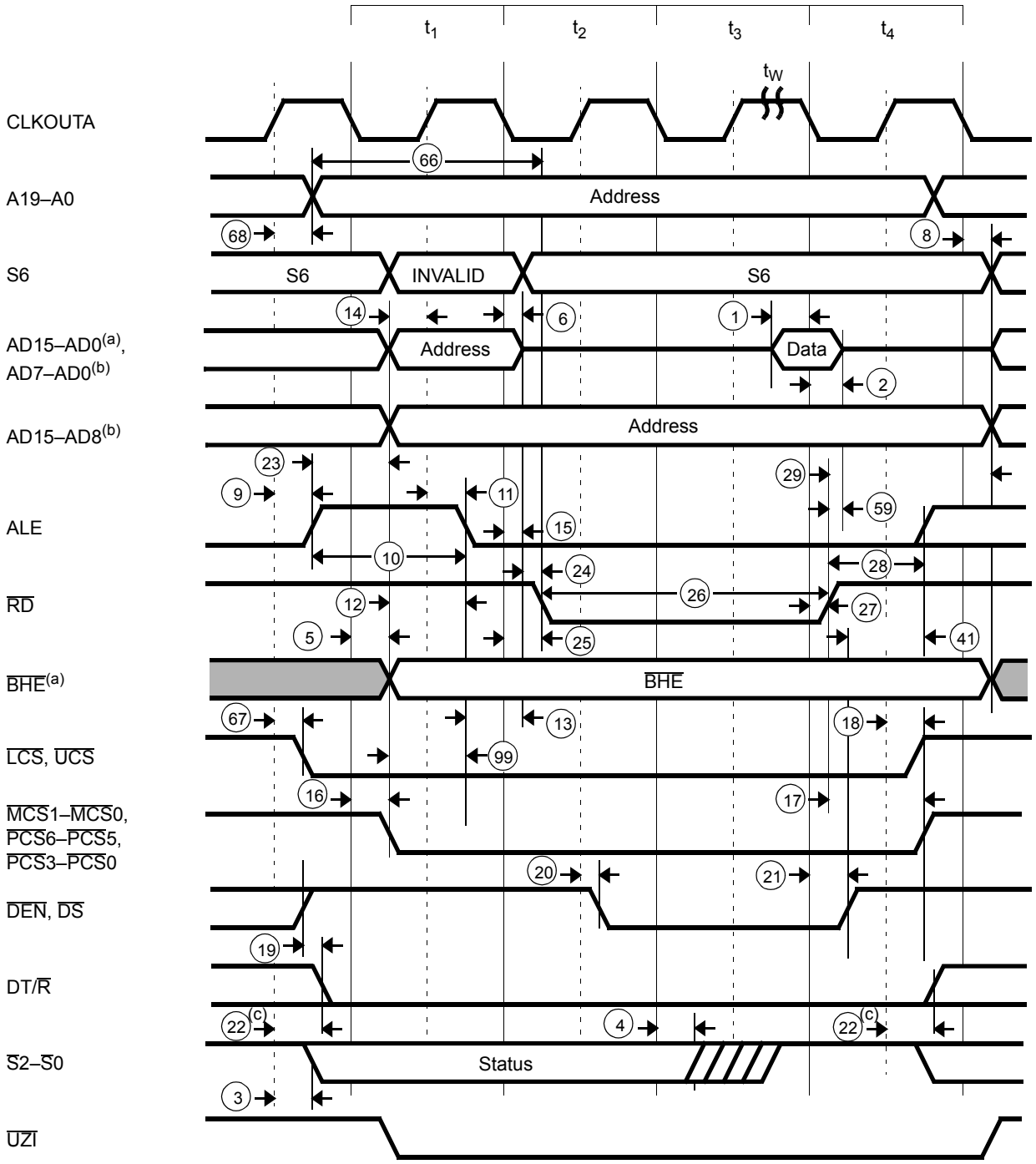
*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a Equal loading on referenced pins.*

*b This parameter applies to the $\overline{DEN}$, $\overline{DS}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.*

*c If either spec 2 or spec 59 is met with respect to data hold time, the part will function correctly.*

## READ CYCLE WAVEFORMS




***Notes:***

*a Am186ED/EDLV microcontrollers in 16-bit mode*

*b Am186ED/EDLV microcontrollers in 8-bit mode*

*c Changes in t phase preceding next bus cycle if followed by read, INTA, or halt.*

## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

### Write Cycle (20 MHz and 25 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 20 MHz | | 25 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **General Timing Responses** | | | | | | | |
| 3 | $t_{CHSV}$ | Status Active Delay | 0 | 25 | 0 | 20 | ns |
| 4 | $t_{CLSH}$ | Status Inactive Delay | 0 | 25 | 0 | 20 | ns |
| 5 | $t_{CLAV}$ | AD Address Valid Delay and BHE | 0 | 25 | 0 | 20 | ns |
| 6 | $t_{CLAX}$ | Address Hold | 0 | 25 | 0 | 20 | ns |
| 7 | $t_{CLDV}$ | Data Valid Delay | 0 | 15 | 0 | 15 | ns |
| 8 | $t_{CHDX}$ | Status Hold Time | 0 | | 0 | | ns |
| 9 | $t_{CHLH}$ | ALE Active Delay | | 25 | | 20 | ns |
| 10 | $t_{LHLL}$ | ALE Width | $t_{CLCL}-10=40$ | | $t_{CLCL}-10=30$ | | ns |
| 11 | $t_{CHLL}$ | ALE Inactive Delay | | 25 | | 20 | ns |
| 12 | $t_{AVLL}$ | AD Address Valid to ALE Low[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 13 | $t_{LLAX}$ | AD Address Hold from ALE Inactive[a] | $t_{CHCL}-2$ | | $t_{CHCL}-2$ | | ns |
| 14 | $t_{AVCH}$ | AD Address Valid to Clock High | 0 | | 0 | | ns |
| 16 | $t_{CLCSV}$ | $\overline{MCS}$/$\overline{PCS}$ Active Delay | 0 | 25 | 0 | 20 | ns |
| 17 | $t_{CXCSX}$ | $\overline{MCS}$/$\overline{PCS}$ Hold from Command Inactive[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 18 | $t_{CHCSX}$ | $\overline{MCS}$/$\overline{PCS}$ Inactive Delay | 0 | 25 | 0 | 20 | ns |
| 19 | $t_{DXDL}$ | $\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a] | 0 | | 0 | | ns |
| 20 | $t_{CVCTV}$ | Control Active Delay 1[b] | 0 | 15 | 0 | 15 | ns |
| 21 | $t_{CVDEX}$ | $\overline{DS}$ Inactive Delay | 0 | 25 | 0 | 20 | ns |
| 22 | $t_{CHCTV}$ | Control Active Delay 2 | 0 | 25 | 0 | 20 | ns |
| 23 | $t_{LHAV}$ | ALE High to Address Valid | 20 | | 15 | | ns |
| 99 | $t_{PLAL}$ | $\overline{PCS}$ Active to ALE Inactive | 15 | 28 | 15 | 24 | ns |
| **Write Cycle Timing Responses** | | | | | | | |
| 30 | $t_{CLDOX}$ | Data Hold Time | 0 | | 0 | | ns |
| 31 | $t_{CVCTX}$ | Control Inactive Delay[b] | 0 | 25 | 0 | 20 | ns |
| 32 | $t_{WLWH}$ | $\overline{WR}$ Pulse Width | $2t_{CLCL}-10=90$ | | $2t_{CLCL}-10=70$ | | ns |
| 33 | $t_{WHLH}$ | $\overline{WR}$ Inactive to ALE High[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 34 | $t_{WHDX}$ | Data Hold after $\overline{WR}$[a] | $t_{CLCL}-10=40$ | | $t_{CLCL}-10=30$ | | ns |
| 35 | $t_{WHDEX}$ | $\overline{WR}$ Inactive to $\overline{DEN}$ Inactive[a] | $t_{CLCH}-3$ | | $t_{CLCH}-3$ | | ns |
| 41 | $t_{DSHLH}$ | $\overline{DS}$ Inactive to ALE Active | $t_{CLCH}-2=21$ | | $t_{CLCH}-2=16$ | | ns |
| 65 | $t_{AVWL}$ | A Address Valid to $\overline{WR}$ Low | $t_{CLCL}+t_{CHCL}-3$ | | $t_{CLCL}+t_{CHCL}-3$ | | ns |
| 67 | $t_{CHCSV}$ | CLKOUTA High to $\overline{LCS}$/$\overline{UCS}$ Valid | 0 | 25 | 0 | 20 | ns |
| 68 | $t_{CHAV}$ | CLKOUTA High to A Address Valid | 0 | 25 | 0 | 20 | ns |
| 87 | $t_{AVBL}$ | A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low | $t_{CHCL}-3$ | 25 | $t_{CHCL}-3$ | 20 | ns |
| 98 | $t_{DSHDIW}$ | $\overline{DS}$ High to Data Invalid—Write | 35 | | 30 | | ns |

***Notes:***

*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a Testing is performed with equal loading on referenced pins.*

*b This parameter applies to the $\overline{DEN}$, $\overline{DS}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

## Write Cycle (33 MHz and 40 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 33 MHz | | 40 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **General Timing Responses** | | | | | | | |
| 3 | $t_{CHSV}$ | Status Active Delay | 0 | 15 | 0 | 12 | ns |
| 4 | $t_{CLSH}$ | Status Inactive Delay | 0 | 15 | 0 | 12 | ns |
| 5 | $t_{CLAV}$ | AD Address Valid Delay and BHE | 0 | 15 | 0 | 12 | ns |
| 6 | $t_{CLAX}$ | Address Hold | 0 | | 0 | | ns |
| 7 | $t_{CLDV}$ | Data Valid Delay | 0 | 15 | 0 | 12 | ns |
| 8 | $t_{CHDX}$ | Status Hold Time | 0 | | 0 | | ns |
| 9 | $t_{CHLH}$ | ALE Active Delay | | 15 | | 12 | ns |
| 10 | $t_{LHLL}$ | ALE Width | $t_{CLCL}-10=20$ | | $t_{CLCL}-5=20$ | | ns |
| 11 | $t_{CHLL}$ | ALE Inactive Delay | | 15 | | 12 | ns |
| 12 | $t_{AVLL}$ | AD Address Valid to ALE Low[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 13 | $t_{LLAX}$ | AD Address Hold from ALE Inactive[a] | $t_{CHCL}-2$ | | $t_{CHCL}-2$ | | ns |
| 14 | $t_{AVCH}$ | AD Address Valid to Clock High | 0 | | 0 | | ns |
| 16 | $t_{CLCSV}$ | $\overline{MCS}$/$\overline{PCS}$ Active Delay | 0 | 15 | 0 | 12 | ns |
| 17 | $t_{CXCSX}$ | $\overline{MCS}$/$\overline{PCS}$ Hold from Command Inactive[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 18 | $t_{CHCSX}$ | $\overline{MCS}$/$\overline{PCS}$ Inactive Delay | 0 | 15 | 0 | 12 | ns |
| 19 | $t_{DXDL}$ | $\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a] | 0 | | 0 | | ns |
| 20 | $t_{CVCTV}$ | Control Active Delay 1[b] | 0 | 15 | 0 | 12 | ns |
| 21 | $t_{CVDEX}$ | $\overline{DS}$ Inactive Delay | 0 | 15 | 0 | 12 | ns |
| 22 | $t_{CHCTV}$ | Control Active Delay 2 | 0 | 15 | 0 | 12 | ns |
| 23 | $t_{LHAV}$ | ALE High to Address Valid | 10 | | 7.5 | | ns |
| 99 | $t_{PLAL}$ | $\overline{PCS}$ Active to ALE Inactive | 12 | 20 | 10 | 18 | ns |
| **Write Cycle Timing Responses** | | | | | | | |
| 30 | $t_{CLDOX}$ | Data Hold Time | 0 | | 0 | | ns |
| 31 | $t_{CVCTX}$ | Control Inactive Delay[b] | 0 | 15 | 0 | 12 | ns |
| 32 | $t_{WLWH}$ | $\overline{WR}$ Pulse Width | $2t_{CLCL}-10=50$ | | $2t_{CLCL}-10=40$ | | ns |
| 33 | $t_{WHLH}$ | $\overline{WR}$ Inactive to ALE High[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 34 | $t_{WHDX}$ | Data Hold after $\overline{WR}$[a] | $t_{CLCL}-10=20$ | | $t_{CLCL}-10=15$ | | ns |
| 35 | $t_{WHDEX}$ | $\overline{WR}$ Inactive to $\overline{DEN}$ Inactive[a] | $t_{CLCH}-3$ | | $t_{CLCH}-3$ | | ns |
| 41 | $t_{DSHLH}$ | $\overline{DS}$ Inactive to ALE Active | $t_{CLCH}-2=11.5$ | | $t_{CLCH}-2=9.25$ | | ns |
| 65 | $t_{AVWL}$ | A Address Valid to $\overline{WR}$ Low | $t_{CLCL}+t_{CHCL}-3$ | | $t_{CLCL}+t_{CHCL}-1.25$ | | ns |
| 67 | $t_{CHCSV}$ | CLKOUTA High to $\overline{LCS}$/$\overline{UCS}$ Valid | 0 | 15 | 0 | 10 | ns |
| 68 | $t_{CHAV}$ | CLKOUTA High to A Address Valid | 0 | 15 | 0 | 10 | ns |
| 87 | $t_{AVBL}$ | A Address Valid to $\overline{WHB}$, $\overline{WLB}$ Low | $t_{CHCL}-3$ | 15 | $t_{CHCL}-1.25$ | 12 | ns |
| 98 | $t_{DSHDIW}$ | $\overline{DS}$ High to Data Invalid—Write | 20 | | 15 | | ns |

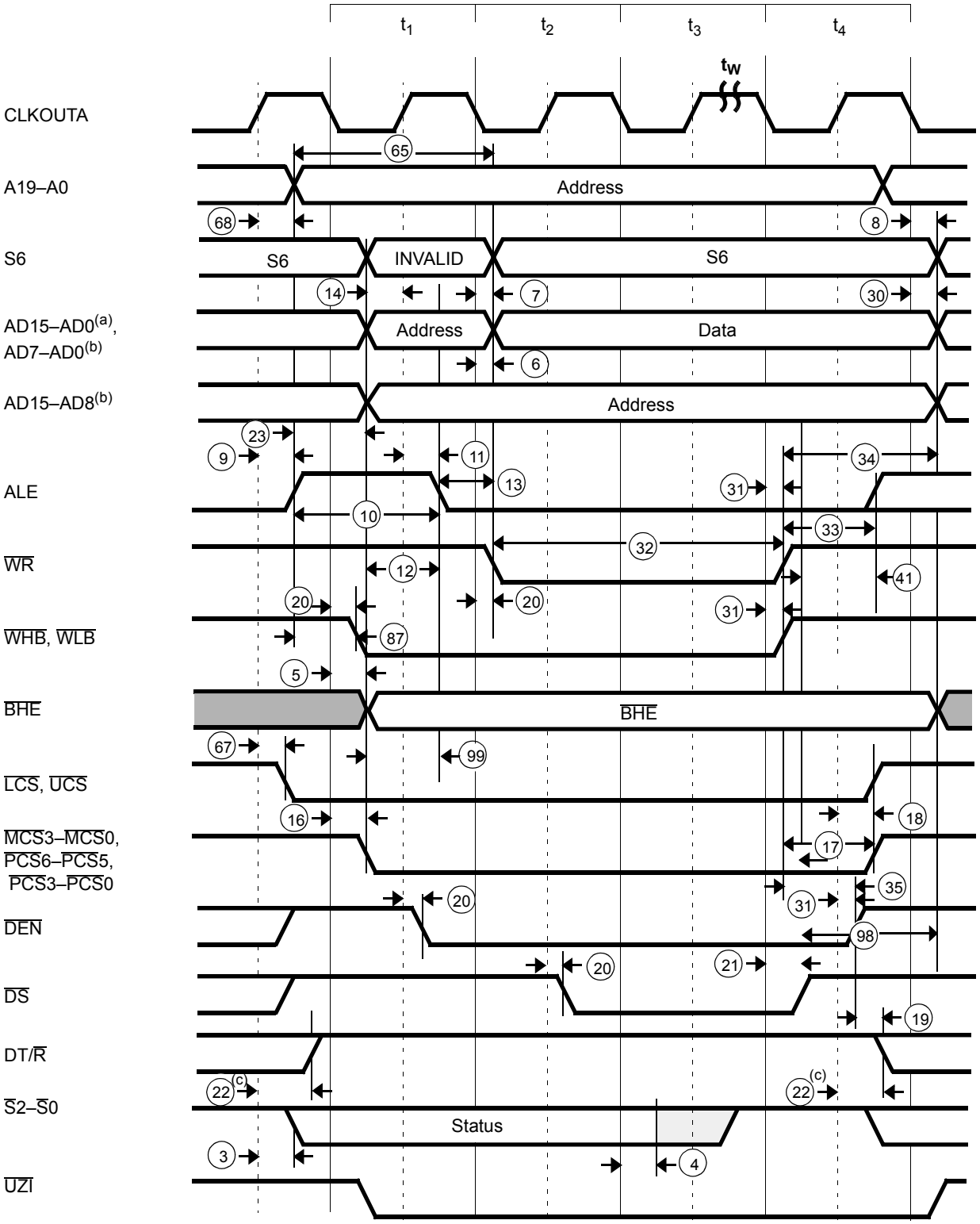
***Notes:***

*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a Testing is performed with equal loading on referenced pins.*

*b This parameter applies to the $\overline{DEN}$, $\overline{DS}$, $\overline{INTA1}$–$\overline{INTA0}$, $\overline{WR}$, $\overline{WHB}$, and $\overline{WLB}$ signals.*

## WRITE CYCLE WAVEFORMS




***Notes:***

*a Am186ED/EDLV microcontrollers in 16-bit mode*

*b Am186ED/EDLV microcontrollers in 8-bit mode*

*c Changes in t phase preceding next bus cycle if followed by read, INTA, or halt*

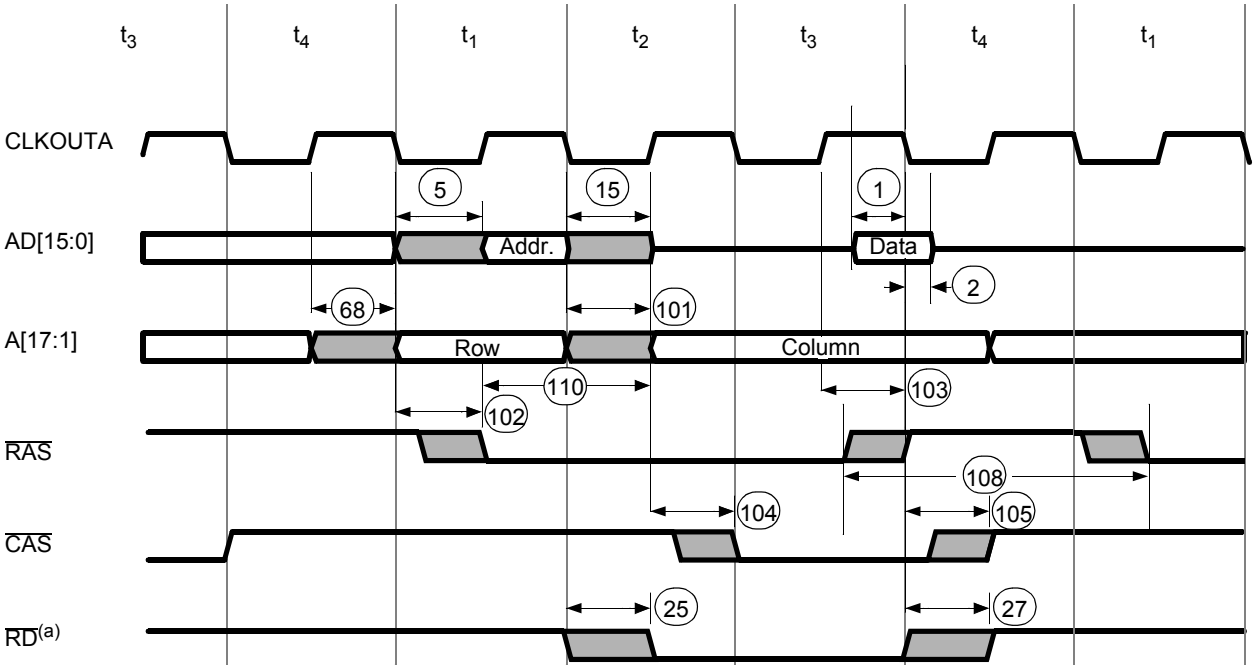
## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges DRAM

| Parameter | | | Preliminary | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 20 MHz | | 25 MHz | | 33 MHz | | 40 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | Min | Max | Min | Max | |
| **General Timing Responses** | | | | | | | | | | | |
| 101 | $t_{CHCAV}$ | CLKOUTA Low to Column Address Valid | 0 | 25 | 0 | 20 | 0 | 15 | 0 | 12 | ns |
| 102 | $t_{CLRA}$ | CLKOUTA Low to $\overline{RAS}$ Active | 3 | 25 | 3 | 20 | 3 | 15 | 3 | 12 | ns |
| 103 | $t_{CHRX}$ | CLKOUTA High to $\overline{RAS}$ Inactive | 3 | 25 | 3 | 20 | 3 | 15 | 3 | 12 | ns |
| 104 | $t_{CHCA}$ | CLKOUTA High to $\overline{CAS}$ Active | 3 | 25 | 3 | 20 | 3 | 15 | 3 | 12 | ns |
| 105 | $t_{CLCX}$ | CLKOUTA Low to $\overline{CAS}$ Inactive | 3 | 25 | 3 | 20 | 3 | 15 | 3 | 12 | ns |
| 106 | $t_{CHRA}$ | CLKOUTA High to $\overline{RAS}$ Active | 3 | 25 | 3 | 20 | 3 | 15 | 3 | 12 | ns |
| 107 | $t_{CLRX}$ | CLKOUTA Low to $\overline{RAS}$ Inactive | 3 | 25 | 3 | 20 | 3 | 15 | 3 | 12 | ns |
| 108 | $t_{RP0W}$ | $\overline{RAS}$ Inactive Pulse Width with 0 Wait States | 60 | — | 50 | — | 40 | — | 30 | — | ns |
| 109 | $t_{RP1W}$ | $\overline{RAS}$ Inactive Pulse Width with 1 or More Wait States | 70 | — | 60 | — | 50 | — | 40 | — | ns |
| 110 | $t_{RD0W}$ | $\overline{RAS}$ To Column Address Delay Time with 0 Wait States | 25 | — | 20 | — | 15 | — | 15 | — | ns |
| 111 | $t_{RD1W}$ | $\overline{RAS}$ to Column Address Delay Time with 1 or More Wait States | 30 | — | 25 | — | 20 | — | 15 | — | ns |

As guaranteed by design, the following table shows the minimum time for $\overline{RAS}$ assertion to $\overline{RAS}$ assertion. These minimums correlate to DRAM spec $t_{RC}$.

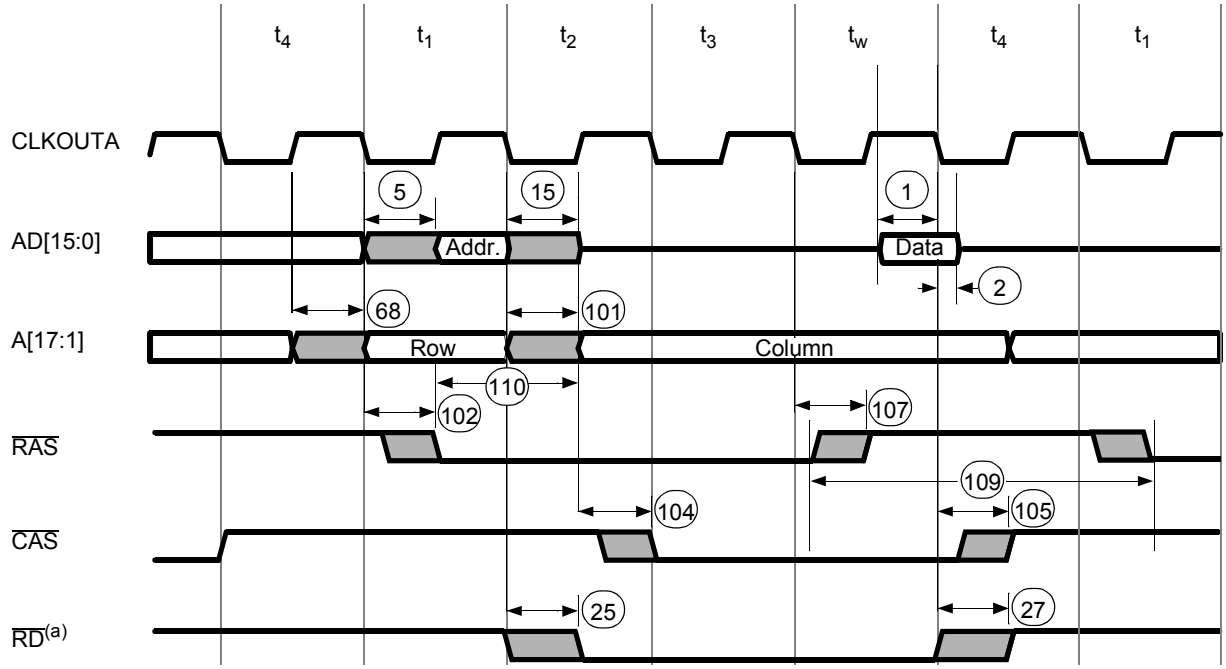
| | | Wait States | | | |
|---|---|---|---|---|---|
| | | 0 | 1 | 2 | 3 |
| Frequency | 40 MHz | 90 | 110 | 130 | 150 |
| | 33 MHz | 110 | 130 | 150 | 170 |
| | 25 MHz | 130 | 150 | 170 | 190 |
| | 20 MHz | 150 | 170 | 190 | 210 |

## DRAM Read Cycle Timing with No-Wait States



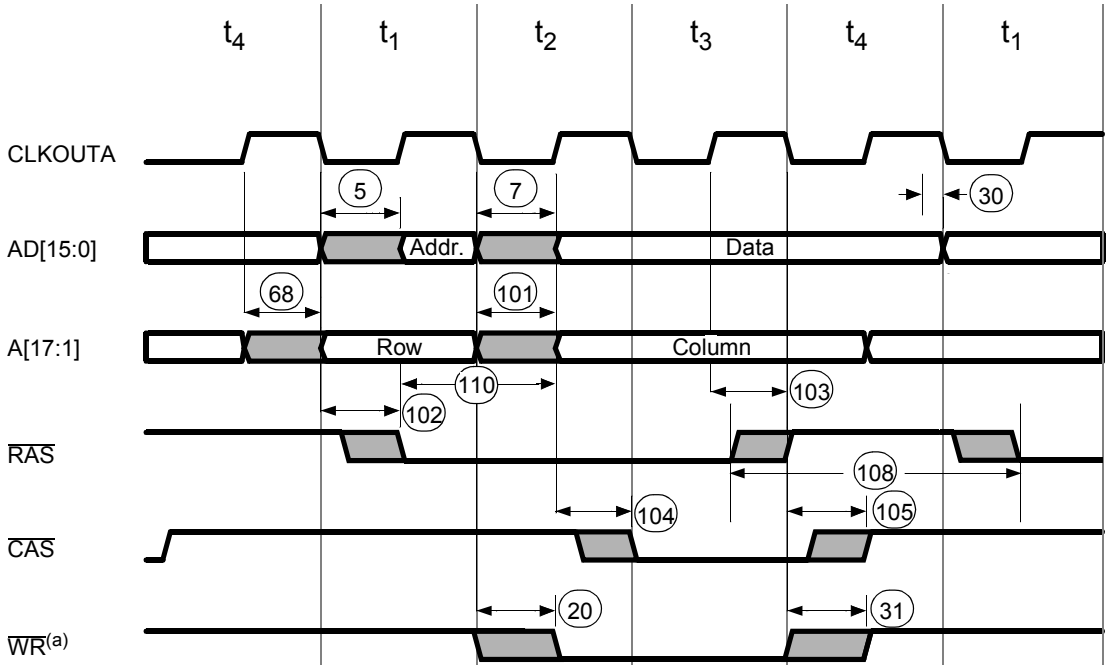

***Note:***
*a The $\overline{RD}$ output connects to the DRAM output enable ($\overline{OE}$) pin for read operations.*

## DRAM Read Cycle Timing with Wait State(s)



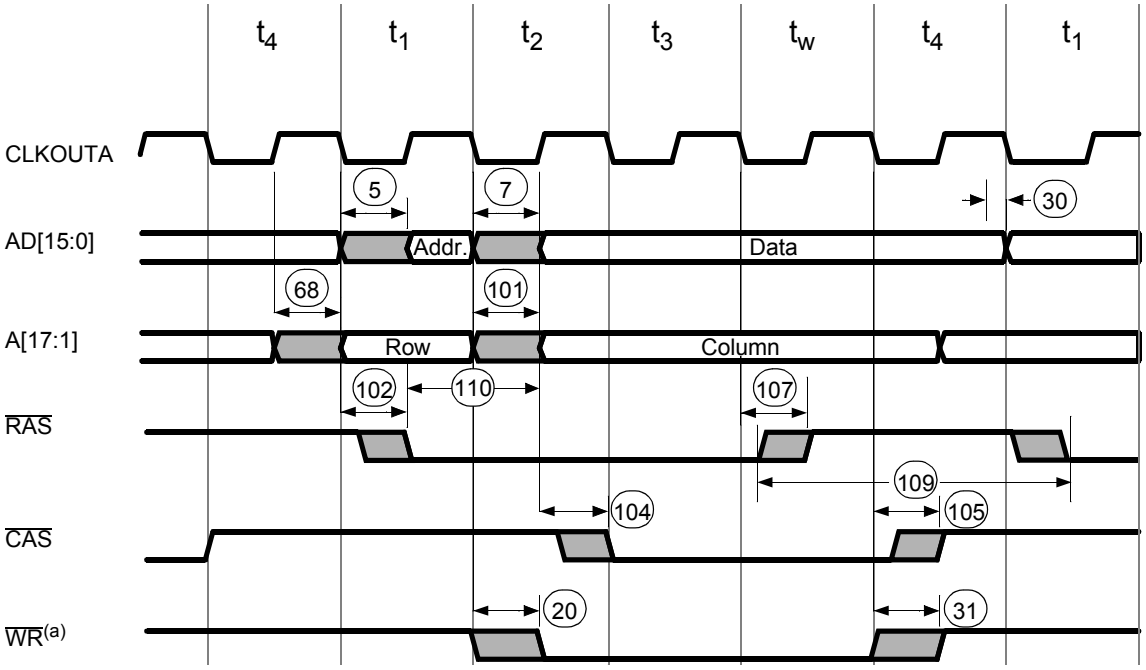

***Note:***
*a The $\overline{RD}$ output connects to the DRAM output enable ($\overline{OE}$) pin for read operations.*

## DRAM Write Cycle Timing with No-Wait States



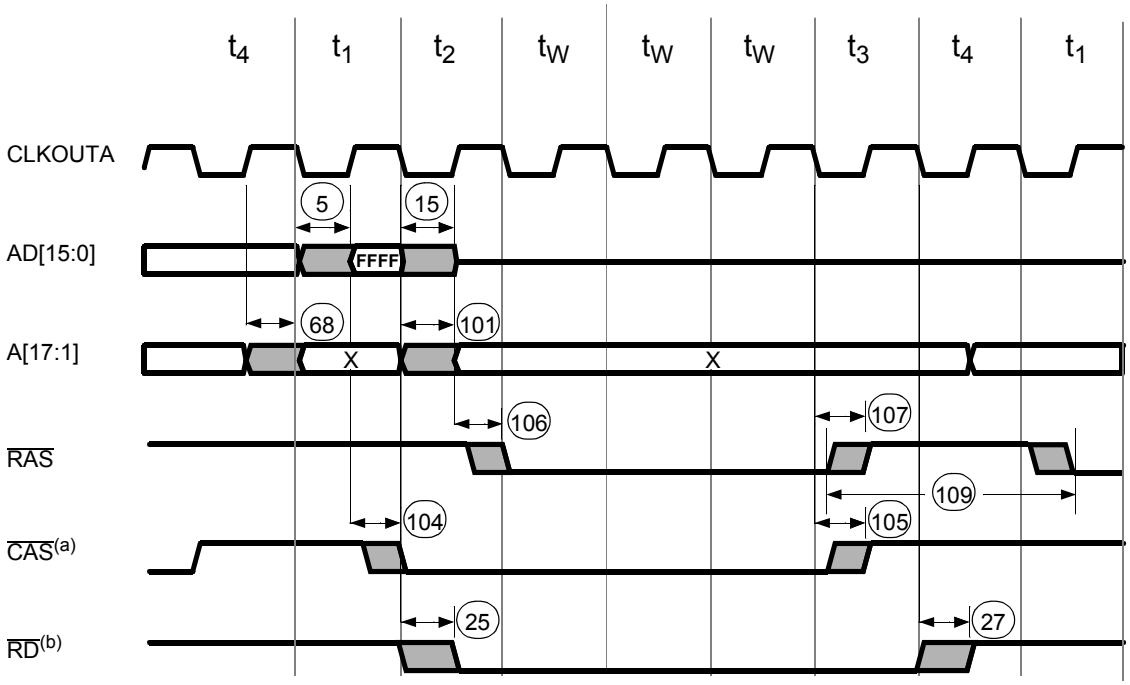

***Note:***
*a Write operations use the $\overline{WR}$ output connected to the DRAM write enable ($\overline{WE}$) pin.*

## DRAM Write Cycle Timing With Wait State(s)




***Note:***
*a Write operations use the $\overline{WR}$ output connected to the DRAM write enable ($\overline{WE}$) pin.*

## DRAM $\overline{CAS}$-before-$\overline{RAS}$ Cycle Timing




***Notes:***

*a* *$\overline{CAS}$ before $\overline{RAS}$ cycle timing is always 7 clocks, independent of wait state timing.*

*b* *The $\overline{RD}$ output connects to the DRAM output enable ($\overline{OE}$) pin for read operations.*

## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

## Interrupt Acknowledge Cycle (20 MHz and 25 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 20 MHz | | 25 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **General Timing Requirements** | | | | | | | |
| 1 | $t_{DVCL}$ | Data in Setup | 10 | | 10 | | ns |
| 2 | $t_{CLDX}$ | Data in Hold | 3 | | 3 | | ns |
| **General Timing Responses** | | | | | | | |
| 3 | $t_{CHSV}$ | Status Active Delay | 0 | 25 | 0 | 20 | ns |
| 4 | $t_{CLSH}$ | Status Inactive Delay | 0 | 25 | 0 | 20 | ns |
| 7 | $t_{CLDV}$ | Data Valid Delay | 0 | 25 | 0 | 20 | ns |
| 8 | $t_{CHDX}$ | Status Hold Time | 0 | | 0 | | ns |
| 9 | $t_{CHLH}$ | ALE Active Delay | | 25 | | 20 | ns |
| 10 | $t_{LHLL}$ | ALE Width | $t_{CLCL}-10=40$ | | $t_{CLCL}-10=30$ | | ns |
| 11 | $t_{CHLL}$ | ALE Inactive Delay | | 25 | | 20 | ns |
| 12 | $t_{AVLL}$ | AD Address Invalid to ALE Low[a] | $t_{CLCH}-2$ | | $t_{CLCH}-2$ | | ns |
| 15 | $t_{CLAZ}$ | AD Address Float Delay | $t_{CLAX}=0$ | 25 | $t_{CLAX}=0$ | 20 | ns |
| 19 | $t_{DXDL}$ | $\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a] | 0 | | 0 | | ns |
| 20 | $t_{CVCTV}$ | Control Active Delay 1[b] | 0 | 25 | 0 | 20 | ns |
| 21 | $t_{CVDEX}$ | $\overline{DEN}$ Inactive Delay | 0 | 25 | 0 | 20 | ns |
| 22 | $t_{CHCTV}$ | Control Active Delay 2[c] | 0 | 25 | 0 | 20 | ns |
| 23 | $t_{LHAV}$ | ALE High to Address Valid | 20 | | 15 | | ns |
| 31 | $t_{CVCTX}$ | Control Inactive Delay[b] | 0 | 25 | 0 | 20 | ns |
| 68 | $t_{CHAV}$ | CLKOUTA High to A Address Valid | 0 | 25 | 0 | 20 | ns |

***Notes:***

*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a Testing is performed with equal loading on referenced pins.*

*b This parameter applies to the $\overline{INTA}1$–$\overline{INTA}0$ signals.*

*c This parameter applies to the $\overline{DEN}$ and DT/$\overline{R}$ signals.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

## Interrupt Acknowledge Cycle (33 MHz and 40 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 33 MHz | | 40 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **General Timing Requirements** | | | | | | | |
| 1 | $t_{DVCL}$ | Data in Setup | 8 | | 5 | | ns |
| 2 | $t_{CLDX}$ | Data in Hold | 3 | | 2 | | ns |
| **General Timing Responses** | | | | | | | |
| 3 | $t_{CHSV}$ | Status Active Delay | 0 | 15 | 0 | 12 | ns |
| 4 | $t_{CLSH}$ | Status Inactive Delay | 0 | 15 | 0 | 12 | ns |
| 7 | $t_{CLDV}$ | Data Valid Delay | 0 | 15 | 0 | 12 | ns |
| 8 | $t_{CHDX}$ | Status Hold Time | 0 | | 0 | | ns |
| 9 | $t_{CHLH}$ | ALE Active Delay | | 15 | | 12 | ns |
| 10 | $t_{LHLL}$ | ALE Width | $t_{CLCL}-10=20$ | | $t_{CLCL}-5=20$ | | ns |
| 11 | $t_{CHLL}$ | ALE Inactive Delay | | 15 | | 12 | ns |
| 12 | $t_{AVLL}$ | AD Address Invalid to ALE Low[a] | $t_{CLCH}$ | | $t_{CLCH}$ | | ns |
| 15 | $t_{CLAZ}$ | AD Address Float Delay | $t_{CLAX}=0$ | 15 | $t_{CLAX}=0$ | 12 | ns |
| 19 | $t_{DXDL}$ | $\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a] | 0 | | 0 | | ns |
| 20 | $t_{CVCTV}$ | Control Active Delay 1[b] | 0 | 15 | 0 | 12 | ns |
| 21 | $t_{CVDEX}$ | $\overline{DEN}$ Inactive Delay | 0 | 15 | 0 | 12 | ns |
| 22 | $t_{CHCTV}$ | Control Active Delay 2[c] | 0 | 15 | 0 | 12 | ns |
| 23 | $t_{LHAV}$ | ALE High to Address Valid | 10 | | 7.5 | | ns |
| 31 | $t_{CVCTX}$ | Control Inactive Delay[b] | 0 | 15 | 0 | 12 | ns |
| 68 | $t_{CHAV}$ | CLKOUTA High to A Address Valid | 0 | 15 | 0 | 10 | ns |

***Notes:***

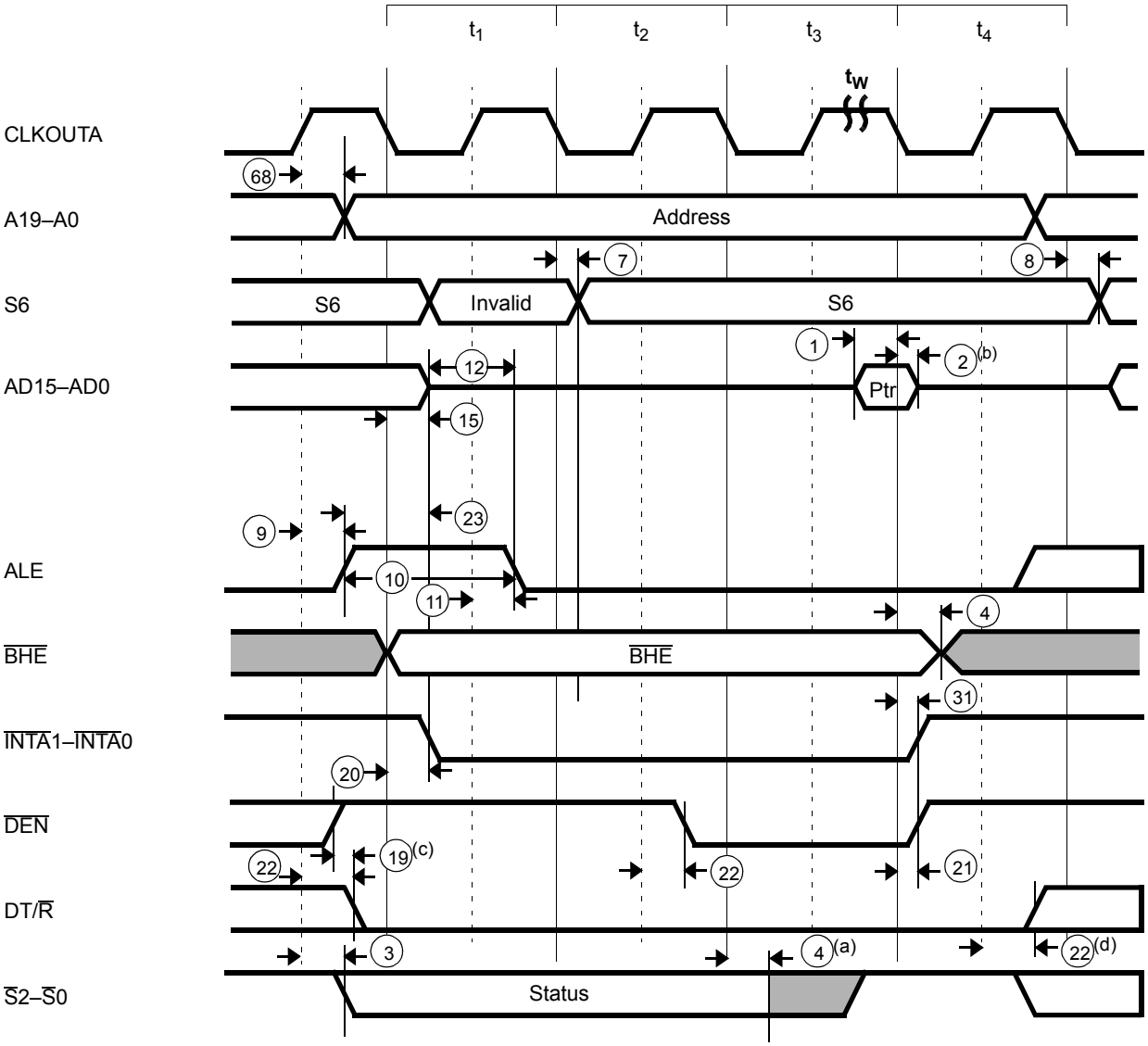
*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a Testing is performed with equal loading on referenced pins.*

*b This parameter applies to the $\overline{INTA}1$–$\overline{INTA}0$ signals.*

*c This parameter applies to the $\overline{DEN}$ and DT/$\overline{R}$ signals.*

## INTERRUPT ACKNOWLEDGE CYCLE WAVEFORMS




***Notes:***

*a The status bits become inactive in the state preceding $t_4$.*

*b The data hold time lasts only until the interrupt acknowledge signal deasserts, even if the interrupt acknowledge transition occurs prior to $t_{CLDX}$ (min).*

*c This parameter applies for an interrupt acknowledge cycle that follows a write cycle.*

*d If followed by a write cycle, this change occurs in the state preceding that write cycle.*

## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

## Software Halt Cycle (20 MHz and 25 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 20 MHz | | 25 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **General Timing Responses** | | | | | | | |
| 3 | $t_{CHSV}$ | Status Active Delay | 0 | 25 | 0 | 20 | ns |
| 4 | $t_{CLSH}$ | Status Inactive Delay | 0 | 25 | 0 | 20 | ns |
| 5 | $t_{CLAV}$ | AD Address Invalid Delay and BHE | 0 | 25 | 0 | 20 | ns |
| 9 | $t_{CHLH}$ | ALE Active Delay | | 25 | | 20 | ns |
| 10 | $t_{LHLL}$ | ALE Width | $t_{CLCL}-10=40$ | | $t_{CLCL}-10=30$ | | ns |
| 11 | $t_{CHLL}$ | ALE Inactive Delay | | 25 | | 20 | ns |
| 19 | $t_{DXDL}$ | $\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a] | 0 | | 0 | | ns |
| 22 | $t_{CHCTV}$ | Control Active Delay 2[b] | 0 | 25 | 0 | 20 | ns |
| 68 | $t_{CHAV}$ | CLKOUTA High to A Address Invalid | 0 | 25 | 0 | 20 | ns |

***Notes:***

*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a Testing is performed with equal loading on referenced pins.*

*b This parameter applies to the $\overline{DEN}$ signal.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

## Software Halt Cycle (33 MHz and 40 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 33 MHz | | 40 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **General Timing Responses** | | | | | | | |
| 3 | $t_{CHSV}$ | Status Active Delay | 0 | 15 | 0 | 12 | ns |
| 4 | $t_{CLSH}$ | Status Inactive Delay | 0 | 15 | 0 | 12 | ns |
| 5 | $t_{CLAV}$ | AD Address Invalid Delay and BHE | 0 | 15 | 0 | 12 | ns |
| 9 | $t_{CHLH}$ | ALE Active Delay | | 15 | | 12 | ns |
| 10 | $t_{LHLL}$ | ALE Width | $t_{CLCL}-10=20$ | | $t_{CLCL}-5=20$ | | ns |
| 11 | $t_{CHLL}$ | ALE Inactive Delay | | 15 | | 12 | ns |
| 19 | $t_{DXDL}$ | $\overline{DEN}$ Inactive to DT/$\overline{R}$ Low[a] | 0 | | 0 | | ns |
| 22 | $t_{CHCTV}$ | Control Active Delay 2[b] | 0 | 15 | 0 | 12 | ns |
| 68 | $t_{CHAV}$ | CLKOUTA High to A Address Invalid | 0 | 15 | 0 | 10 | ns |

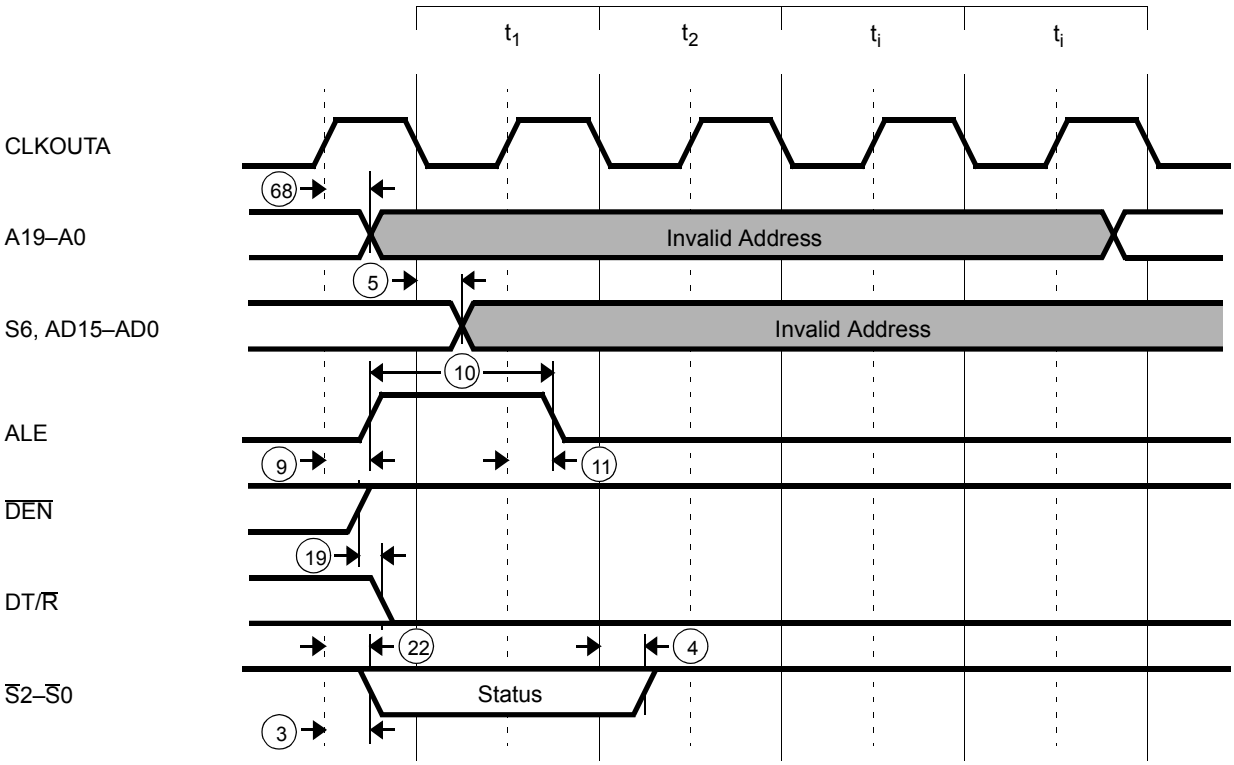
***Notes:***

*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a Testing is performed with equal loading on referenced pins.*

*b This parameter applies to the $\overline{DEN}$ signal.*

## SOFTWARE HALT CYCLE WAVEFORMS



## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

## Clock (20 MHz and 25 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 20 MHz | | 25 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **CLKIN Requirements** | | | | | | | |
| 36 | $t_{CKIN}$ | X1 Period[a] | 50 | 60 | 40 | 60 | ns |
| 37 | $t_{CLCK}$ | X1 Low Time (1.5 V)[a] | 15 | | 15 | | ns |
| 38 | $t_{CHCK}$ | X1 High Time (1.5 V)[a] | 15 | | 15 | | ns |
| 39 | $t_{CKHL}$ | X1 Fall Time (3.5 to 1.0 V)[a] | | 5 | | 5 | ns |
| 40 | $t_{CKLH}$ | X1 Rise Time (1.0 to 3.5 V)[a] | | 5 | | 5 | ns |
| **CLKOUT Timing** | | | | | | | |
| 42 | $t_{CLCL}$ | CLKOUTA Period | 50 | | 40 | | ns |
| 43 | $t_{CLCH}$ | CLKOUTA Low Time ($C_L$=50 pF) | $0.5t_{CLCL}-2=23$ | | $0.5t_{CLCL}-2=18$ | | ns |
| 44 | $t_{CHCL}$ | CLKOUTA High Time ($C_L$=50 pF) | $0.5t_{CLCL}-2=23$ | | $0.5t_{CLCL}-2=18$ | | ns |
| 45 | $t_{CH1CH2}$ | CLKOUTA Rise Time (1.0 to 3.5 V) | | 3 | | 3 | ns |
| 46 | $t_{CL2CL1}$ | CLKOUTA Fall Time (3.5 to 1.0 V) | | 3 | | 3 | ns |
| 61 | $t_{LOCK}$ | Maximum PLL Lock Time | | 1 | | 1 | ms |
| 69 | $t_{CICOA}$ | X1 to CLKOUTA Skew | | 15 | | 15 | ns |
| 70 | $t_{CICOB}$ | X1 to CLKOUTB Skew | | 25 | | 25 | ns |

***Notes:***

*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a The specifications for CLKIN are applicable to the normal PLL and CLKDIV2 modes.*

*The PLL should be used for operations from 16.667 MHz to 40 MHz. For operations below 16.667 MHz, the CLKDIV2 mode should be used.*

*Because the CLKDIV2 input frequency is two times the system frequency, the specifications for twice the frequency should be used for CLKDIV2 mode. For example, use the 20 MHz CLKIN specifications for 10 MHz operation.*

## SWITCHING CHARACTERISTICS over Commercial operating ranges

## Clock (33 MHz and 40 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 33 MHz | | 40 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **CLKIN Requirements** | | | | | | | |
| 36 | $t_{CKIN}$ | X1 Period[a] | 30 | 60 | 25 | 60 | ns |
| 37 | $t_{CLCK}$ | X1 Low Time (1.5 V)[a] | 10 | | 7.5 | | ns |
| 38 | $t_{CHCK}$ | X1 High Time (1.5 V)[a] | 10 | | 7.5 | | ns |
| 39 | $t_{CKHL}$ | X1 Fall Time (3.5 to 1.0 V)[a] | | 5 | | 5 | ns |
| 40 | $t_{CKLH}$ | X1 Rise Time (1.0 to 3.5 V)[a] | | 5 | | 5 | ns |
| **CLKOUT Timing** | | | | | | | |
| 42 | $t_{CLCL}$ | CLKOUTA Period | 30 | | 25 | | ns |
| 43 | $t_{CLCH}$ | CLKOUTA Low Time ($C_L$=50 pF) | $0.5t_{CLCL}-1.5$ =13.5 | | $0.5t_{CLCL}-1.25$ =11.25 | | ns |
| 44 | $t_{CHCL}$ | CLKOUTA High Time ($C_L$=50 pF) | $0.5t_{CLCL}-1.5$ =13.5 | | $0.5t_{CLCL}-1.25$ =11.25 | | ns |
| 45 | $t_{CH1CH2}$ | CLKOUTA Rise Time (1.0 to 3.5 V) | | 3 | | 3 | ns |
| 46 | $t_{CL2CL1}$ | CLKOUTA Fall Time (3.5 to 1.0 V) | | 3 | | 3 | ns |
| 61 | $t_{LOCK}$ | Maximum PLL Lock Time | | 1 | | 1 | ms |
| 69 | $t_{CICOA}$ | X1 to CLKOUTA Skew | | 15 | | 15 | ns |
| 70 | $t_{CICOB}$ | X1 to CLKOUTB Skew | | 25 | | 25 | ns |

***Notes:***

*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

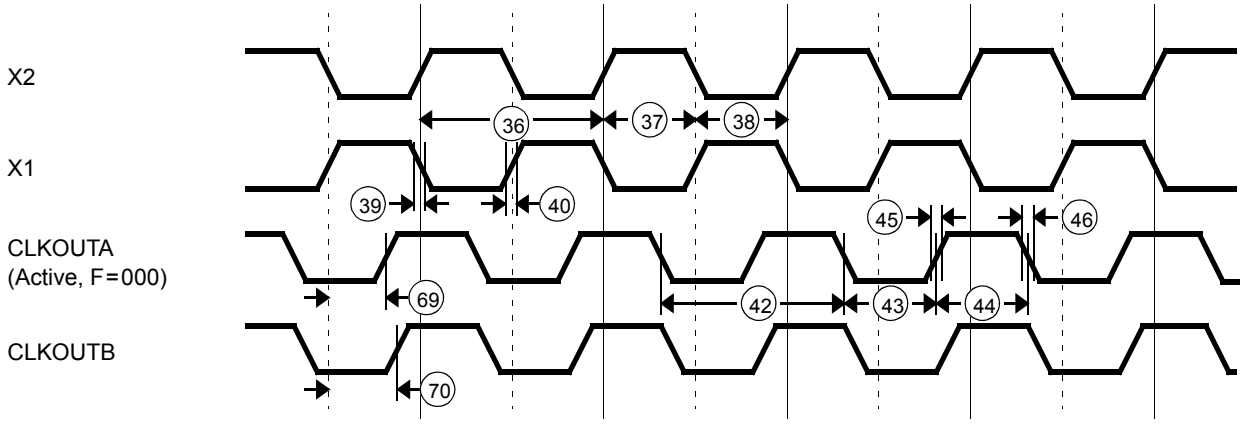
*a The specifications for CLKIN are applicable to the normal PLL and CLKDIV2 modes.*

*The PLL should be used for operations from 16.667 MHz to 40 MHz. For operations below 16.667 MHz, the CLKDIV2 mode should be used.*

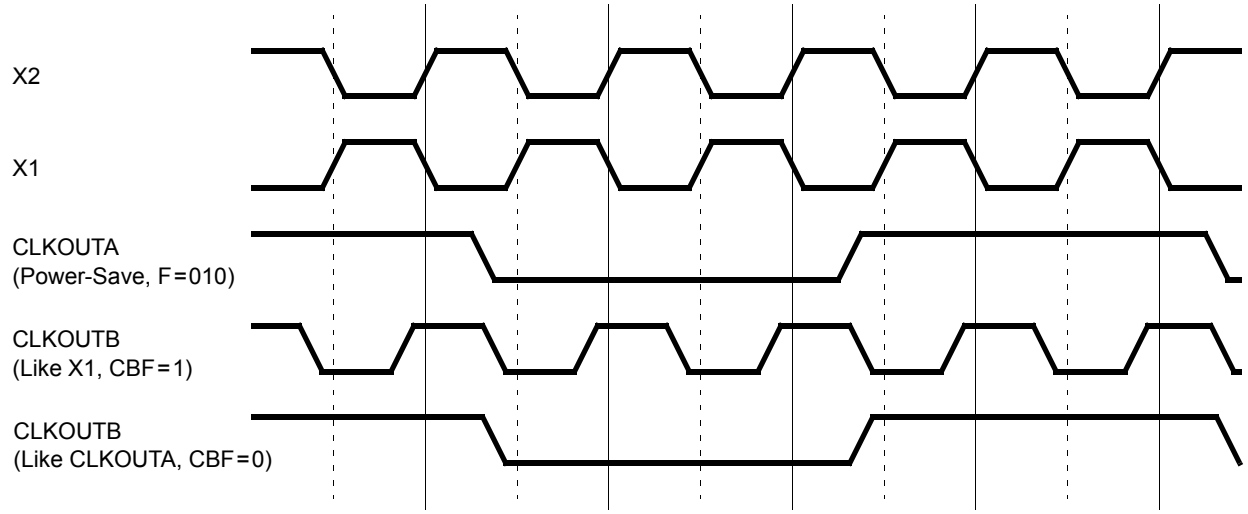
*Because the CLKDIV2 input frequency is two times the system frequency, the specifications for twice the frequency should used for CLKDIV2 mode. For example, use the 20 MHz CLKIN specifications for 10 MHz operation.*

## CLOCK WAVEFORMS

### Clock Waveforms—Active Mode




### Clock Waveforms—Power-Save Mode



## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

## Ready and Peripheral (20 MHz and 25 MHz)

| Parameter | | | Preliminary 20 MHz | | Preliminary 25 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| No. | Symbol | Description | Min | Max | Min | Max | |
| **Ready and Peripheral Timing Requirements** | | | | | | | |
| 47 | $t_{SRYCL}$ | SRDY Transition Setup Time[a] | 10 | | 10 | | ns |
| 48 | $t_{CLSRY}$ | SRDY Transition Hold Time[a] | 3 | | 3 | | ns |
| 49 | $t_{ARYCH}$ | ARDY Resolution Transition Setup Time[b] | 10 | | 10 | | ns |
| 50 | $t_{CLARX}$ | ARDY Active Hold Time[a] | 4 | | 4 | | ns |
| 51 | $t_{ARYCHL}$ | ARDY Inactive Holding Time | 6 | | 6 | | ns |
| 52 | $t_{ARYLCL}$ | ARDY Setup Time[a] | 15 | | 15 | | ns |
| 53 | $t_{INVCH}$ | Peripheral Setup Time[b] | 10 | | 10 | | ns |
| 54 | $t_{INVCL}$ | DRQ Setup Time[b] | 10 | | 10 | | ns |
| **Peripheral Timing Responses** | | | | | | | |
| 55 | $t_{CLTMV}$ | Timer Output Delay | | 25 | | 20 | ns |

***Notes:***

*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a This timing must be met to guarantee proper operation.*

*b This timing must be met to guarantee recognition at the clock edge.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges

## Ready and Peripheral (33 MHz and 40 MHz)

| Parameter | | | Preliminary 33 MHz | | Preliminary 40 MHz | | Unit |
|---|---|---|---|---|---|---|---|
| No. | Symbol | Description | Min | Max | Min | Max | |
| **Ready and Peripheral Timing Requirements** | | | | | | | |
| 47 | $t_{SRYCL}$ | SRDY Transition Setup Time[a] | 8 | | 5 | | ns |
| 48 | $t_{CLSRY}$ | SRDY Transition Hold Time[a] | 3 | | 2 | | ns |
| 49 | $t_{ARYCH}$ | ARDY Resolution Transition Setup Time[b] | 8 | | 5 | | ns |
| 50 | $t_{CLARX}$ | ARDY Active Hold Time[a] | 4 | | 3 | | ns |
| 51 | $t_{ARYCHL}$ | ARDY Inactive Holding Time | 6 | | 5 | | ns |
| 52 | $t_{ARYLCL}$ | ARDY Setup Time[a] | 10 | | 5 | | ns |
| 53 | $t_{INVCH}$ | Peripheral Setup Time[b] | 8 | | 5 | | ns |
| 54 | $t_{INVCL}$ | DRQ Setup Time[b] | 8 | | 5 | | ns |
| **Peripheral Timing Responses** | | | | | | | |
| 55 | $t_{CLTMV}$ | Timer Output Delay | | 15 | | 12 | ns |

***Notes:***

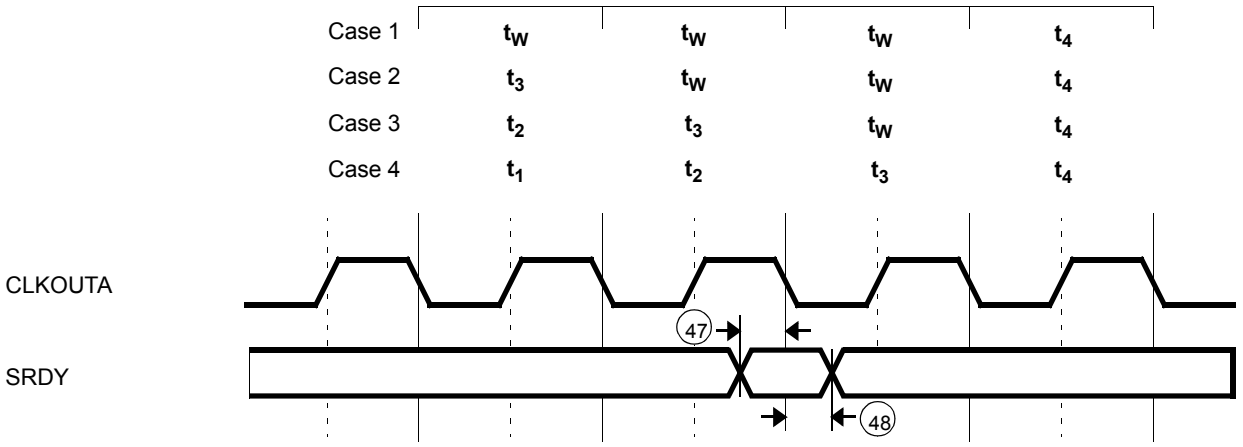
*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

*a This timing must be met to guarantee proper operation.*

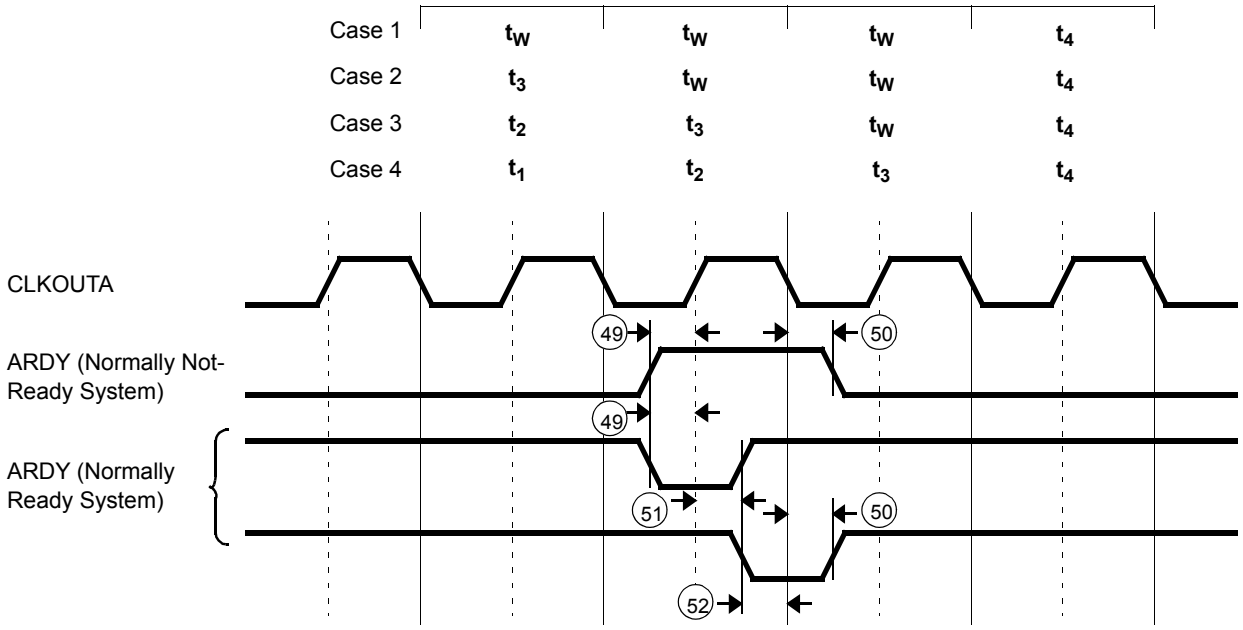
*b This timing must be met to guarantee recognition at the clock edge.*

## SYNCHRONOUS, ASYNCHRONOUS, and PERIPHERAL WAVEFORMS

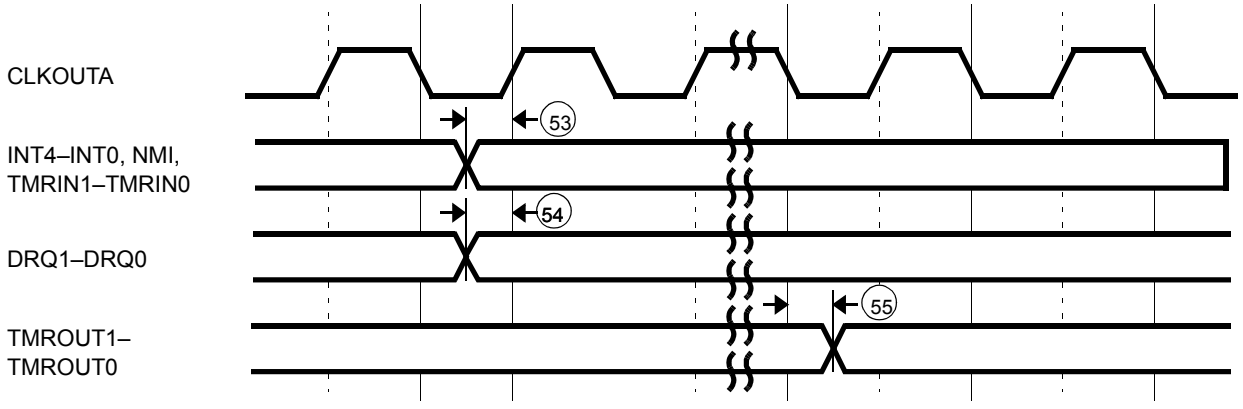
### Synchronous Ready Waveforms




### Asynchronous Ready Waveforms




### Peripheral Waveforms



## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges
## Reset and Bus Hold (20 MHz and 25 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 20 MHz | | 25 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **Reset and Bus Hold Timing Requirements** | | | | | | | |
| 5 | $t_{CLAV}$ | AD Address Valid Delay and BHE | 0 | 25 | 0 | 20 | ns |
| 15 | $t_{CLAZ}$ | AD Address Float Delay | 0 | 25 | 0 | 20 | ns |
| 57 | $t_{RESIN}$ | $\overline{RES}$ Setup Time | 10 | | 10 | | ns |
| 58 | $t_{HVCL}$ | HOLD Setup[a] | 10 | | 10 | | ns |
| **Reset and Bus Hold Timing Responses** | | | | | | | |
| 62 | $t_{CLHAV}$ | HLDA Valid Delay | 0 | 25 | 0 | 20 | ns |
| 63 | $t_{CHCZ}$ | Command Lines Float Delay | | 25 | | 20 | ns |
| 64 | $t_{CHCV}$ | Command Lines Valid Delay (after Float) | | 25 | | 20 | ns |

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges
## Reset and Bus Hold (33 MHz and 40 MHz)

| Parameter | | | Preliminary | | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | 33 MHz | | 40 MHz | | |
| No. | Symbol | Description | Min | Max | Min | Max | |
| **Reset and Bus Hold Timing Requirements** | | | | | | | |
| 5 | $t_{CLAV}$ | AD Address Valid Delay and BHE | 0 | 15 | 0 | 12 | ns |
| 15 | $t_{CLAZ}$ | AD Address Float Delay | 0 | 15 | 0 | 12 | ns |
| 57 | $t_{RESIN}$ | $\overline{RES}$ Setup Time | 8 | | 5 | | ns |
| 58 | $t_{HVCL}$ | HOLD Setup[a] | 8 | | 5 | | ns |
| **Reset and Bus Hold Timing Responses** | | | | | | | |
| 62 | $t_{CLHAV}$ | HLDA Valid Delay | 0 | 15 | 0 | 12 | ns |
| 63 | $t_{CHCZ}$ | Command Lines Float Delay | | 15 | | 12 | ns |
| 64 | $t_{CHCV}$ | Command Lines Valid Delay (after Float) | | 15 | | 12 | ns |

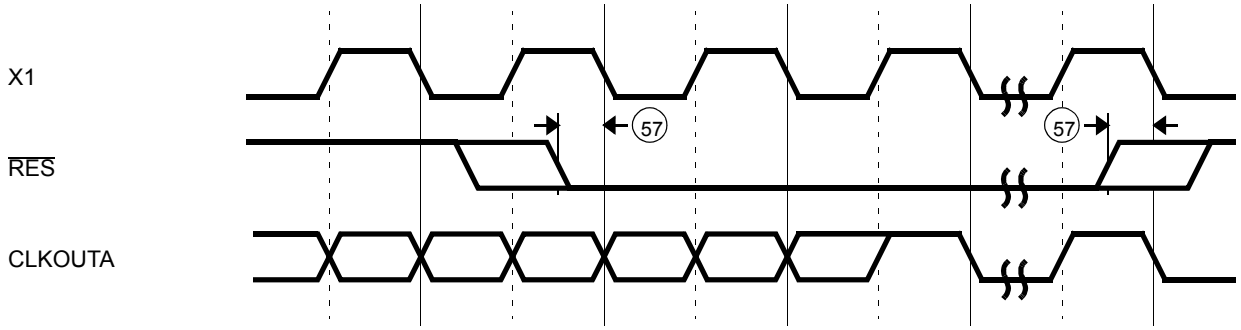
***Notes:***

*All timing parameters are measured at 1.5 V with 50 pF loading on CLKOUTA, unless otherwise noted. All output test conditions are with $C_L$ =50 pF. For switching tests, $V_{IL}$ =0.45 V and $V_{IH}$ =2.4 V, except at X1 where $V_{IH}=V_{CC}-0.5$ V.*

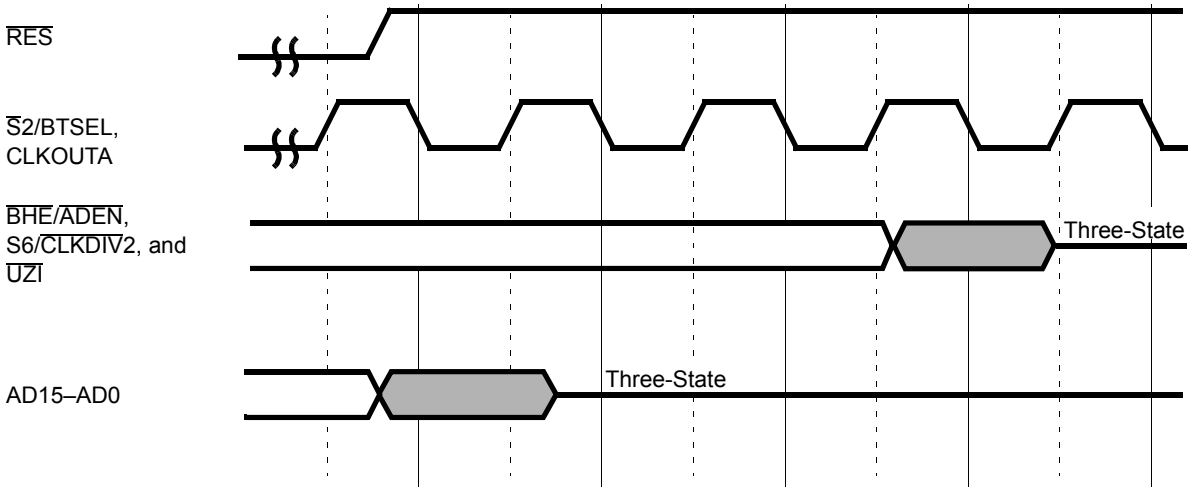
*a This timing must be met to guarantee recognition at the next clock.*

## RESET and BUS HOLD WAVEFORMS

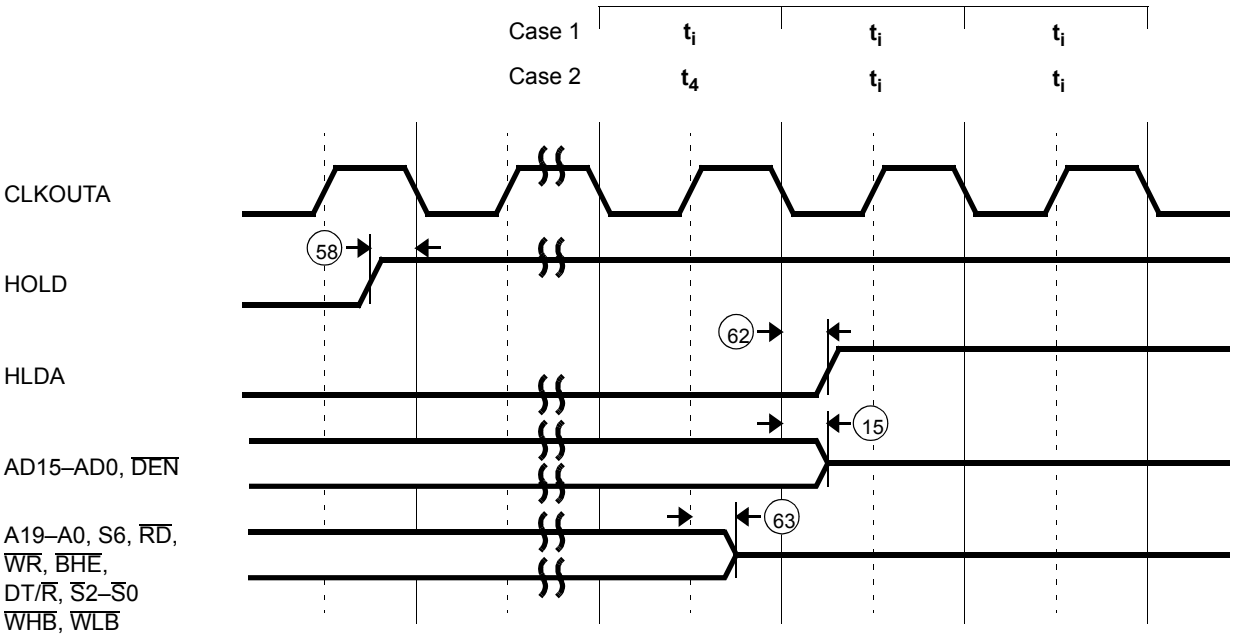
### Reset Waveforms




### Signals Related to Reset Waveforms



## Bus Hold Waveforms—Entering




## Bus Hold Waveforms—Leaving