HARRIS

2N6755
2N6756

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

- 12A and 14A, 60V - 100V
- $r_{DS(on)}$ = 0.18Ω and 0.25Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

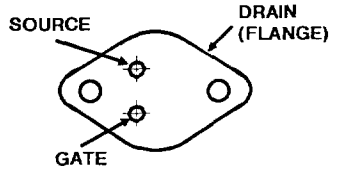
Description

The 2N6755 and 2N6756 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

These types are supplied in the JEDEC TO-204AA steel package.

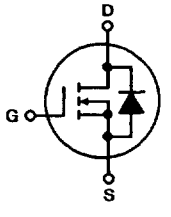
Package

TO-204AA
BOTTOM VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C) Unless Otherwise Specified

		2N6755	2N6756	UNITS
Drain-Source Voltage	V_{DS}	60*	100*	V
Drain-Gate Voltage (R_{GS} = 20kΩ)	V_{DGR}	60*	100*	V
Continuous Drain Current				
T_C = +25°C	I_D	12*	14*	A
T_C = +100°C	I_D	8.0*	9.0*	A
Pulsed Drain Current	I_{DM}	25	30	A
Gate-Source Voltage	V_{GS}	±20	±20	V
Maximum Power Dissipation				
T_C = +25°C (See Fig. 11)	P_D	75*	75*	W
T_C = +100°C (See Fig. 11)	P_D	30*	30*	W
Linear Derating Factor (See Fig. 11)		0.6*	0.6*	W/°C
Inductive Current, Clamped (See Figures 1 and 2, L = 100μH)	I_{LM}	25	30	A
Operating and Storage Junction Temperature Range	T_J, T_{STG}	-55 to +150*	-55 to +150*	°C
Maximum Lead Temperature for Soldering (0.063" (1.6mm) from case for 10s)	T_L	300*	300*	°C

*JEDEC registered values

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number 1586.1

Electrical Characteristics @ T_C = 25°C (Unless Otherwise Specified)

Parameter		Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain – Source Breakdown Voltage	2N6755	60	–	–	V	V_{GS} = 0
		2N6756	100	–	–	V	I_D = 1.0 mA
$V_{GS(th)}$	Gate Threshold Voltage	ALL	2.0*	–	4.0*	V	V_{DS} = V_{GS}, I_D = 1 mA
I_{GSSF}	Gate – Body Leakage Forward	ALL	–	–	100*	nA	V_{GS} = 20V
I_{GSSR}	Gate – Body Leakage Reverse	ALL	–	–	100*	nA	V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	ALL	–	0.1	1.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0
			–	0.2	4.0*	mA	V_{DS} = Max. Rating, V_{GS} = 0, T_C = 125°C
$V_{DS(on)}$	Static Drain-Source On-State Voltage ①	2N6755	–	–	3.0*	V	V_{GS} = 10V, I_D = 12A
		2N6756	–	–	2.52*	V	V_{GS} = 10V, I_D = 14A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6755	–	0.20	0.25*	Ω	V_{GS} = 10V, I_D = 8A
		2N6756	–	0.14	0.18*	Ω	V_{GS} = 10V, I_D = 9A
$R_{DS(on)}$	Static Drain-Source On-State Resistance ①	2N6755	–	–	0.45*	Ω	V_{GS} = 10V, I_D = 8A, T_C = 125°C
		2N6756	–	–	0.33*	Ω	V_{GS} = 10V, I_D = 9A, T_C = 125°C
g_{fs}	Forward Transconductance ①	ALL	4.0*	5.5	12.0*	S (℧)	V_{DS} = 15V, I_D = 9A
C_{iss}	Input Capacitance	ALL	350*	600	800*	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz See Fig. 10
C_{oss}	Output Capacitance	ALL	150*	300	500*	pF	
C_{rss}	Reverse Transfer Capacitance	ALL	50*	100	150*	pF	
$t_{d(on)}$	Turn-On Delay Time	ALL	–	–	30*	ns	V_{DD} ≅ 36V, I_D = 9A, Z_o = 15Ω
t_r	Rise Time	ALL	–	–	75*	ns	(See Figs. 13 and 14)
$t_{d(off)}$	Turn-Off Delay Time	ALL	–	–	40*	ns	(MOSFET switching times are essentially
t_f	Fall Time	ALL	–	–	45*	ns	independent of operating temperature.)

Thermal Resistance

R_{thJC}	Junction-to-Case	ALL	–	–	1.67*	°C/W	
R_{thCS}	Case-to-Sink	ALL	–	0.1	–	°C/W	Mounting surface flat, smooth, and greased.
R_{thJA}	Junction-to-Ambient	ALL	–	–	30	°C/W	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S	Continuous Source Current (Body Diode)	2N6755	–	–	12*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier.
		2N6756	–	–	14*		
I_{SM}	Pulsed Source Current (Body Diode)	2N6755	–	–	25	A	
		2N6756	–	–	30		
V_{SD}	Diode Forward Voltage ①	2N6755	0.85*	–	1.7*	V	T_C = 25°C, I_S = 12A, V_{GS} = 0
		2N6756	0.90*	–	1.8*	V	T_C = 25°C, I_S = 14A, V_{GS} = 0
t_{rr}	Reverse Recovery Time	ALL		300		ns	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs
Q_{RR}	Reverse Recovered Charge	ALL	–	4.0	–	μC	T_J = 150°C, I_F = I_{SM}, dI_F/dt = 100 A/μs

*JEDEC registered values ① Pulse Test: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%

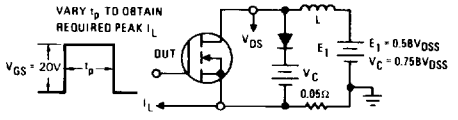


Fig. 1 – Clamped Inductive Test Circuit

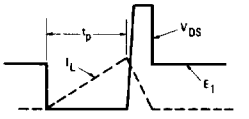


Fig. 2 – Clamped Inductive Waveforms

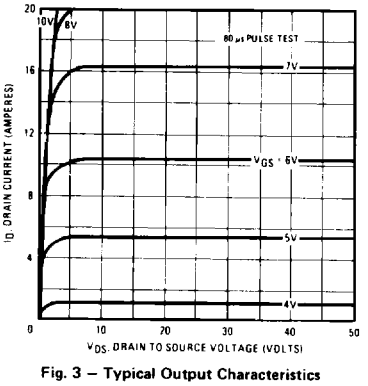


Fig. 3 – Typical Output Characteristics

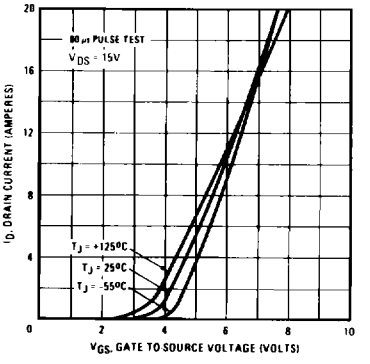


Fig. 4 – Typical Transfer Characteristics

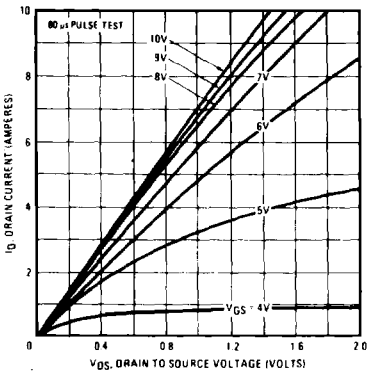


Fig. 5— Typical Saturation Characteristics (2N6755)

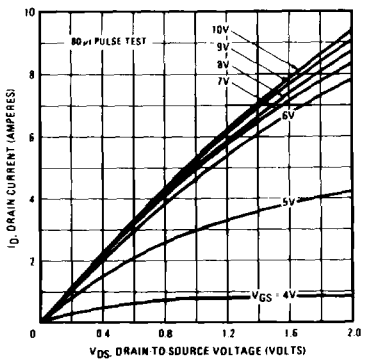


Fig. 6— Typical Saturation Characteristics (2N6756)

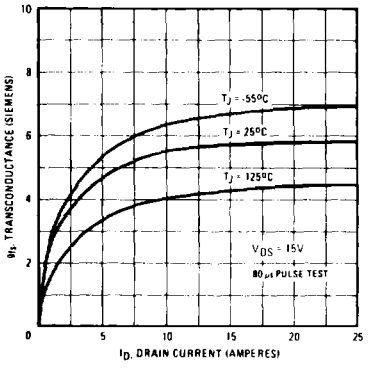


Fig. 7 — Typical Transconductance Vs. Drain Current

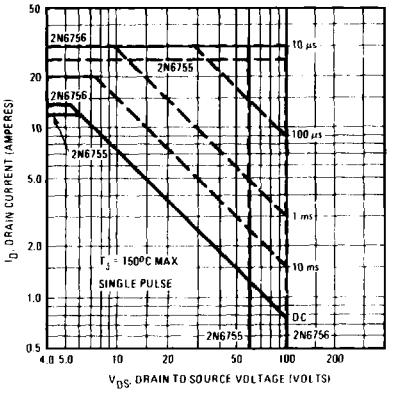


Fig. 8 — Maximum Safe Operating Area

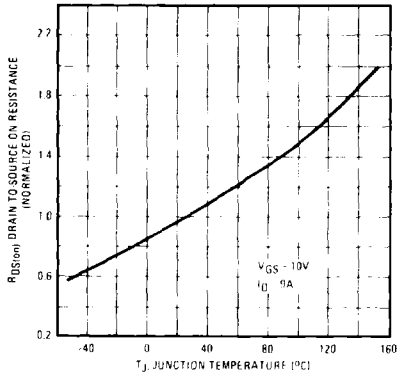


Fig. 9 — Normalized Typical On-Resistance Vs. Temperature

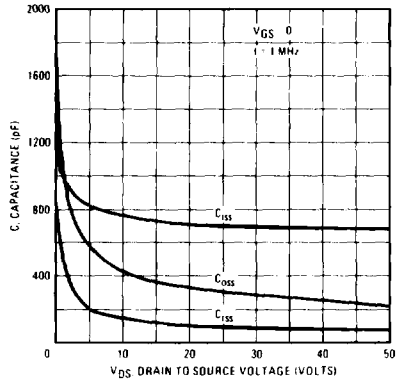


Fig. 10 — Typical Capacitance Vs. Drain-to-Source Voltage

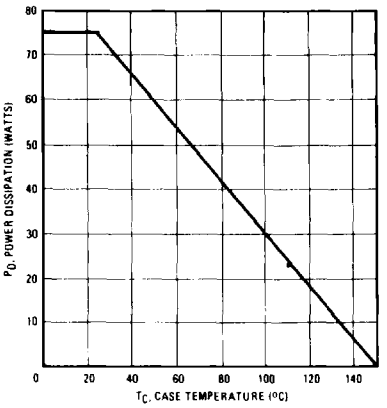


Fig. 11 – Power Vs. Temperature Derating Curve

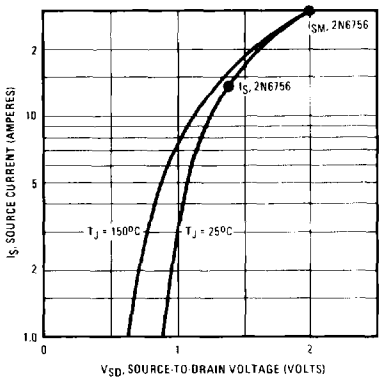


Fig. 12 – Typical Body-Drain Diode Forward Voltage

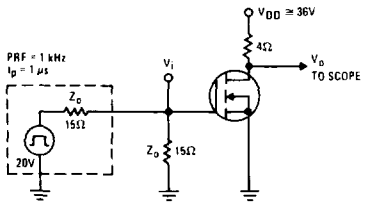


Fig. 13 – Switching Time Test Circuit

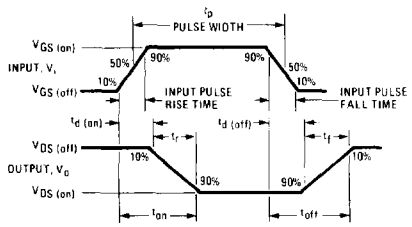


Fig. 14 – Switching Time Waveforms