MC7660

Charge Pump DC-to-DC Voltage Converter

The MC7660 is a pin-compatible replacement for the Industry standard ICL7660 charge pump voltage converter. It converts a +1.5 V to +10 V input to a corresponding -1.5 V to -10 V output using only two low-cost capacitors, eliminating inductors and their associated cost, size and EMI.

The on-board oscillator operates at a nominal frequency of 10 kHz. Operation below 10 kHz (for lower supply current applications) is possible by connecting an external capacitor from OSC to ground (with pin 1 open).

The MC7660 is available in an 8-pin SOIC package in extended temperature range.

Features

- Converts +5.0 V Supply to -5.0 V Supply
- Wide Input Voltage Range: 1.5 V to 10 V
- Efficient Voltage Conversion: 99.9%
- Excellent Power Efficiency: 98%
- Low Power Supply: 80 μA @ 5.0 V_{IN}
- Low Cost and Easy to Use
  - Only Two External Capacitors Required
- Available in Small Outline (SO) Package
- ESD Protection: ≥ 2.5 kV
- No Dx Diode Required for High Voltage Operation

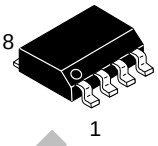
Typical Applications

- RS-232 Negative Bias
- Display Bias
- Data Acquisition Negative Supply Generation

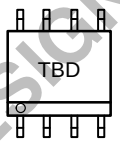
ON Semiconductor®

http://onsemi.com

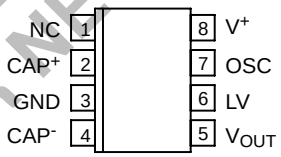
MARKING DIAGRAM



SO-8
D SUFFIX
CASE 751



PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
MC7660DR2	8-Pin SOIC	2500 Tape/Reel

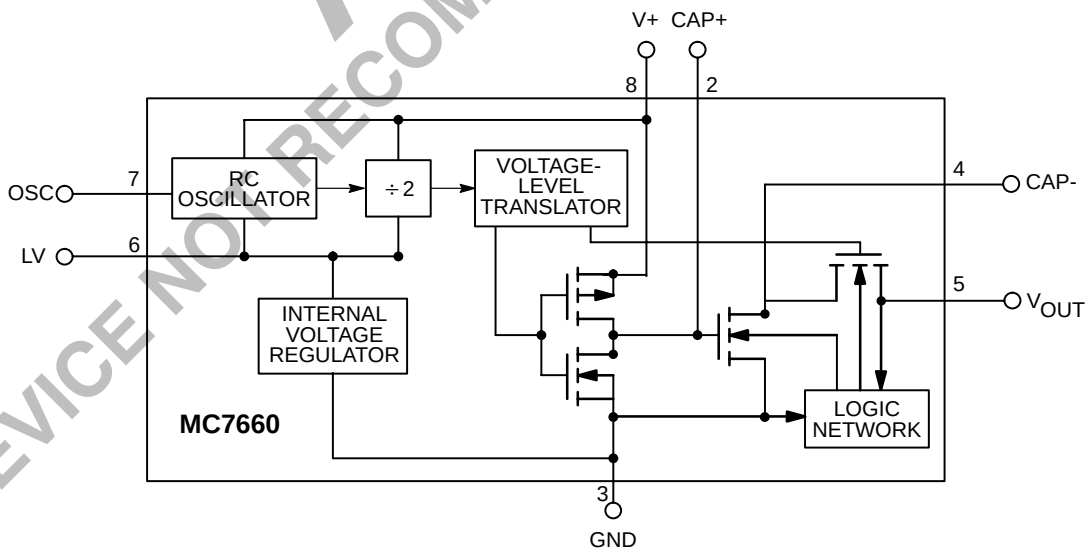


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS*

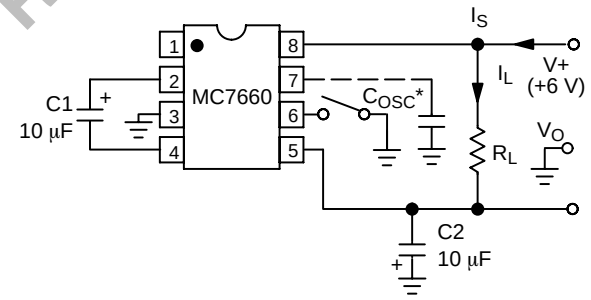
Rating	Value	Unit
Supply Voltage	+10.5	V
LV and OSC Inputs Voltage (Note 1.) $V^+ < 5.5$ V $V^+ > 5.5$ V	 -0.3 to (V^+ + 0.3) (V^+ - 5.5) to (V^+ + 0.3)	V
Current Into LV (Note 1.) $V^+ > 3.5$ V	20	μA
Output Short Duration ($V_{SUPPLY} \le 5.5$ V)	Continuous	
Power Dissipation ($T_A \le 70°C$) Derate above 50°C	470 5.5	mW mW/°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
Lead Temperature (Soldering, 10 Seconds)	+300	°C

*Maximum Ratings are those values beyond which damage to the device may occur.

ELECTRICAL CHARACTERISTICS (Specifications Measured Over Operating Temperature Range, $V^+ = 5.0$ V,$C_{OSC} = 0$, Test Circuit (Figure 2), unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Current ($R_L = \infty$)	I^+	-	80	180	μA
Supply Voltage Range, High (-40 °C ≤ T_A ≤ +85°C, R_L = 10 kΩ, LV Open)	V^+_H	 3.0	 -	 10	V
Supply Voltage Range, Low (-40 °C ≤ T_A ≤ +85°C, R_L = 10 kΩ, LV to GND)	V^+_L	 1.5	 -	 3.5	V
Output Source Resistance I_{OUT} = 20 mA, T_A = 25°C I_{OUT} = 20 mA, 0°C ≤ T_A ≤ +70°C I_{OUT} = 20 mA, -40°C ≤ T_A ≤ +85°C V^+ = 2.0 V, I_{OUT} = 3.0 mA, LV to GND, 0°C ≤ T_A ≤ +70°C	R_{OUT}	 - - - -	 70 - - 150	 100 120 130 300	Ω
Oscillator Frequency (Pin 7 Open)	F_{OSC}	-	10	-	kHz
Power Efficiency (R_L = 5.0 kΩ)	P_{EFF}	95	98	-	%
Voltage Conversion Efficiency	V_{OUT} E_{FF}	97	99.9	-	%
Oscillator Impedance V^+ = 2.0 V V^+ = 5.0 V	Z_{OSC}	 - -	 1000 100	 - -	kΩ

1. Connecting any input terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to “power up” of the MC7660.



*NOTE: For large values of C_{OSC} (>1000 pF), the values of C1 and C2 should be increased to 100 μF.

Figure 2. MC7660 Test Circuit

APPLICATIONS INFORMATION

Detailed Description

The MC7660 contains all the necessary circuitry to implement a voltage inverter, with the exception of two external capacitors, which may be inexpensive 10 μF polarized electrolytic capacitors. Operation is best understood by considering Figure 3, which shows an idealized voltage inverter. Capacitor C_1 is charged to a voltage, V^+, for the half cycle when switches S_1 and S_3 are closed. (**Note:** Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2, such that the voltage on C_2 is exactly V^+, assuming ideal switches and no load on C_2.

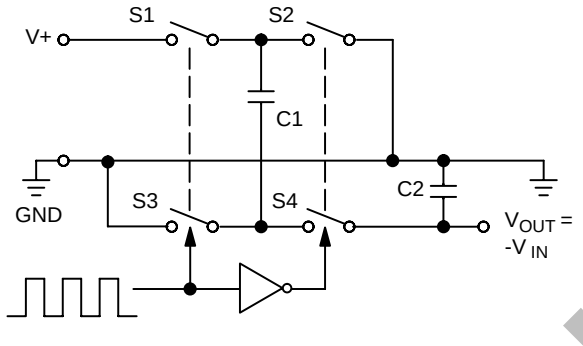


Figure 3. Idealized Charge Pump Inverter

The four switches in Figure 3 are MOS power switches; S_1 is a P-channel device, and S_2, S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistances. In addition, at circuit start-up, and under output short circuit conditions ($V_{OUT} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up.

This problem is eliminated in the MC7660 by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the MC7660 is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can, however, degrade operation at low voltages. To improve low-voltage operation, the LV pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5 V, the LV terminal must be left open to ensure latch-up-proof operation and prevent device damage.

Theoretical Power Efficiency Considerations

In theory, a capacitive charge pump can approach 100% efficiency if certain conditions are met:

(1) The drive circuitry consumes minimal power.

(2) The output switches have extremely low ON resistance and virtually no offset.

(3) The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The MC7660 approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. **Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs.** The energy lost is defined by:

$$E = 1/2\ C_1\ (V_1^2 — V_2^2)$$

V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 3), compared to the value of R_L, there will be a substantial difference in voltages V_1 and V_2. Therefore, it is not only desirable to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

Dos and Don'ts

- Do not exceed maximum supply voltages.
- Do not connect LV terminal to GND for supply voltages greater than 3.5 V.
- Do not short circuit the output to V^+ supply for voltages above 5.5 V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of C_1 must be connected to pin 2 of the MC7660 and the + terminal of C_2 must be connected to GND Pin 3.

Simple Negative Voltage Converter

Figure 4 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5 V to +10 V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5 V.

The output characteristics of the circuit in Figure 4 are those of a nearly ideal voltage source in series with 70 Ω. Thus, for a load current of -10 mA and a supply voltage of +5.0 V, the output voltage would be -4.3 V.

The dynamic output impedance of the MC7660 is due, primarily, to capacitive reactance of the charge transfer capacitor (C_1). Since this capacitor is connected to the output for only 1/2 of the cycle, the equation is:

$$X_C = \frac{2}{2\pi f C_1} = 3.18\Omega,$$

where f = 10kHz and C_1 = 10μF.

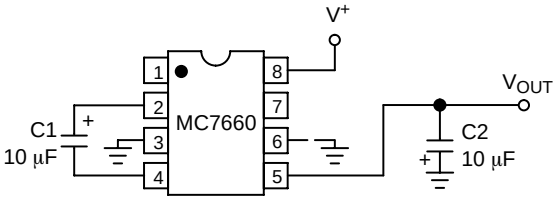


Figure 4. Simple Negative Converter

Parallel Devices

Any number of MC7660 voltage converters may be paralleled to reduce output resistance (Figure 5). The reservoir capacitor, C_2, serves all devices, while each device requires its own pump capacitor, C_1. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT}\text{ (of MC7660)}}{\text{n (number of devices)}}$$

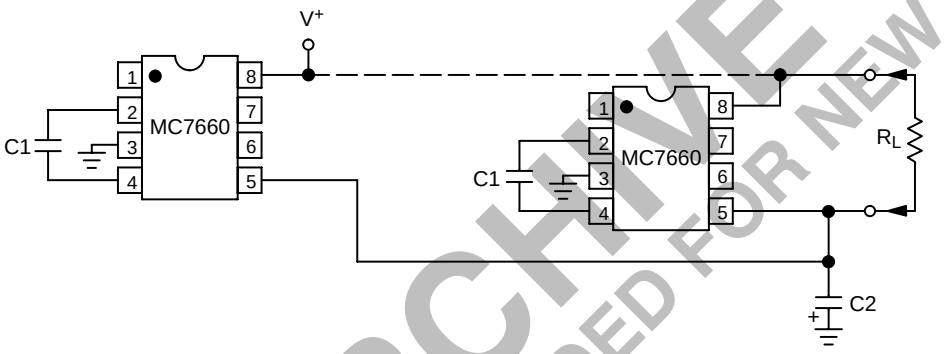


Figure 5. Paralleling Devices Lowers Output Impedance

Cascading Devices

The MC7660 may be cascaded as shown (Figure 6) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n\ (V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual MC7660 R_{OUT} values.

Changing the MC7660 Oscillator Frequency

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. This is achieved by overdriving the oscillator from an external clock, as shown in Figure 7. In order to prevent possible device latch-up, a 1.0 kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10 kΩ pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the MC7660 at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC}, as shown in Figure 8. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this, increase the values of C_1 and C_2 by the same factor that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (OSC) and pin 8 (V^+) will lower the oscillator frequency to 1.0 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the values of C_1 and C_2 (from 10 μF to 100 μF).

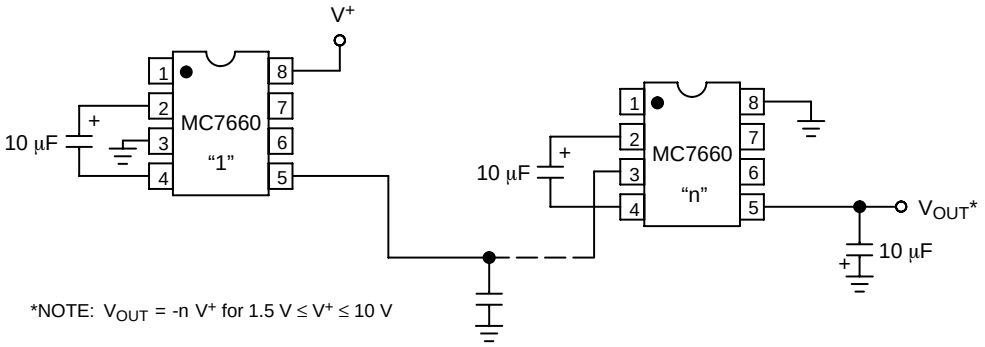


Figure 6. Increased Output Voltage by Cascading Devices

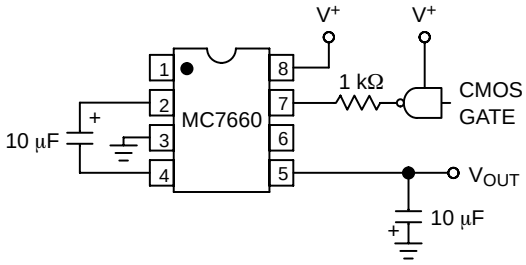


Figure 7. External Clocking

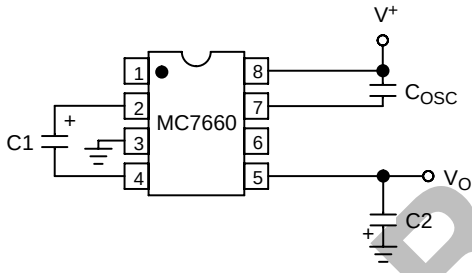


Figure 8. Lowering Oscillator Frequency

Positive Voltage Multiplication

The MC7660 may be employed to achieve positive voltage multiplication using the circuit shown in Figure 9. In this application, the pump inverter switches of the MC7660 are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2. The voltage thus created on C_2 becomes $(2.0\ V^+) - (2.0\ V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2.

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5.0$ V and an output current of 10 mA, it will be approximately 60 Ω.

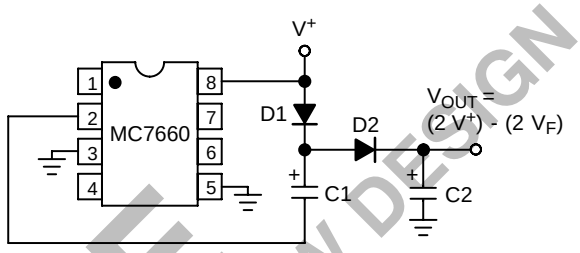


Figure 9. Positive Voltage Multiplier

Combined Negative Voltage Conversion and Positive Supply Multiplication

Figure 10 combines the functions shown in Figures 4 and 9 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be, for example, suitable for generating +9.0 V and -5.0 V from an existing +5.0 V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir functions, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

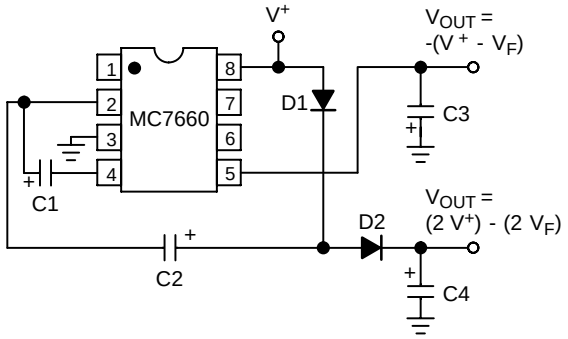


Figure 10. Combined Negative Converter and Positive Multiplier

Efficient Positive Voltage Multiplication/Conversion

Since the switches that allow the charge pumping operation are bidirectional, the charge transfer can be performed backwards as easily as forwards. Figure 11 shows a MC7660 transforming -5.0 V to +5.0 V (or +5.0 V to +10 V, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 10, could be used to start this circuit up, after which it will bypass the other (D_1 and D_2 in Figure 10 would never turn on), or else the diode and resistor shown dotted in Figure 11 can be used to “force” the internal regulator on.

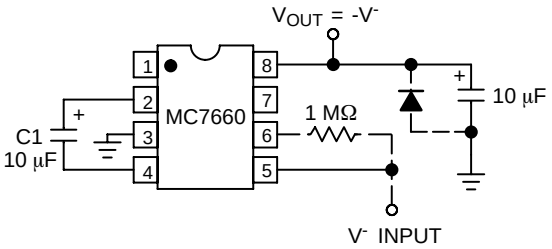


Figure 11. Positive Voltage Conversion

Voltage Splitting

The same bidirectional characteristics used in Figure 11 can also be used to split a higher supply in half, as shown in Figure 12. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 6, +15 V can be converted (via +7.5 V and -7.5 V) to a nominal -15 V, though with rather high series resistance (~250 Ω).

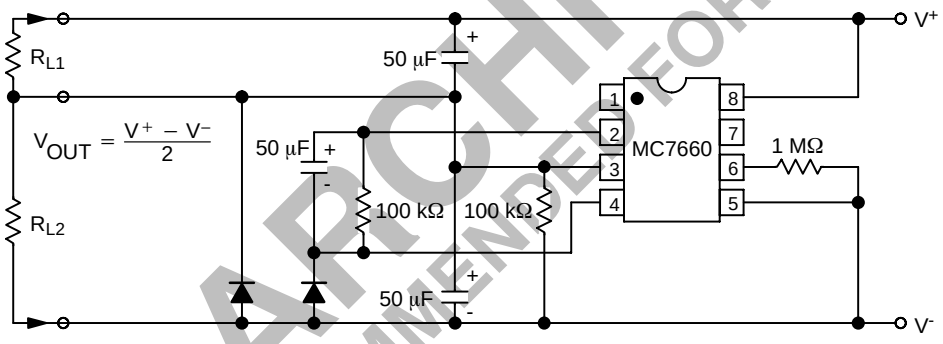


Figure 12. Splitting a Supply in Half

TYPICAL PERFORMANCE CHARACTERISTICS

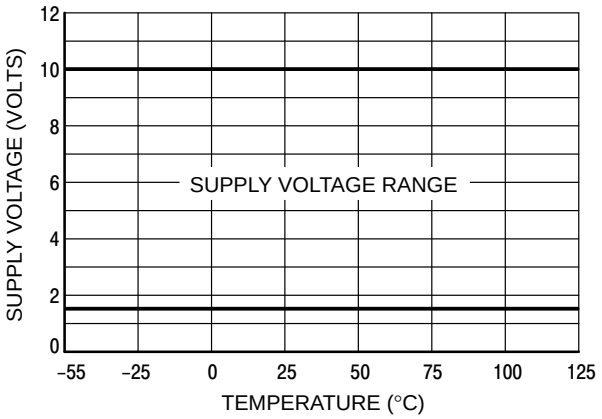


Figure 13. Operating Voltage versus Temperature

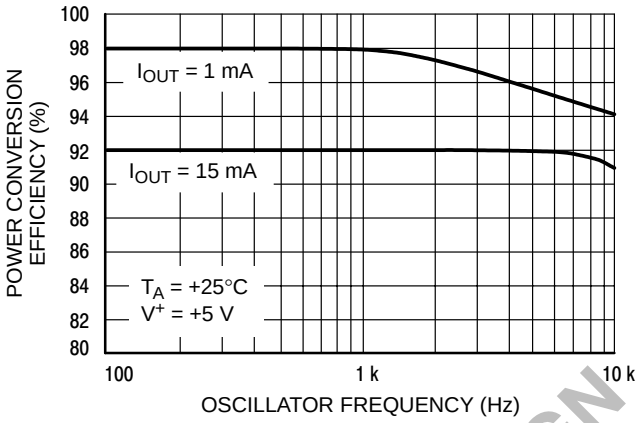


Figure 14. Power Conversion Efficiency versus Oscillator Frequency

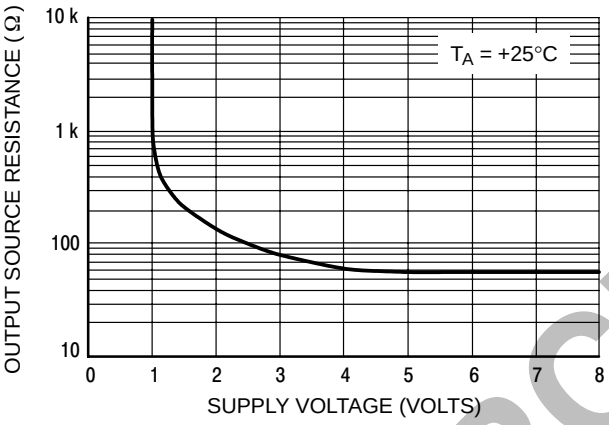


Figure 15. Output Source Resistance versus Supply Voltage

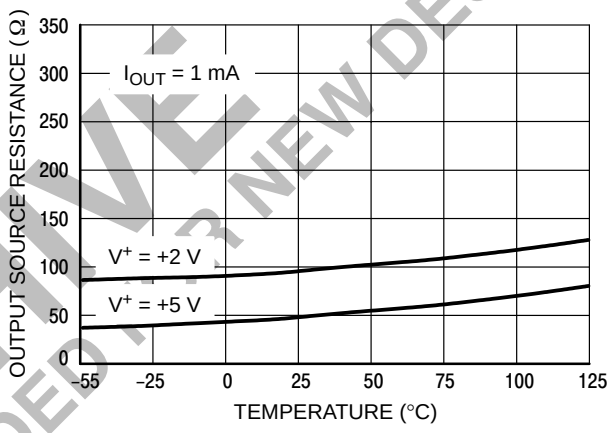


Figure 16. Output Source Resistance versus Temperature

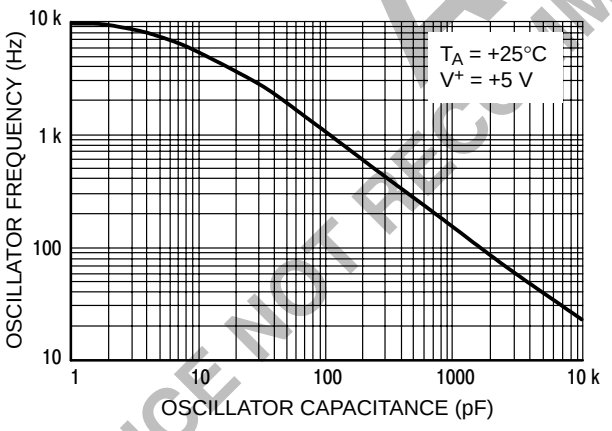


Figure 17. Frequency of Oscillation versus Oscillator Capacitance

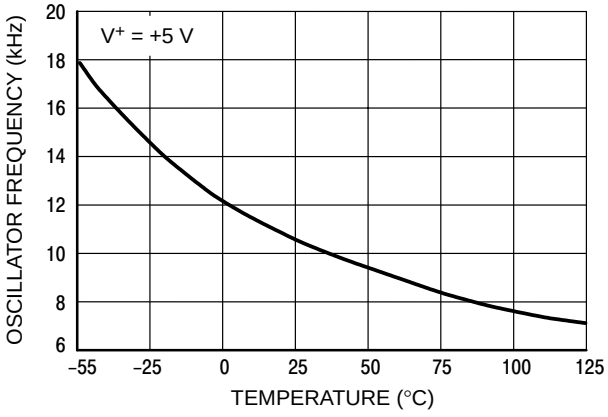


Figure 18. Unloaded Oscillator Frequency versus Temperature

TYPICAL CHARACTERISTICS (Cont.)

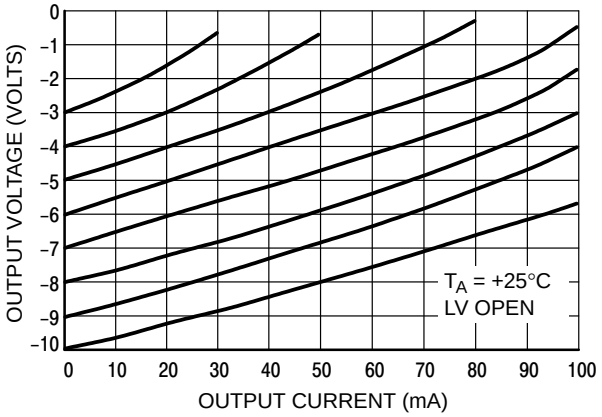


Figure 19. Output Voltage versus Output Current

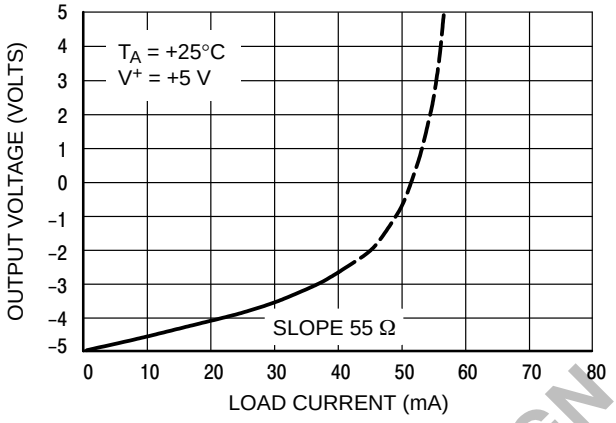


Figure 20. Output Voltage versus Load Current

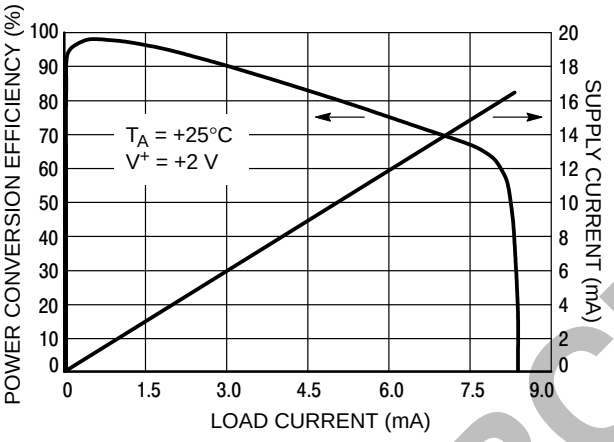


Figure 21. Supply Current and Power Conversion Efficiency versus Load Current

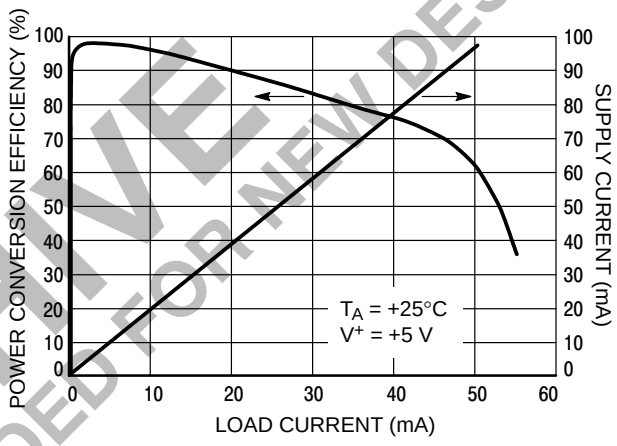


Figure 22. Supply Current and Power Conversion Efficiency versus Load Current

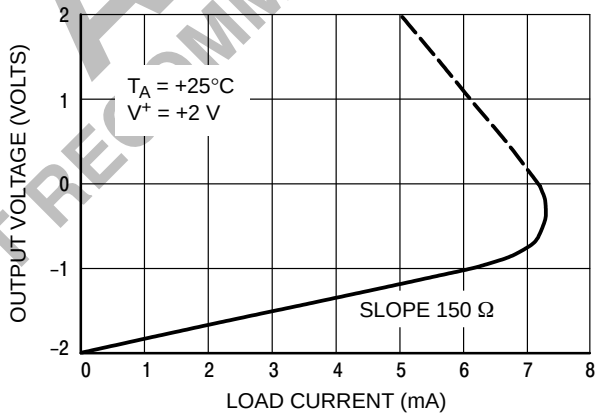
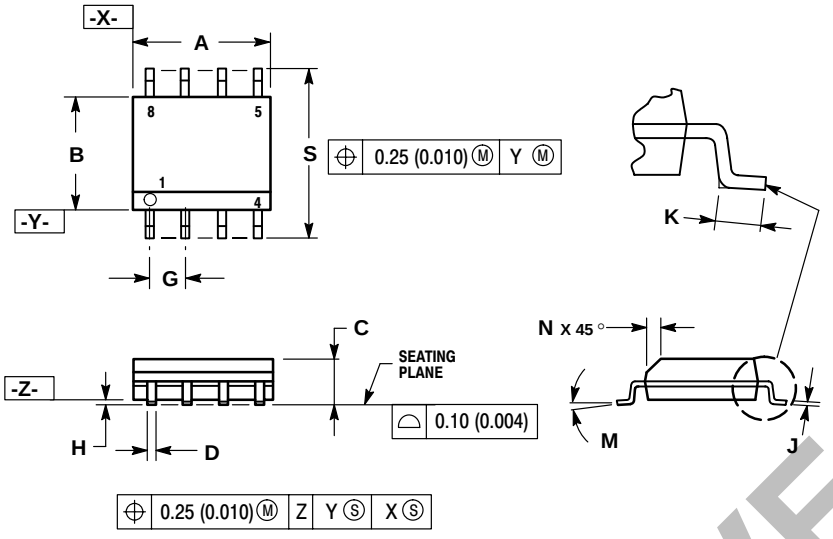


Figure 23. Output Voltage versus Load Current

PACKAGE DIMENSIONS

8-Pin SOIC
D SUFFIX
CASE 751-07
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751–01 THRU 751–06 ARE OBSOLETE. NEW STANDARD IS 751–07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

PUBLICATION ORDERING INFORMATION

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Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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