

N-Channel Enhancement-Mode Power Field-Effect Transistors

August 1991

Features

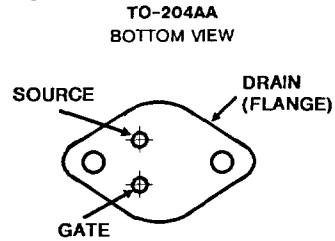
- 8A and 9A, 150V - 200V
- $r_{DS(on)} = 0.4\Omega$ and 0.6Ω
- SOA is Power-Dissipation Limited
- Nanosecond Switching Speeds
- Linear Transfer Characteristics
- High Input Impedance
- Majority Carrier Device

Description

The 2N6757 and 2N6758 are n-channel enhancement-mode silicon-gate power field-effect transistors designed for applications such as switching regulators, switching converters, motor drivers, relay drivers, and drivers for high-power bipolar switching transistors requiring high speed and low gate-drive power. These types can be operated directly from integrated circuits.

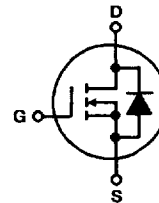
These types are supplied in the JEDEC TO-204AA steel package.

Package



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings ($T_C = +25^\circ\text{C}$) Unless Otherwise Specified

	2N6757	2N6758	UNITS
Drain-Source Voltage	150*	200*	V
Drain-Gate Voltage ($R_{GS} = 20k\Omega$)	150*	200*	V
Continuous Drain Current			
$T_C = +25^\circ\text{C}$	8.0*	9.0*	A
$T_C = +100^\circ\text{C}$	5.0*	6.0*	A
Pulsed Drain Current	12	15	A
Gate-Source Voltage	± 20	± 20	V
Maximum Power Dissipation			
$T_C = +25^\circ\text{C}$ (See Figure 11)	75*	75*	W
$T_C = +100^\circ\text{C}$ (See Figure 11)	30*	30*	W
Linear Derating Factor (See Figure 11)	0.6*	0.6*	W/ $^\circ\text{C}$
Inductive Current, Clamped	12	15	A
(See Figures 1 and 2, $L = 100\mu\text{H}$)			
Operating and Storage Junction Temperature Range	-55 to $+150^*$	-55 to $+150^*$	$^\circ\text{C}$
Maximum Lead Temperature for Soldering	300*	300*	$^\circ\text{C}$
(0.063" (1.6mm) from case for 10s)			

*JEDEC registered values

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N-CHANNEL
POWER MOSFETS

Specifications 2N6757, 2N6758


Electrical Characteristics @ $T_C = 25^\circ\text{C}$ (Unless Otherwise Specified)

Parameter	Type	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS} Drain - Source Breakdown Voltage	2N6757	150	—	—	V	$V_{GS} = 0$ $I_D = 1.0 \text{ mA}$
	2N6758	200	—	—	V	
$V_{GS(th)}$ Gate Threshold Voltage	ALL	2.0*	—	4.0*	V	$V_{DS} = V_{GS}$, $I_D = 1 \text{ mA}$
I_{GSSF} Gate - Body Leakage Forward	ALL	—	—	100*	nA	$V_{GS} = 20\text{V}$
I_{GSSR} Gate - Body Leakage Reverse	ALL	—	—	100*	nA	$V_{GS} = -20\text{V}$
I_{DSS} Zero Gate Voltage Drain Current	ALL	—	0.1	1.0*	mA	$V_{DS} = \text{Max. Rating}$, $V_{GS} = 0$ $V_{DS} = \text{Max. Rating}$, $V_{GS} = 0$, $T_C = 125^\circ\text{C}$
		—	0.2	4.0*		
$V_{DS(on)}$ Static Drain-Source On-State Voltage $\text{\textcircled{1}}$	2N6757	—	—	4.8*	V	$V_{GS} = 10\text{V}$, $I_D = 8\text{A}$
	2N6758	—	—	3.6*	V	$V_{GS} = 10\text{V}$, $I_D = 9\text{A}$
$R_{DS(on)}$ Static Drain-Source On-State Resistance $\text{\textcircled{1}}$	2N6757	—	0.4	0.6*	Ω	$V_{GS} = 10\text{V}$, $I_D = 5\text{A}$
	2N6758	—	0.25	0.4*	Ω	$V_{GS} = 10\text{V}$, $I_D = 6\text{A}$
$R_{DS(on)}$ Static Drain-Source On-State Resistance $\text{\textcircled{1}}$	2N6757	—	—	1.13*	Ω	$V_{GS} = 10\text{V}$, $I_D = 5\text{A}$, $T_C = 125^\circ\text{C}$
				0.75*		$V_{GS} = 10\text{V}$, $I_D = 6\text{A}$, $T_C = 125^\circ\text{C}$
g_{fs} Forward Transconductance $\text{\textcircled{1}}$	ALL	3.0*	5.0	9.0*	S (V)	$V_{DS} = 15\text{V}$, $I_D = 6\text{A}$
C_{iss} Input Capacitance	ALL	350*	600	800*	pF	$V_{GS} = 0$, $V_{DS} = 25\text{V}$, $f = 1.0 \text{ MHz}$
C_{oss} Output Capacitance	ALL	100*	250	450*	pF	See Fig. 10
C_{rss} Reverse Transfer Capacitance	ALL	40*	80	150*	pF	
$t_{d(on)}$ Turn-On Delay Time	ALL	—	—	30*	ns	$V_{DD} \approx 90\text{V}$, $I_D = 6\text{A}$, $Z_o = 15\Omega$
t_r Rise Time	ALL	—	—	50*	ns	(See Figs. 13 and 14)
$t_{d(off)}$ Turn-Off Delay Time	ALL	—	—	50*	ns	(MOSFET switching times are essentially independent of operating temperature.)
t_f Fall Time	ALL	—	—	40*	ns	

Thermal Resistance

R_{thJC} Junction-to-Case	ALL	—	—	1.67*	$^\circ\text{C/W}$	
R_{thCS} Case-to-Sink	ALL	—	0.1	—	$^\circ\text{C/W}$	Mounting surface flat, smooth, and grinded.
R_{thJA} Junction-to-Ambient	ALL	—	—	30	$^\circ\text{C/W}$	Free Air Operation

Body-Drain Diode Ratings and Characteristics

I_S Continuous Source Current (Body Diode)	2N6757	—	—	8.0*	A	Modified MOSFET symbol showing the integral reverse P-N junction rectifier. 
	2N6758	—	—	9.0*		
I_{SM} Pulsed Source Current (Body Diode)	2N6757	—	—	12	A	
	2N6758	—	—	15		
V_{SD} Diode Forward Voltage $\text{\textcircled{1}}$	2N6757	0.75*	—	1.50*	V	$T_C = 25^\circ\text{C}$, $I_S = 8\text{A}$, $V_{GS} = 0$
	2N6758	0.80*	—	1.60*	V	$T_C = 25^\circ\text{C}$, $I_S = 9\text{A}$, $V_{GS} = 0$
t_{rr} Reverse Recovery Time	ALL	—	650	—	ns	$T_J = 150^\circ\text{C}$, $I_F = I_{SM}$, $dI_F/dt = 100 \text{ A}/\mu\text{s}$
Q_{RR} Reverse Recovered Charge	ALL	—	10	—	μC	$T_J = 150^\circ\text{C}$, $I_F = I_{SM}$, $dI_F/dt = 100 \text{ A}/\mu\text{s}$

*JEDEC registered values. $\text{\textcircled{1}}$ Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$

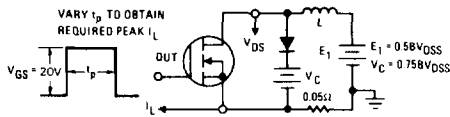


Fig. 1 - Clamped Inductive Test Circuit

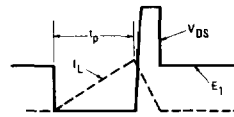


Fig. 2 - Clamped Inductive Waveforms

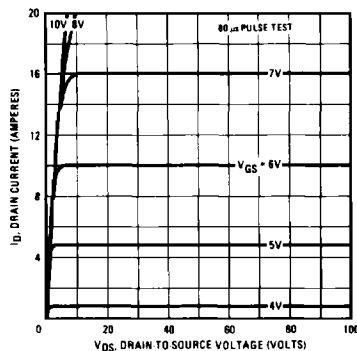


Fig. 3 - Typical Output Characteristics

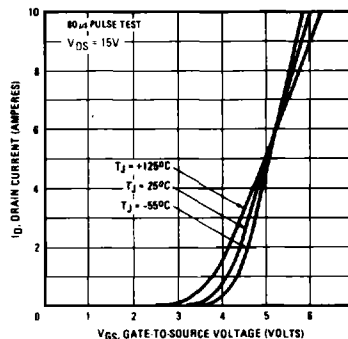


Fig. 4 - Typical Transfer Characteristics

2N6757, 2N6758

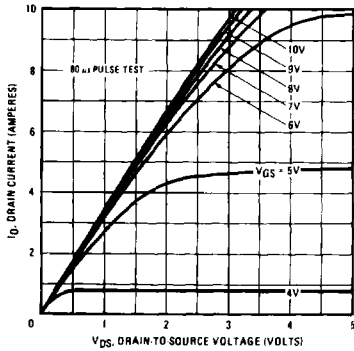


Fig. 5 - Typical Saturation Characteristics (2N6757)

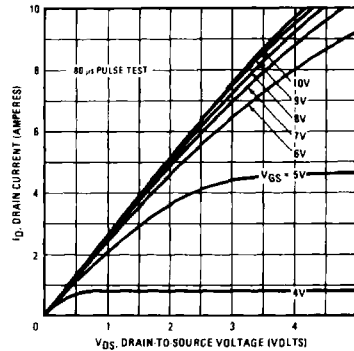


Fig. 6 - Typical Saturation Characteristics (2N6758)

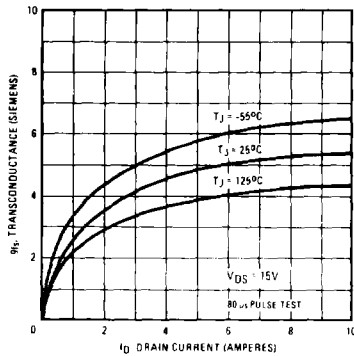


Fig. 7 - Typical Transconductance Vs. Drain Current

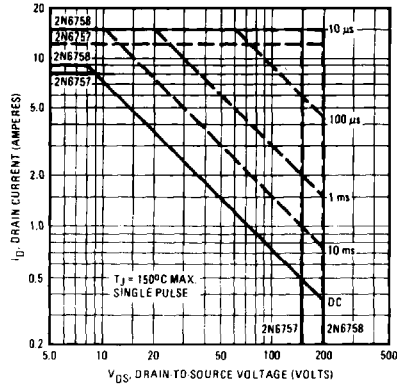


Fig. 8 - Maximum Safe Operating Area

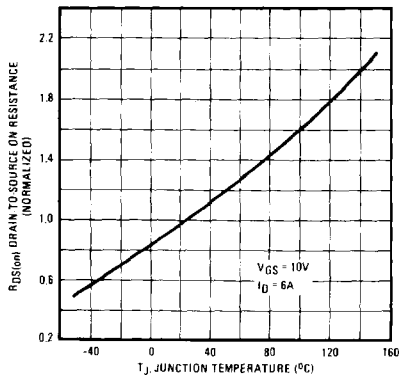


Fig. 9 - Normalized Typical On-Resistance Vs. Temperature

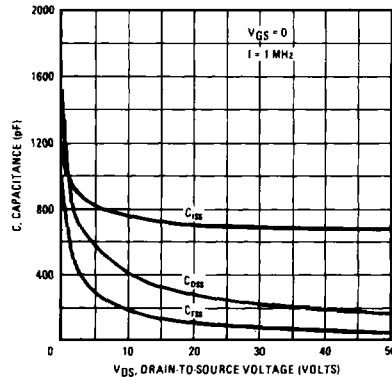


Fig. 10 - Typical Capacitance Vs. Drain-to-Source Voltage

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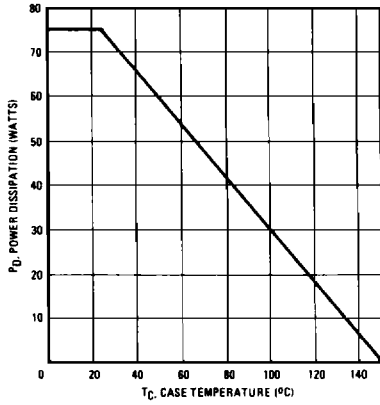


Fig. 11 -- Power Vs. Temperature Derating Curve

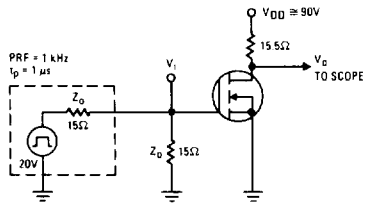


Fig. 13 -- Switching Time Test Circuit

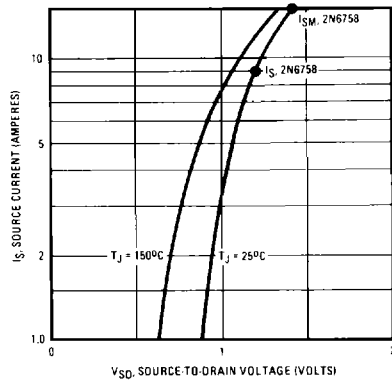


Fig. 12 -- Typical Body-Drain Diode Forward Voltage

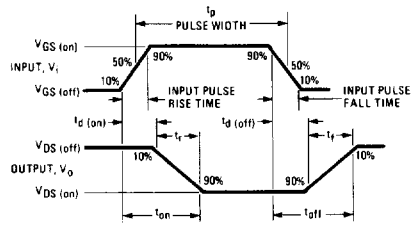


Fig. 14 -- Switching Time Waveforms