



4-Mb (512K x 8) MoBL[®] Static RAM

Features

- **Very high speed: 55 ns**
 - Wide voltage range: 2.20V – 3.60V
- **Pin-compatible with CY62148CV25, CY62148CV30 and CY62148CV33**
- **Ultra low active power**
 - Typical active current: 1.5 mA @ f = 1 MHz
 - Typical active current: 8 mA @ f = f_{max}(55-ns speed)
- **Ultra low standby power**
- **Easy memory expansion with \overline{CE} , and \overline{OE} features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Packages offered: 36-ball BGA, 32-pin TSOPII and 32-pin SOIC**

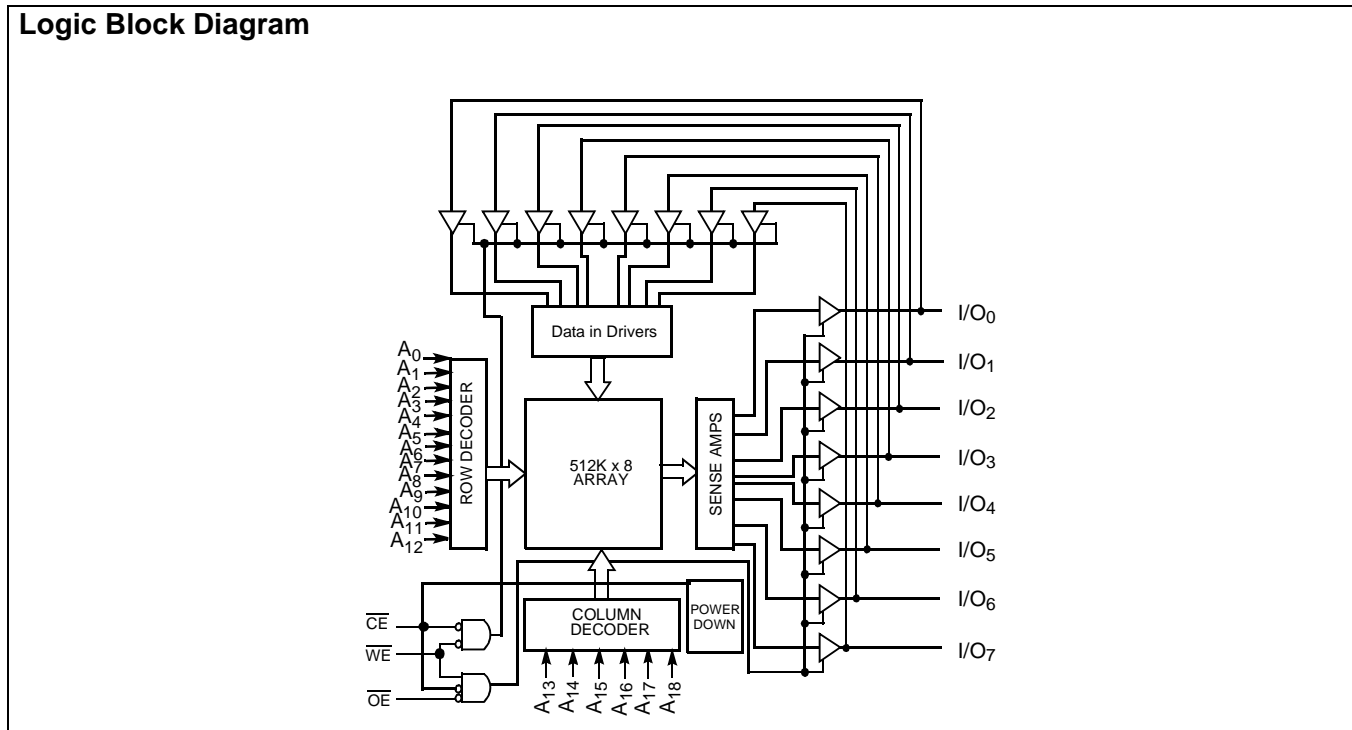
Functional Description^[1]

The CY62148DV30 is a high-performance CMOS static RAMs organized as 512K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL[®]) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption. The device can be put into standby mode reducing power consumption when deselected (\overline{CE} HIGH).

Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₈).

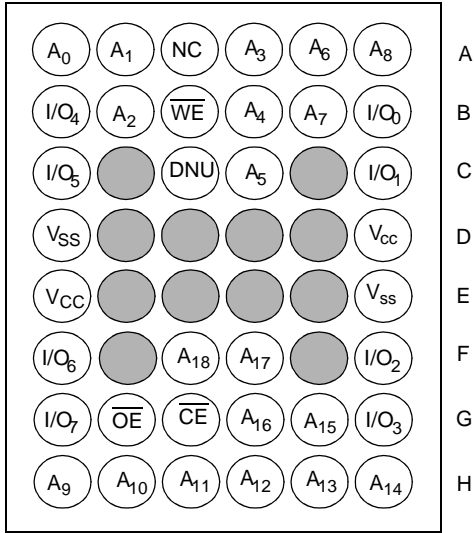
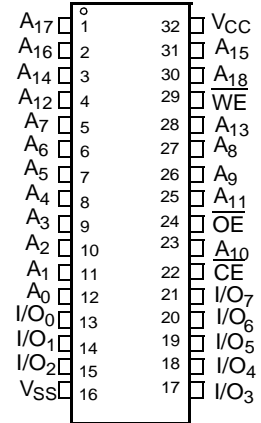
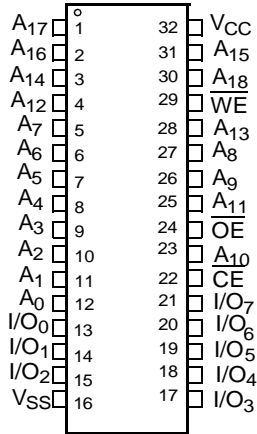
Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or during a write operation (\overline{CE} LOW and \overline{WE} LOW).



Note:

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

Pin Configuration^[2,3]
**FBGA
Top View**

**32 TSOPII
Top View**

**32 SOIC
Top View**

Notes:

- NC pins are not connected on the die.
- DNU pins have to be left floating or tied to V_{SS} to ensure proper application.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature -65°C to +150°C

Ambient Temperature with Power Applied..... 55°C to +125°C

Supply Voltage to Ground Potential -0.3V to $V_{CC(MAX)}$ + 0.3V

DC Voltage Applied to Outputs in High-Z State^[4,5] -0.3V to $V_{CC(MAX)}$ + 0.3V

DC Input Voltage^[4,5] -0.3V to $V_{CC(MAX)}$ + 0.3V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Product	Range	Ambient Temperature	V_{CC} ^[6]
CY62148DV30L	Industrial	-40°C to +85°C	2.2V to 3.6V
CY62148DV30LL			

Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (uA)	
					f = 1 MHz		f = f_{max}			
					Min.	Typ. ^[7]	Max.	Typ. ^[7]	Max.	Typ. ^[7]
CY62148DV30L	2.2	3.0	3.6	55	1.5	3	8	15	2	12
CY62148DV30LL	2.2	3.0	3.6	55		3		10		8
CY62148DV30L	2.2	3.0	3.6	70	1.5	3	8	15	2	12
CY62148DV30LL	2.2	3.0	3.6	70		3		10		8

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		CY62148DV30-55			CY62148DV30-70			Unit	
				Min.	Typ. ^[7]	Max.	Min.	Typ. ^[7]	Max.		
V_{OH}	Output HIGH Voltage	$I_{OH} = -0.1$ mA	$V_{CC} = 2.20$ V	2.0			2.0			V	
		$I_{OH} = -1.0$ mA	$V_{CC} = 2.70$ V	2.4			2.4			V	
V_{OL}	Output LOW Voltage	$I_{OL} = 0.1$ mA	$V_{CC} = 2.20$ V			0.4			0.4	V	
		$I_{OL} = 2.1$ mA	$V_{CC} = 2.70$ V			0.4			0.4	V	
V_{IH}	Input HIGH Voltage	$V_{CC} = 2.2$ V to 2.7 V		1.8		$V_{CC} + 0.3$ V	1.8		$V_{CC} + 0.3$ V	V	
		$V_{CC} = 2.7$ V to 3.6 V		2.2		$V_{CC} + 0.3$ V	2.2		$V_{CC} + 0.3$ V	V	
V_{IL}	Input LOW Voltage	$V_{CC} = 2.2$ V to 2.7 V		-0.3		0.6	-0.3		0.6	V	
		$V_{CC} = 2.7$ V to 3.6 V		-0.3		0.8	-0.3		0.8	V	
I_{IX}	Input Leakage Current	$GND \leq V_I \leq V_{CC}$		-1		+1	-1		+1	μA	
I_{OZ}	Output Leakage Current	$GND \leq V_O \leq V_{CC}$, Output Disabled		-1		+1	-1		+1	μA	
I_{CC}	V_{CC} Operating Supply Current	f = $f_{MAX} = 1/t_{RC}$	$V_{CC} = V_{CCmax}$ $I_{OUT} = 0$ mA CMOS levels	L		8	15		8	15	mA
				LL			10			10	mA
		f = 1 MHz	L		1.5	3		1.5	3	mA	
			LL							mA	
I_{SB1}	Automatic CE Power-down Current — CMOS Inputs	$CE \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V, $V_{IN} \leq 0.2$ V) f = f_{MAX} (Address and Data Only), f = 0 (OE, and WE), $V_{CC} = 3.60$ V		L		2	12		2	12	μA
				LL			8			8	μA
I_{SB2}	Automatic CE Power-down Current — CMOS Inputs	$CE \geq V_{CC} - 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V, f = 0, $V_{CC} = 3.60$ V		L		2	12		2	12	μA
				LL			8			8	μA

Notes:

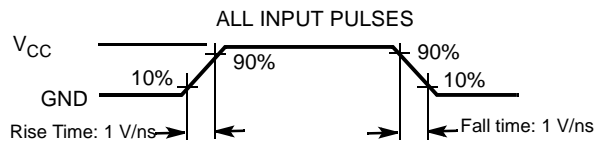
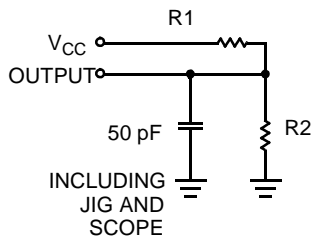
- $V_{IL(min)}$ = -2.0V for pulse durations less than 20 ns.
- $V_{IH(max)}$ = $V_{CC} + 0.75$ V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to $V_{CC(min)}$ and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25^\circ\text{C}$.

Capacitance for all packages^[8]

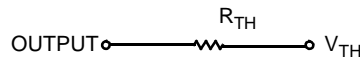
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC}(\text{typ.})$	10	pF
C_{OUT}	Output Capacitance		10	pF

Thermal Resistance

Parameter	Description	Test Conditions	BGA	TSOP II	SOIC	STSOP	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, four-layer printed circuit board	72	75.13	55	105	$^\circ\text{C/W}$
Θ_{JC}	Thermal Resistance (Junction to Case)		8.86	8.95	22	13	$^\circ\text{C/W}$

AC Test Loads and Waveforms


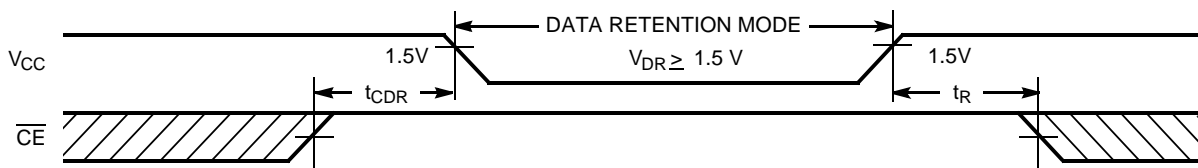
Equivalent to: THÉVENIN EQUIVALENT



Parameters	2.50V	3.0V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics (Over the Operating Range)

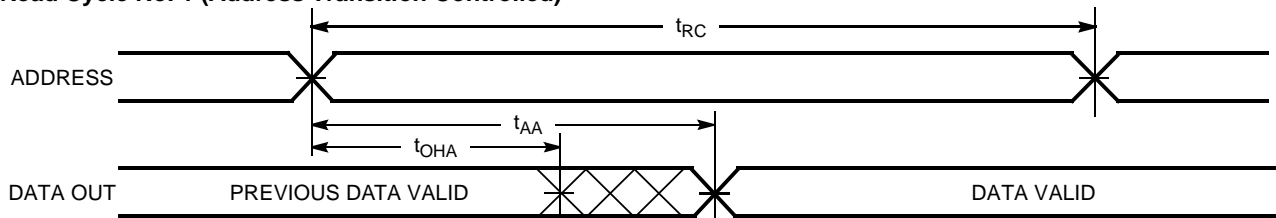
Parameter	Description	Conditions	Min.	Typ. ^[7]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR}	Data Retention Current	$V_{CC} = 1.5\text{V}$, $\overline{CE} \geq V_{CC} - 0.2\text{V}$, $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	L		9	μA
			LL		6	μA
$t_{CDR}^{[8]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[9]}$	Operation Recovery Time		t_{RC}			ns

Data Retention Waveform

Notes:

8. Tested initially and after any design or process changes that may affect these parameters.
9. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC}(\text{min.}) \geq 100\ \mu\text{s}$ or stable at $V_{CC}(\text{min.}) \geq 100\ \mu\text{s}$.

Switching Characteristics (Over the Operating Range)^[10]

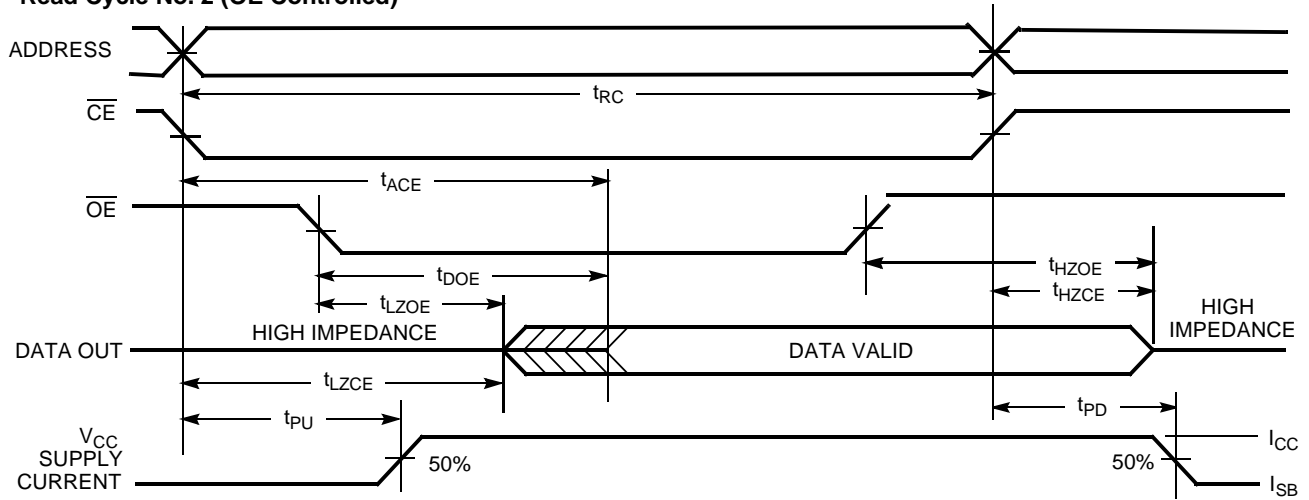
Parameter	Description	55 ns		70 ns		Unit
		Min.	Max.	Min.	Max.	
Read Cycle						
t_{RC}	Read Cycle Time	55		70		ns
t_{AA}	Address to Data Valid		55		70	ns
t_{OHA}	Data Hold from Address Change	10		10		ns
t_{ACE}	CE LOW to Data Valid		55		70	ns
t_{DOE}	OE LOW to Data Valid		25		35	ns
t_{LZOE}	OE LOW to Low Z ^[11]	5		5		ns
t_{HZOE}	OE HIGH to High Z ^[11,12]		20		25	ns
t_{LZCE}	CE LOW to Low Z ^[11]	10		10		ns
t_{HZCE}	CE HIGH to High Z ^[11, 12]		20		25	ns
t_{PU}	CE LOW to Power-up	0		0		ns
t_{PD}	CE HIGH to Power-up		55		70	ns
Write Cycle^[13]						
t_{WC}	Write Cycle Time	55		70		ns
t_{SCE}	CE LOW to Write End	40		45		ns
t_{AW}	Address Set-up to Write End	40		45		ns
t_{HA}	Address Hold from Write End	0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		ns
t_{PWE}	WE Pulse Width	40		45		ns
t_{SD}	Data Set-up to Write End	25		30		ns
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	WE LOW to High Z ^[11, 12]		20		25	ns
t_{LZWE}	WE HIGH to Low Z ^[11]	10		10		ns

Switching Waveforms
Read Cycle No. 1 (Address Transition Controlled)^[14, 15]

Notes:

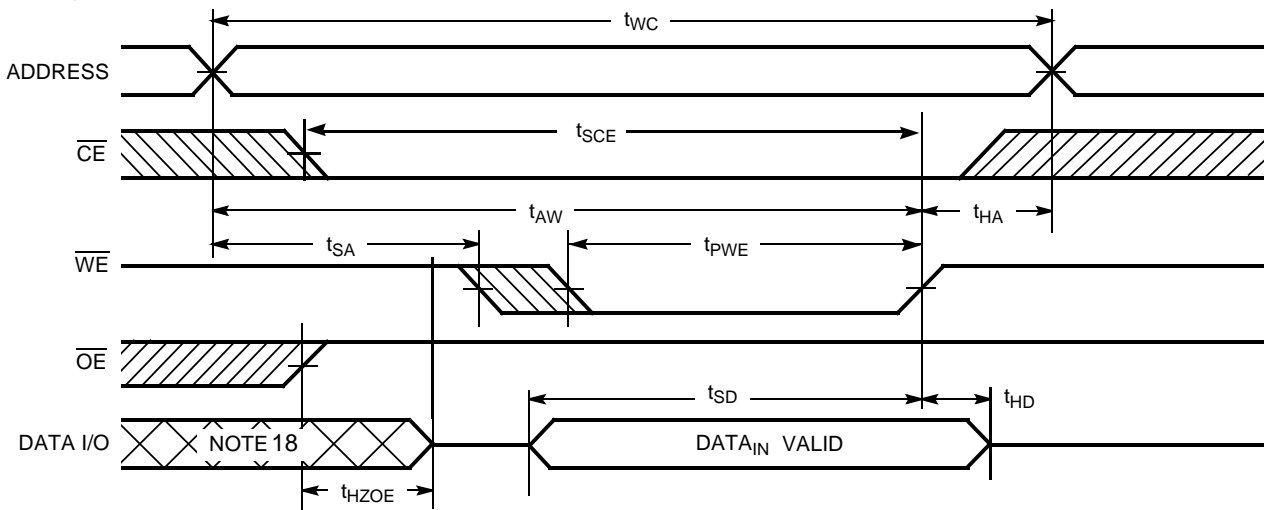
10. Test Conditions for all parameters other than three-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the "AC Test Loads and Waveforms" section.
11. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
12. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the output enters a high impedance state.
13. The internal write time of the memory is defined by the overlap of WE, CE = V_{IL} . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.
14. Device is continuously selected. OE, CE = V_{IL} .
15. WE is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 (\overline{OE} Controlled) [15, 16]

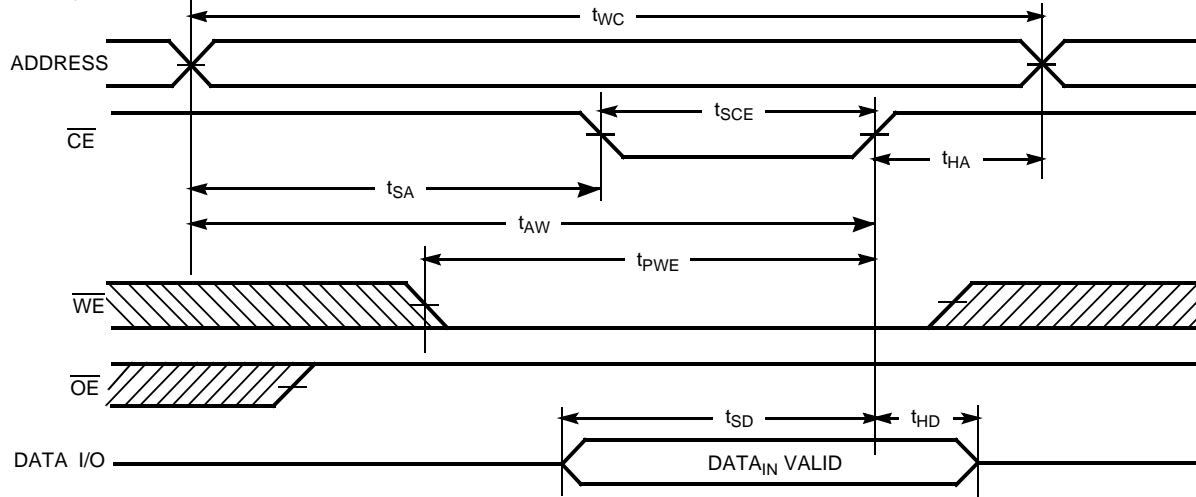
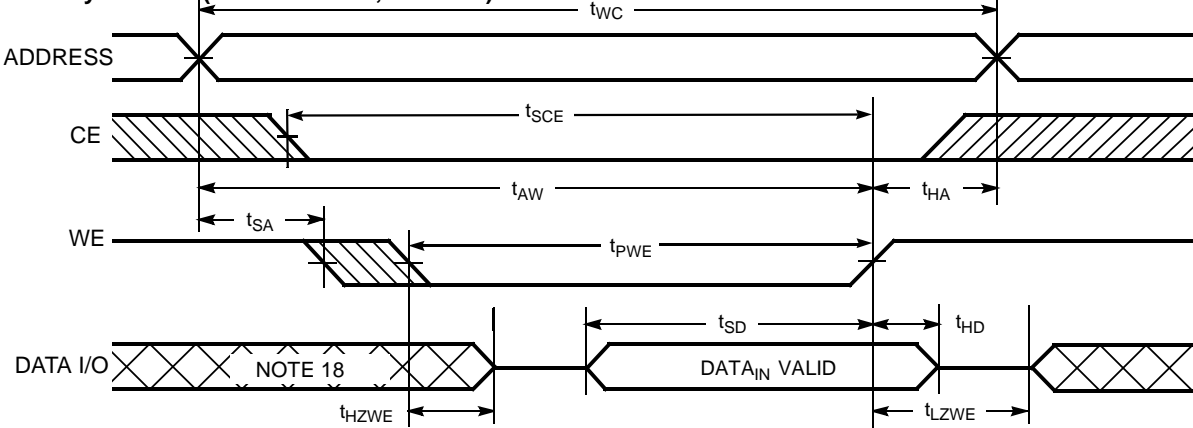


Write Cycle No. 1 (\overline{WE} Controlled) [17, 19]



Notes:

- 16. Address valid prior to or coincident with \overline{CE} transition LOW.
- 17. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 18. During this period, the I/Os are in output state and input signals should not be applied.
- 19. If CE goes HIGH simultaneously with WE HIGH, the output remains in high-impedance state.

Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CE} Controlled)^[17, 19]

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[19]

Truth Table

\overline{CE}	\overline{WE}	\overline{OE}	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	Data Out (I/O ₀ -I/O ₇)	Read	Active (I_{CC})
L	H	H	High Z	Output Disabled	Active (I_{CC})
L	L	X	Data in (I/O ₀ -I/O ₇)	Write	Active (I_{CC})

Ordering Information

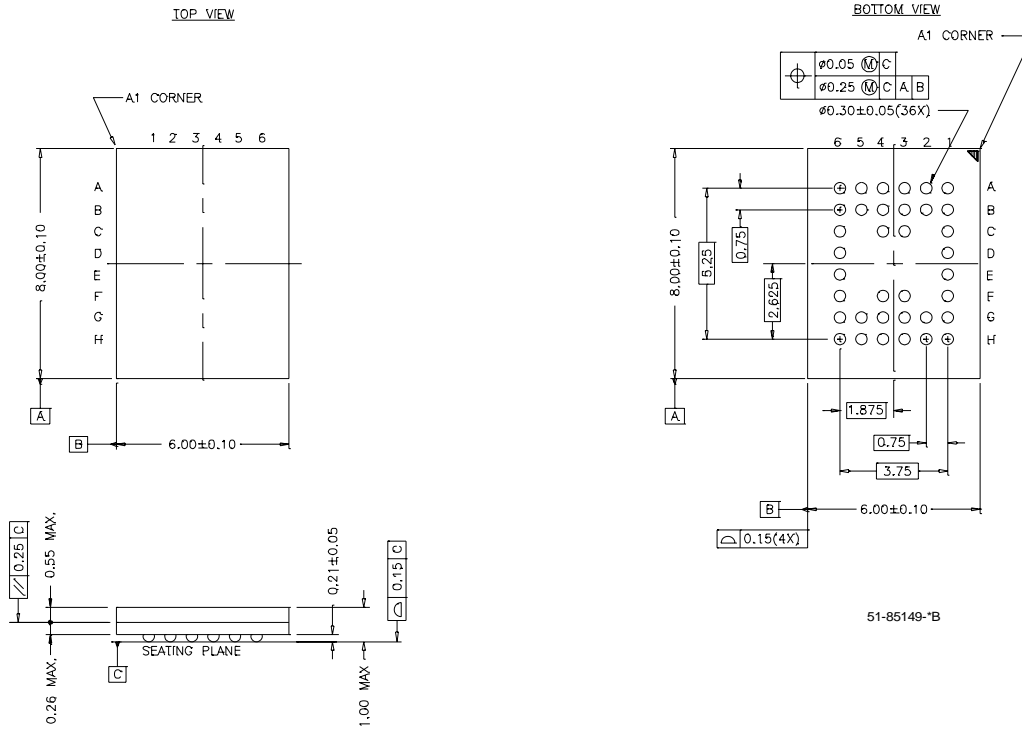
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
55	CY62148DV30L-55BVI	BV36A	36-ball Very Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62148DV30LL-55BVI			
55	CY62148DV30L-55BVXI	BV36A	36-ball Very Fine Pitch BGA (6 mm x 8 mm x 1 mm) Pb-free	Industrial
	CY62148DV30LL-55BVXI			
55	CY62148DV30L-55ZSXI	ZS-32	32-pin TSOP II Pb-free	Industrial
	CY62148DV30LL-55ZSXI			
55	CY62148DV30L-55SXI	S-32	32-pin SOIC Pb-free	Industrial
	CY62148DV30LL-55SXI			

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY62148DV30L-70BVI	BV36A	36-ball Very Fine Pitch BGA (6 mm x 8 mm x 1 mm)	Industrial
	CY62148DV30LL-70BVI			
70	CY62148DV30L-70BVXI	BV36A	36-ball Very Fine Pitch BGA (6 mm x 8 mm x 1 mm) Pb-free	Industrial
	CY62148DV30LL-70BVXI			
70	CY62148DV30L-70ZSXI	ZS-32	32-pin TSOP II Pb-free	Industrial
	CY62148DV30LL-70ZSXI			
70	CY62148DV30L-70SXI	S-32	32-pin SOIC Pb-free	Industrial
	CY62148DV30LL-70SXI			

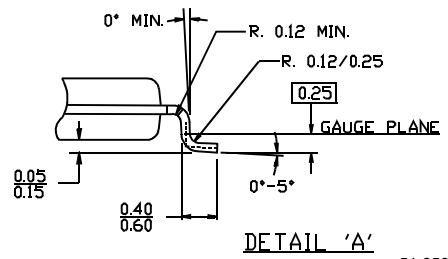
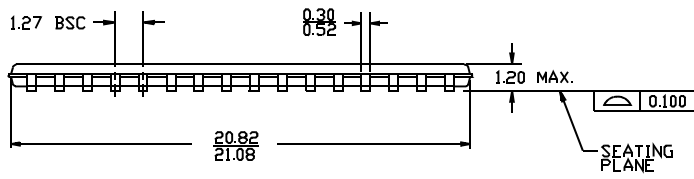
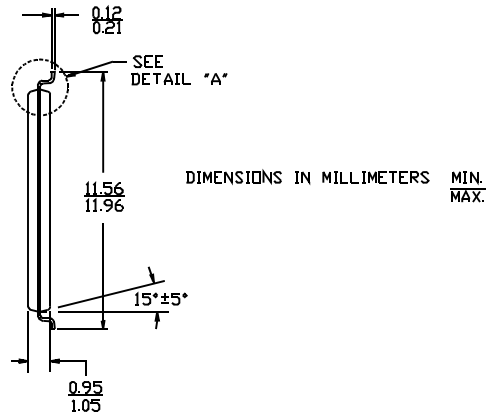
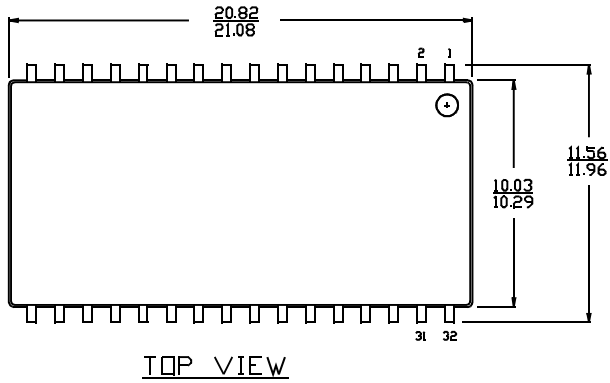
Package Diagrams

36-Lead FBGA (6 x 8 x 1 mm) BV36A

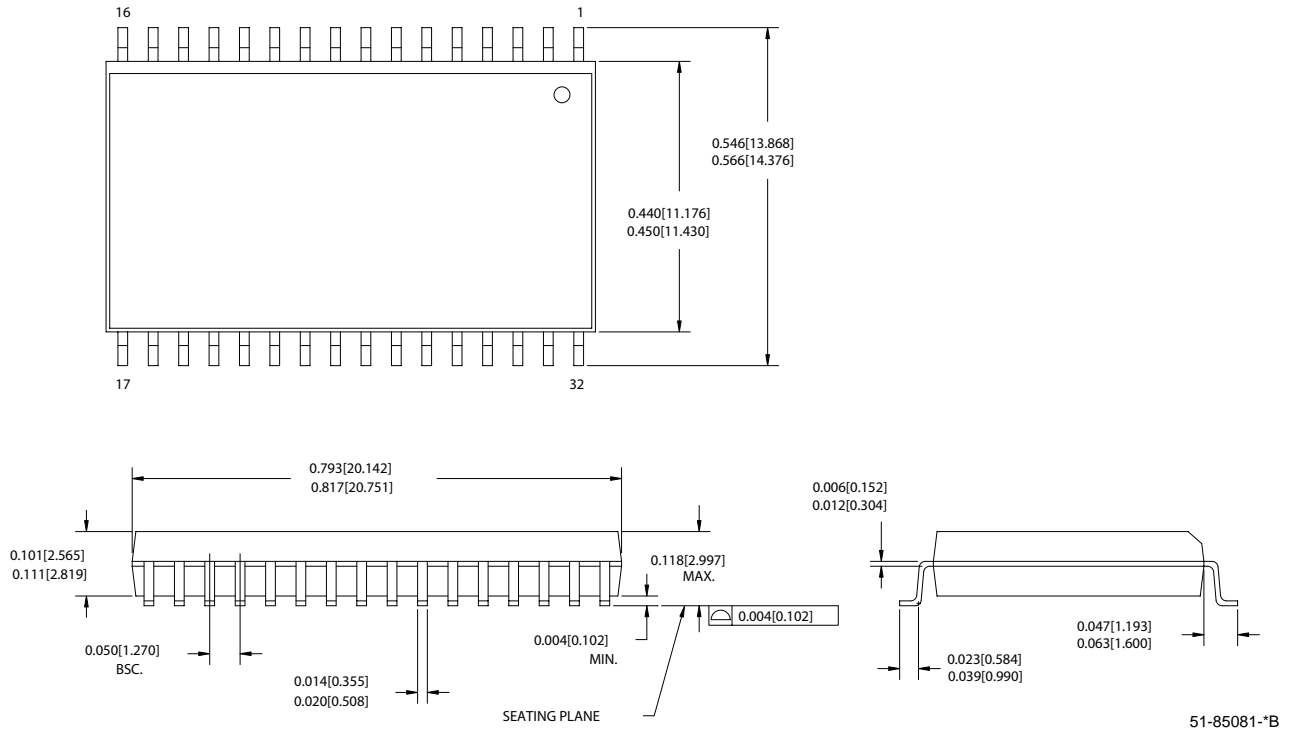


Package Diagrams (continued)

32-Lead TSOP II ZS32



51-85095-**

Package Diagrams (continued)
32-Lead (450 MIL) Molded SOIC S34


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Document History Page

Document Title: CY62148DV30 4-Mb (512K x 8) MoBL [®] Static RAM				
Document Number: 38-05341				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	127480	06/17/03	HRT	Created new data sheet
*A	131041	01/23/04	CBD	Change from Advance to Preliminary
*B	222180	See ECN	AJU	Change from Preliminary to Final Added 70 ns speed bin Modified footnote #6 and #12 Removed MAX value for V _{DR} on "Data Retention Characteristics" table Modified input and output capacitance values Added Pb-free ordering information Removed 32-pin STSOP package