

# High-Speed CMOS 16-Bit Bus Register Transceiver (3-State)

QS74FCT16952T  
 QS74FCT162952T

## FEATURES/BENEFITS

- Pin and function compatible with T.I. Widebus™ and IDT Double-Density™ families
- CMOS power levels: <math><1\mu\text{W}</math> typical standby
- SSOP (PV) and TSSOP (PA) packages
- Low output skew: 0.5ns  $t_{SK(O)}$
- Flow-through pinout for easy layout
- Power off disable allows hot plugging
- Industrial temperature:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise

### FCT16952T

- High drive standard FCT-T outputs:  
 $I_{OL} = +64\text{mA}$ ,  $I_{OH} = -32\text{mA}$
- Incident switching for driving buses and large loads

### FCT162952T

- Balanced output drivers:  $\pm 24\text{mA}$
- Reduced switching noise for point to point signals

## DESCRIPTION

The FCT16952 family of products are 16-bit bus register transceivers with three-state outputs that are ideal for driving address and data buses. Two independent 8-bit registered transceivers are used to permit independent control of data flow in either direction. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. All outputs have ground bounce suppression circuitry (see QSI Application Note AN-01) and many power and ground pins provide low ground bounce. To accommodate hot-plug or live insertion applications, both versions of this product were designed not to load an active bus when  $V_{CC}$  is removed. In applications where bus signals are point-to-point or driving light capacitance loads, the balanced drive FCT162952 is recommended.

Figure 1. Functional Block Diagram

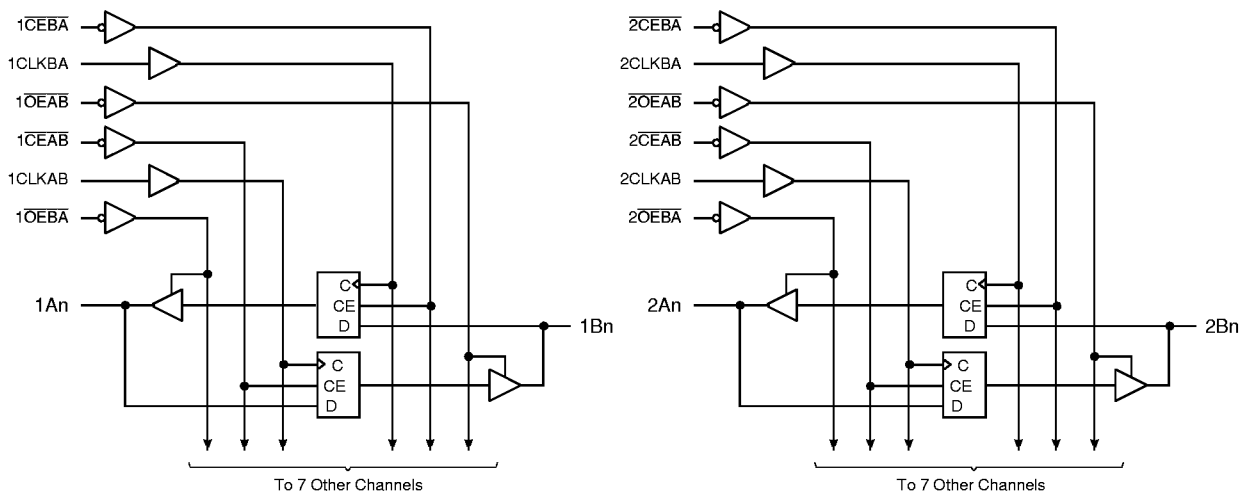


Figure 2. Pin Configuration (All Pins Top View)

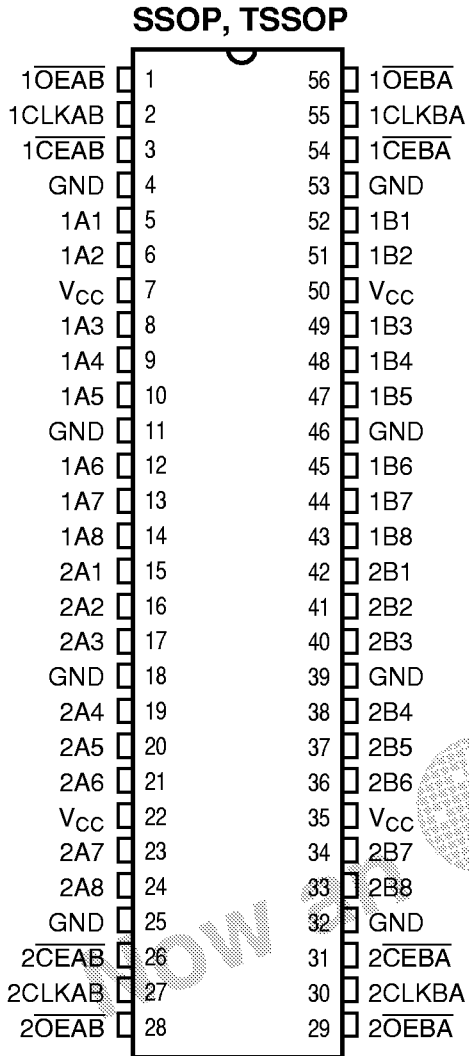


Table 1. Pin Description

Name	Description
$\overline{xOEAB}$	A to B Output Enable Inputs (Active LOW)
$\overline{xOEBA}$	B to A Output Enable Inputs (Active LOW)
$\overline{xCEAB}$	A to B Enable Inputs (Active LOW)
$\overline{xCEBA}$	B to A Enable Inputs (Active LOW)
$xCLKAB$	A to B Clock Inputs
$xCLKBA$	B to A Clock Inputs
$xAx$	A to B Data Inputs or B to A 3 State Outputs
$xBx$	B to A Data Inputs or A to B 3 State Outputs

Table 2. Function Table<sup>(1,2)</sup>

Inputs			Outputs	
$\overline{xCEAB}$	$xCLKAB$	$\overline{xOEAB}$	$xAx$	$xBx$
H	X	L	X	B <sup>(3)</sup>
X	L	L	X	B <sup>(3)</sup>
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

**Notes:**

- ↑ = LOW-to-HIGH Transition  
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care
- A-to-B data flow shown: B-to-A flow control is the same, except using  $\overline{xCEBA}$ ,  $xCLKBA$ , and  $\overline{xOEBA}$ .
- Level of B before the indicated steady-state input conditions were established.

**Table 3. Absolute Maximum Ratings**

Supply Voltage to Ground .....	-0.5V to +7.0V
DC Output Voltage $V_{OUT}$ .....	-0.5V to +7.0V
DC Input Voltage $V_{IN}$ .....	-0.5V to +7.0V
AC Input Voltage (for a pulse width $\leq 20$ ns) .....	-3.0V
DC Input Diode Current with $V_{IN} < 0$ .....	-20mA
DC Output Diode Current with $V_{OUT} < 0$ .....	-50mA
DC Output Current Max. Sink Current/Pin .....	120mA
Maximum Power Dissipation .....	1.0 watts
$T_{STG}$ Storage Temperature .....	-65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

**Table 4. Recommended Operating Conditions**

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Supply Voltage	4.5	5.5	V
$V_{IN}$	Input Voltage	-0.5	5.5	V
$V_{OUT}$	Voltage Applied to Output or I/O	0	$V_{CC}$	V
$\Delta t/\Delta v$	Input Transition Slew Rate	—	10	ns/V
$T_A$	Operating Free Air Temperature	-40	+85	°C

**Table 5. DC Electrical Characteristics Over Operating Range**

Recommended Operating Conditions apply unless otherwise noted.

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Unit
$V_{IH}$	Input HIGH Voltage	Logic HIGH for All Inputs	2.0	—	—	V
$V_{IL}$	Input LOW Voltage	Logic LOW for All Inputs	—	—	0.8	V
$\Delta V_T$	Input Hysteresis	$V_{TLH} - V_{THL}$ for All Inputs <sup>(4)</sup>	—	100	—	mV
$ I_{IH} $ $ I_{IL} $	Input Current Input HIGH or LOW	$V_{CC} = \text{Max.}, 0 \leq V_{IN} < V_{CC}$	—	—	1	$\mu\text{A}$
$ I_{OZ} $	Off-State Output Current (Hi-Z)	$V_{CC} = \text{Max.}, 0 \leq V_{OUT} \leq V_{CC}$	—	—	1	$\mu\text{A}$
$ I_{OFF} $	Power off leakage	$V_{CC} = 0\text{V}, V_{IN}/V_{OUT} \leq 4.5\text{V}^{(5)}$	—	—	1	$\mu\text{A}$
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_{OUT} = \text{GND}^{(3,4)}$	-80	-140	-225	mA
$V_{IK}$	Input Clamp Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$	-	-0.7	-1.2	V

**Notes:**

1. For conditions shown as Min. or Max. use appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values indicate  $V_{CC} = 5.0\text{V}$  and  $T_A = 25^\circ\text{C}$ .
3. Not more than one output should be tested at one time. Duration of test should not exceed one second.
4. These parameters are guaranteed by design but not tested.
5. The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$

**Table 6. Capacitance**

$T_A = 25^\circ\text{C}, f = 1\text{MHz}, V_{IN} = 0\text{V}, V_{OUT} = 0\text{V}$

Pins	Typ	Max	Unit
All	6.0	9.0	pF

Table 7. Output Drive Characteristics for FCT16952T

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min.	I <sub>OH</sub> = -3mA	2.5	3.4	—	V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -15mA	2.4	3.2	—	V
			I <sub>OH</sub> = -32mA <sup>(4)</sup>	2.0	3.0	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 64mA	—	0.3	0.55	V

Table 8. Output Drive Characteristics for FCT162952T

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min	Typ <sup>(2)</sup>	Max	Unit	
I <sub>ODL</sub>	Output LOW Current	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 1.5V <sup>(3)</sup>	60	115	200	mA	
I <sub>ODH</sub>	Output HIGH Current	V <sub>CC</sub> = 5V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> V <sub>OUT</sub> = 1.5V <sup>(3)</sup>	-60	-115	-200	mA	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -24mA	2.4	3.1	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min. V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 24mA	—	0.3	0.55	V

**Notes:**

1. For conditions shown as Min. or Max. use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values indicate V<sub>CC</sub> = 5.0V and T<sub>A</sub> = 25°C.
3. Not more than one output should be shorted and the duration is ≤1 second.
4. Duration of the condition should not exceed one second.

**Table 9. Power Supply Characteristics**

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Typ <sup>(2)</sup>	Max	Unit	
$I_{CCL}$ $I_{CCH}$ $I_{CCZ}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$	5	500	$\mu\text{A}$	
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = \text{Max.}, V_{IN} = 3.4\text{V}^{(3)}$	0.5	1.5	mA	
$Q_{CCD}$	Supply Current per Input per MHz <sup>(4)</sup>	$V_{CC} = \text{Max.}, \text{Outputs Open One Bit Toggling @ 50\% Duty Cycle}$ $\overline{xOEAB} = \overline{xCEAB} = \text{GND}$	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	75 120	$\mu\text{A}/\text{MHz}$	
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}, \text{Outputs Open One Bit Toggling @ 50\% Duty Cycle}$ $f_I = 5\text{MHz},$ $f_{CP} = 10\text{MHz (xCLKAB)}$ $\overline{xOEAB} = \overline{xCEAB} = \text{GND}$ $\overline{xOEBA} = V_{CC}$	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	0.8	1.7 <sup>(5)</sup>	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	1.3	3.2 <sup>(5)</sup>	mA
		$V_{CC} = \text{Max.}, \text{Outputs Open Sixteen Bits Toggling @ 50\% Duty Cycle}$ $f_I = 2.5\text{MHz},$ $f_{CP} = 10\text{MHz (xCLKAB)}$ $\overline{xOEAB} = \overline{xCEAB} = \text{GND}$ $\overline{xOEBA} = V_{CC}$	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	3.8	6.5 <sup>(5)</sup>	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	8.3	20 <sup>(5)</sup>	mA

**Notes:**

- For conditions shown as Min. or Max., use the appropriate values specified under Recommended Operating Conditions for applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}, +25^\circ\text{C}$  ambient.
- Per TTL driven input ( $V_{IN} = 3.4\text{V}$ ). All Other Inputs at  $V_{CC}$  or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the  $I_{CC}$  formula. These limits are guaranteed by design but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} = I_{\text{DYNAMIC}}$   
 $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_I N_I)$   
 $I_{CCQ} = \text{Quiescent Current (} I_{CCL}, I_{CCH}, \text{ and } I_{CCZ}\text{)}$   
 $\Delta I_{CC} = \text{Power Supply Current for a TTL-High Input (} V_{IN} = 3.4\text{V)}$   
 $D_H = \text{Duty Cycle for TTL High Inputs.}$   
 $N_T = \text{Number of TTL High Inputs.}$   
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$   
 $f_{CP} = \text{Clock Frequency for Register devices (Zero for Non-Register Devices)}$   
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$   
 $f_I = \text{Input Frequency.}$   
 $N_I = \text{Number of Inputs at } f_I$

**Table 10. Switching Characteristics Over Operating Range**

Recommended Operating Ranges apply unless otherwise specified.

$C_{LOAD} = 50\text{pF}$ ,  $R_{LOAD} = 500\Omega$  unless otherwise noted.

Symbol	Description <sup>(1)</sup>	FCT16952AT		FCT16952BT		FCT16952CT		Unit
		FCT162952AT		FCT162952BT		FCT162952CT		
		Min	Max	Min	Max	Min	Max	
$t_{PHL}$ $t_{PLH}$	Propagation Delay xCLKAB, xCLKBA to xAx, xBx	2.0	10.0	2.0	7.5	2.0	6.3	ns
$t_{PZH}$ $t_{PZL}$	Output Enable Time xOEBA, xOEAB to xAx, xBx	1.5	10.5	1.5	8.0	1.5	7.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable Time <sup>(2)</sup> xOEBA, xOEAB to xAx, xBx	1.5	10.0	1.5	7.5	1.5	6.5	ns
$t_{SU}$	Setup Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA	2.5	—	2.5	—	2.5	—	ns
$t_H$	Hold Time HIGH or LOW xAx, xBx to xCLKAB, xCLKBA	2.0	—	1.5	—	1.5	—	ns
$t_{SU}$	Setup Time HIGH or LOW xCEBA, xCEAB to xCLKAB, xCLKBA	3.0	—	3.0	—	3.0	—	ns
$t_H$	Hold Time HIGH or LOW xCEBA, xCEAB to xCLKAB, xCLKBA	2.0	—	2.0	—	2.0	—	ns
$t_W$	Pulse Width LOW xCLKAB or xCLKBA <sup>(2)</sup>	3.0	—	3.0	—	3.0	—	ns
$t_{SK(O)}$	Output Skew <sup>(3)</sup>	—	0.5	—	0.5	—	0.5	ns

**Notes:**

1. Minimums guaranteed but not tested. See Test Circuit and Waveforms.
2. This parameter is guaranteed but not production tested.
3. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design but not tested.