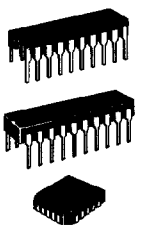
Quad Bus Driver/Receiver with Transmit and Receiver Latches

MC10H334

The MC10H334 is a Quad Bus Driver/Receiver with transmit and receiver latches. When disabled, ($\overline{OE}$ = high) the bus outputs will fall to –2.0 V. Data to be transmitted or received is passed through its respective latch when the respective latch enable ($\overline{DLE}$ and $\overline{RLE}$) is at a low level. Information is latched on the positive transition of $\overline{DLE}$ and $\overline{RLE}$. The parameters specified are with 25 Ω loading on the bus drivers and 50 Ω loads on the receivers.

- Propagation Delay, 1.6 ns Typical Data–to–Output
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 732–03

P SUFFIX
PLASTIC PACKAGE
CASE 738–03

FN SUFFIX
PLCC
CASE 775–02

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MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	–8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	–55 to +150 –55 to +165	°C °C

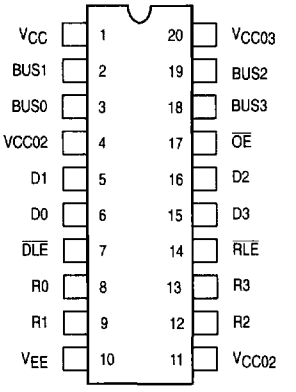
ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	Symbol	Min	Max	Min	Max	Min	Max	Unit
Power Supply Current	I_E	—	161	—	161	—	161	mA
Input Current High Pins 5,6,15,16 Pins 7,14 Pin 17	I_{inH}	 — — —	 397 460 520	 — — —	 273 297 357	 — — —	 273 297 357	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
Low Output Voltage	V_{OL}	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
High Input Voltage	V_{IH}	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
Low Input Voltage	V_{IL}	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

Propagation Delay Data–to–Bus Output $\overline{DLE}$–to–Bus Output $\overline{OE}$–to–Bus Output Bus–to–R0 $\overline{RLE}$–to–R0 Data–to–Receiver R0	t_{pd}	 0.5 1.0 0.5 0.5 0.5 1.0	 2.5 2.7 2.5 1.9 2.1 3.8	 0.5 1.0 0.5 0.5 0.5 1.0	 2.5 2.7 2.5 1.9 2.1 3.8	 0.5 1.0 0.5 0.5 0.5 1.0	 2.5 2.7 2.5 1.9 2.1 3.8	ns
Rise Time	t_r	0.5	2.2	0.5	2.2	0.5	2.2	ns
Fall Time	t_f	0.5	2.2	0.5	2.2	0.5	2.2	ns

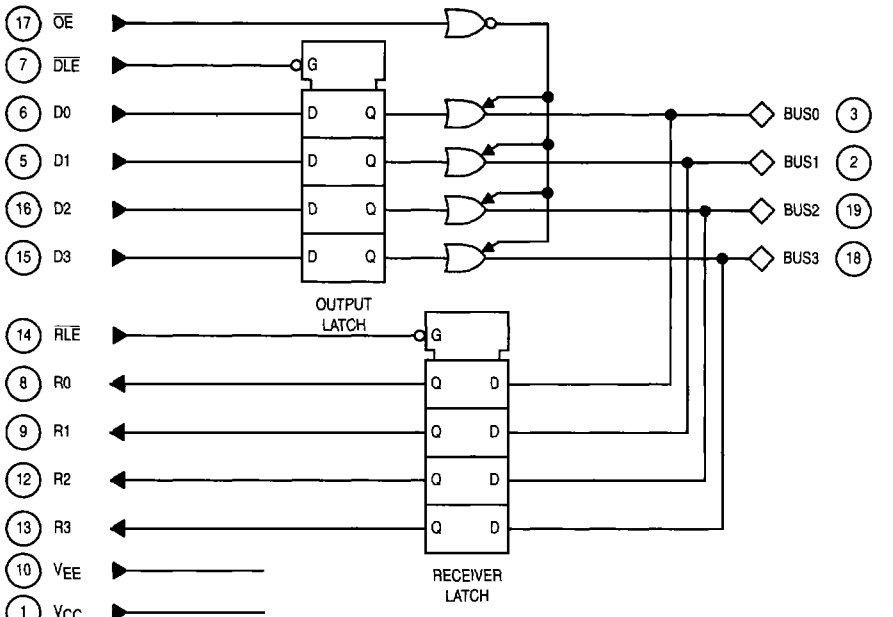
DIP & PLCC PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfpm is maintained. Receiver outputs are terminated through a 50–ohm resistor to –2.0 volts dc. Bus outputs are terminated through a 25–ohm resistor to –2.0 volts dc.

LOGIC DIAGRAM



DRIVER TRUTH TABLE

D	$\overline{DLE}$	$\overline{OE}$	Bus_{n+1}
X	X	H	–2.0 V
D	L	L	D
X	H	L	Bus_n

RECEIVER TRUTH TABLE

Bus	$\overline{RLE}$	R_{n+1}
Bus	L	Bus
X	H	R_n

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