

## DS36954 Quad Differential Bus Transceiver

 Check for Samples: [DS36954](#)

### FEATURES

- Pinout for SCSI Interface
- Compact 20-Pin PLCC or SOIC Package
- Meets EIA-485 Standard for Multipoint Bus Transmission
- Greater than 60 mA Source/Sink Currents
- Thermal Shutdown Protection
- Glitch-Free Driver Outputs on Power Up and Down

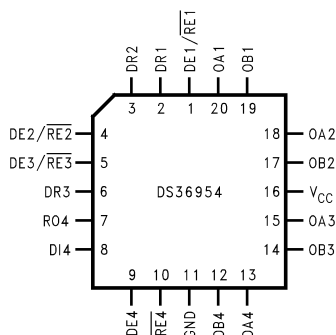
### DESCRIPTION

The DS36954 is a low power, quad EIA-485 differential bus transceiver especially suited for high speed, parallel, multipoint, I/O bus applications. A compact 20-pin surface mount PLCC or SOIC package provides high transceiver integration and a very small PC board footprint.

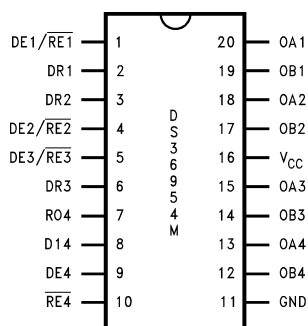
Propagation delay skew between devices is specified to aid in parallel interface designs—limits on maximum and minimum delay times are verified.

Five devices can implement a complete SCSI initiator or target interface. Three transceivers in a package are pinned out for data bus connections. The fourth transceiver, with the flexibility provided by its individual enables, can serve as a control bus transceiver.

### Connection Diagram

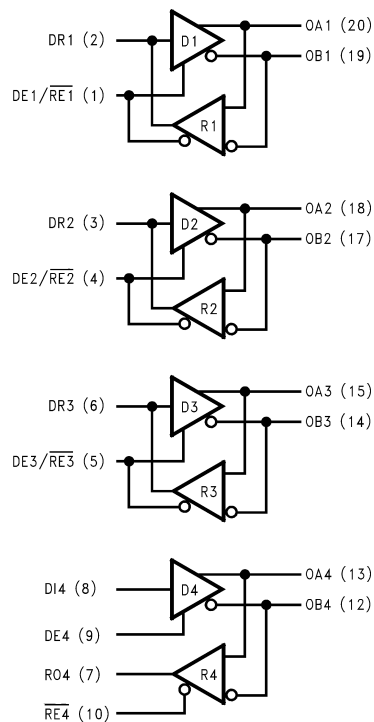


See Package Number FN (S-PQCC-J20)



See Package Number DW (R-PDSO-G20)

### Logic Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### Absolute Maximum Ratings <sup>(1)(2)</sup>

Supply Voltage	7V
Control Input Voltage	$V_{CC} + 0.5V$
Driver Input Voltage	$V_{CC} + 0.5V$
Driver Output Voltage/Receiver Input Voltage	-10V to +15V
Receiver Output Voltage	5.5V
Continuous Power Dissipation @ +25°C	
FN Package	1.73W
DW Package	1.73W
Derate FN Package	13.9 mW/°C above +25°C
Derate DW Package	13.7 mW/°C above +25°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 4 Sec.)	260°C

- (1) "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be verified. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instrument Sales Office/ Distributors for availability and specifications.

### Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, $V_{CC}$	4.75	5.25	V
Bus Voltage	-7	+12	V
Operating Free Air Temperature ( $T_A$ )	0	+70	°C

### Electrical Characteristics <sup>(1)(2)</sup>

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>DRIVER CHARACTERISTICS</b>						
$V_{ODL}$	Differential Driver Output Voltage (Full Load)	$I_L = 60 \text{ mA}$ $V_{CM} = 0V$	1.5	1.9		V
$V_{OD}$	Differential Driver Output Voltage (Termination Load)	$R_L = 100\Omega$ (EIA-422) $R_L = 54\Omega$ (EIA-485)	2.0 1.5	2.25 2.0		V
$\Delta IVODI$	Change in Magnitude of Driver Differential Output Voltage for Complementary Output States	$R_L = 54$ or $100\Omega$ <sup>(3)</sup> (Figure 1) (EIA-422/485)			0.2	V
$V_{OC}$	Driver Common Mode Output Voltage <sup>(4)</sup>	$R_L = 54\Omega$ (Figure 1) (EIA-485)			3.0	V
$\Delta IVOCI$	Change in Magnitude of Common Mode Output Voltage	<sup>(3)</sup> (Figure 1) (EIA-422/485)			0.2	V
$V_{OH}$	Output Voltage High	$I_{OH} = -55 \text{ mA}$	2.7	3.2		V
$V_{OL}$	Output Voltage Low	$I_{OL} = 55 \text{ mA}$		1.4	1.7	V
$V_{IH}$	Input Voltage High		2.0			V
$V_{IL}$	Input Voltage Low				0.8	V
$V_{CL}$	Input Clamp Voltage	$I_{CL} = -18 \text{ mA}$			-1.5	V

- (1) Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.
- (2) All typicals are given for  $V_{CC} = 5V$  and  $T_A = 25^\circ\text{C}$ .
- (3)  $\Delta IVODI$  and  $\Delta IVOCI$  are changes in magnitude of  $V_{OD}$  and  $V_{OC}$ , respectively, that occur when the input changes state.
- (4) In EIA Standards EIA-422 and EIA-485,  $V_{OC}$ , which is the average of the two output voltages with respect to ground, is called output offset voltage,  $V_{OS}$ .

**Electrical Characteristics <sup>(1)(2)</sup> (continued)**

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$I_{IH}$	Input High Current	$V_{IN} = 2.4V$ <sup>(5)</sup>			20	$\mu A$
$I_{IL}$	Input Low Current	$V_{IN} = 0.4V$ <sup>(5)</sup>			-20	$\mu A$
$I_{OSC}$	Driver Short-Circuit Output Current <sup>(6)</sup>	$V_O = -7V$ (EIA-485)		-130	-250	mA
		$V_O = 0V$ (EIA-422)		-90	-150	mA
		$V_O = +12V$ (EIA-485)		130	250	mA
<b>RECEIVER CHARACTERISTICS</b>						
$I_{OSR}$	Short Circuit Output Current	$V_O = 0V$ <sup>(6)</sup>	-15	-28	-75	mA
$I_{OZ}$	TRI-STATE Output Current	$V_O = 0.4V$ to $2.4V$			20	$\mu A$
$V_{OH}$	Output Voltage High	$V_{ID} = 0.2V$ , $I_{OH} = 0.4$ mA	2.4	3.0		V
$V_{OL}$	Output Voltage Low	$V_{ID} = -0.2V$ , $I_{OL} = 4$ mA		0.35	0.5	V
$V_{TH}$	Differential Input High Threshold Voltage	$V_O = V_{OH}$ , $I_O = -0.4$ mA (EIA-422/485)		0.03	0.2	V
$V_{TL}$	Differential Input Low Threshold Voltage <sup>(7)</sup>	$V_O = V_{OL}$ , $I_O = 4.0$ mA (EIA-422/485)	-0.2 0	-0.03		V
$V_{HST}$	Hysteresis <sup>(8)</sup>	$V_{CM} = 0V$	35	60		mV
<b>DRIVER AND RECEIVER CHARACTERISTICS</b>						
$V_{IH}$	Enable Input Voltage High		2.0			V
$V_{IL}$	Enable Input Voltage Low				0.8	V
$V_{CL}$	Enable Input Clamp Voltage	$I_{CL} = -18$ mA			-1.5	V
$I_{IN}$	Line Input Current <sup>(9)</sup>	Other Input = 0V DE/RE = 0.8V DE4 = 0.8V	$V_I = +12V$	0.5	1.0	mA
			$V_I = -7V$	-0.45	-0.8	mA
$I_{ING}$	Line Input Current <sup>(9)</sup>	Other Input = 0V DE/RE and DE4 = 2V $V_{CC} = 3.0V$ $T_A = +25^\circ C$	$V_I = +12V$		1.0	mA
			$V_I = -7V$		-0.8	mA
$I_{IH}$	Enable Input Current High	$V_{IN} = 2.4V$ DE/RE	$V_{CC} = 3.0V$	1	40	$\mu A$
			$V_{CC} = 4.75V$	1		$\mu A$
			$V_{CC} = 5.25V$	1	40	$\mu A$
		$V_{IN} = 2.4V$ DE4 or RE4	$V_{CC} = 3.0V$	1	20	$\mu A$
			$V_{CC} = 5.25V$	1	20	$\mu A$
$I_{IL}$	Enable Input Current Low	$V_{IN} = 0.8V$ DE/RE	$V_{CC} = 3.0V$	-6	-40	$\mu A$
			$V_{CC} = 4.75V$	-12		$\mu A$
			$V_{CC} = 5.25V$	-14	-40	$\mu A$
		$V_{IN} = 0.8V$ DE4 or RE4	$V_{CC} = 3.0V$	-3	-20	$\mu A$
			$V_{CC} = 5.25V$	-7	-20	$\mu A$
$I_{CCD}$	Supply Current <sup>(10)</sup>	No Load, DE/RE and DE4 = 2.0V		75	90	mA
$I_{CCR}$	Supply Current <sup>(10)</sup>	No Load, DE/RE and RE4 = 0.8V		50	70	mA

(5)  $I_{IH}$  and  $I_{IL}$  include driver input current and receiver TRI-STATE leakage current on DR(1–3).

(6) Short one output at a time.

(7) Threshold parameter limits specified as an algebraic value rather than by magnitude.

(8) Hysteresis defined as  $V_{HST} = V_{TH} - V_{TL}$ .

(9)  $I_{IN}$  includes the receiver input current and driver TRI-STATE leakage current.

(10) Total package supply current.

## Switching Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units	
<b>DRIVER SINGLE-ENDED CHARACTERISTICS</b>							
$t_{PZH}$	Output Enable Time to High Level	$R_L = 110\Omega$ ( <a href="#">Figure 6</a> )		35	40	ns	
$t_{PZL}$	Output Enable Time to Low Level		( <a href="#">Figure 8</a> )	25	40	ns	
$t_{PHZ}$	Output Disable Time to High Level		( <a href="#">Figure 6</a> )		15	25	ns
$t_{PLZ}$	Output Disable Time to Low Level		( <a href="#">Figure 8</a> )		35	40	ns
<b>DRIVER DIFFERENTIAL CHARACTERISTICS</b>							
$t_r, t_f$	Rise and Fall Time	$R_L = 54\Omega$ $C_L = 50\text{ pF}$ $C_D = 15\text{ pF}$ ( <a href="#">Figure 3</a> <a href="#">Figure 4</a> <sup>(1)</sup> )		13	16	ns	
$t_{PLHD}$	Differential Propagation		9	15	19	ns	
$t_{PHLD}$	Delays <sup>(2)</sup>		9	12	19	ns	
$t_{SKD}$	$ t_{PLHD} - t_{PHLD} $ Diff. Skew			3	6	ns	
<b>RECEIVER CHARACTERISTICS</b>							
$t_{PLHD}$	Differential Propagation Delays	$C_L = 15\text{ pF}$ $V_{CM} = 2.0V$ ( <a href="#">Figure 10</a> )	9	14	19	ns	
$t_{PHLD}$			9	13	19	ns	
$t_{SKD}$	$ t_{PLHD} - t_{PHLD} $ Diff. Receiver Skew			1	3	ns	
$t_{PZH}$	Output Enable Time to High Level	$C_L = 15\text{ pF}$ ( <a href="#">Figure 15</a> )		15	22	ns	
$t_{PZL}$	Output Enable Time to Low Level			20	30	ns	
$t_{PHZ}$	Output Disable Time from High Level			20	30	ns	
$t_{PLZ}$	Output Disable Time from Low Level			17	25	ns	

(1) Propagation Delay Timing for Calculations of Driver Differential Propagation Delays

(2) Differential propagation delays are calculated from single-ended propagation delays measured from driver input to the 20% and 80% levels on the driver outputs ([Figure 16](#)).

PARAMETER MEASUREMENT INFORMATION

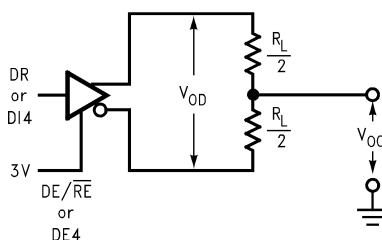


Figure 1. Driver  $V_{OD}$  and  $V_{OC}$ <sup>(3)</sup>

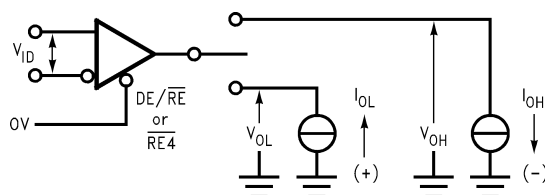
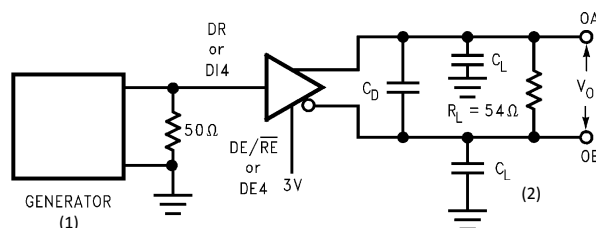
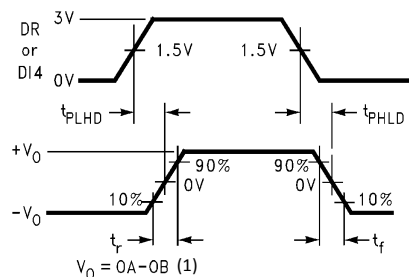


Figure 2. Receiver  $V_{OH}$  and  $V_{OL}$



- (1) The input pulse is supplied by a generator having the following characteristics:  $f = 1.0$  MHz, 50% duty cycle,  $\text{trand} \text{tf} < 6.0$  ns,  $Z_0 = 50\Omega$
- (2)  $C_L$  includes probe and stray capacitance.

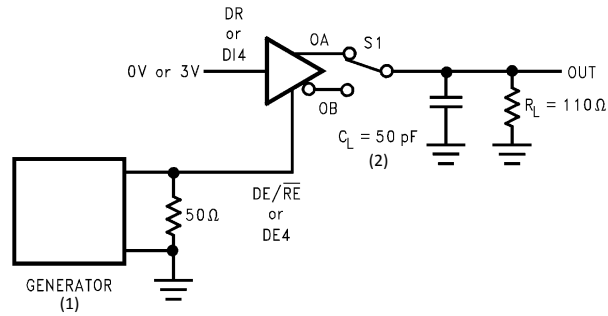
Figure 3. Driver Differential Propagation Delay Load Circuit



- (1) Differential propagation delays are calculated from single-ended propagation delays measured from driver input to the 20% and 80% levels on the driver outputs (Figure 16).

Figure 4. Driver Differential Propagation Delays and Transition Times

(3)  $C_L$  includes probe and stray capacitance.

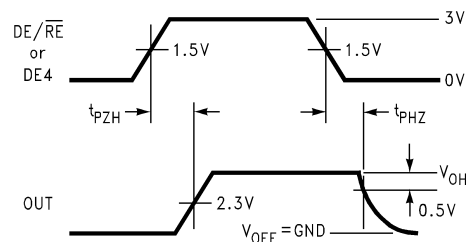


S1 to OA for DI = 3V

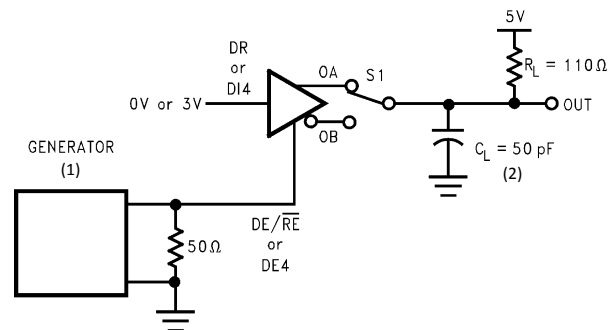
S1 to OB for DI = 0V

- (1) The input pulse is supplied by a generator having the following characteristics:  $f = 1.0$  MHz, 50% duty cycle,  $\text{trand tf} < 6.0$  ns,  $Z_O = 50\Omega$ .
- (2)  $C_L$  includes probe and stray capacitance.

**Figure 5.**



**Figure 6. Driver Enable and Disable Timing ( $t_{PZH}$ ,  $t_{PHZ}$ )**



S1 to OA for DI = 0V

S1 to OB for DI = 3V

- (1) The input pulse is supplied by a generator having the following characteristics:  $f = 1.0$  MHz, 50% duty cycle,  $\text{trand tf} < 6.0$  ns,  $Z_O = 50\Omega$ .
- (2)  $C_L$  includes probe and stray capacitance.

**Figure 7.**

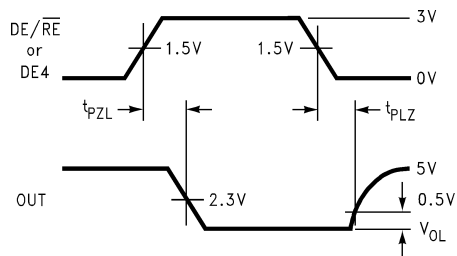
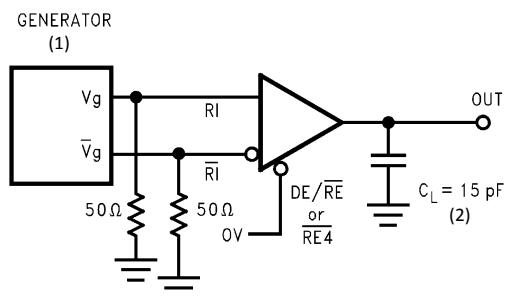


Figure 8. Driver Enable and Disable Timing ( $t_{PZL}$ ,  $t_{PLZ}$ )



- (1) The input pulse is supplied by a generator having the following characteristics:  $f = 1.0$  MHz, 50% duty cycle,  $\text{trand} \text{tf} < 6.0$  ns,  $Z_O = 50\Omega$ .
- (2)  $C_L$  includes probe and stray capacitance.

Figure 9.

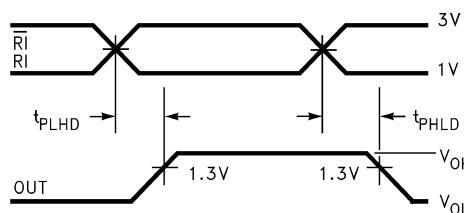
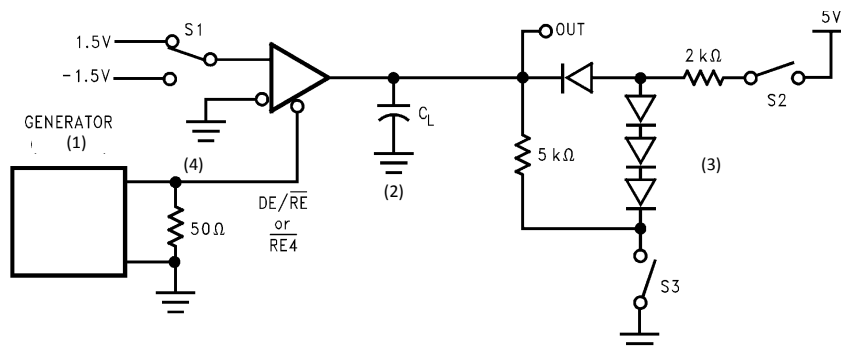
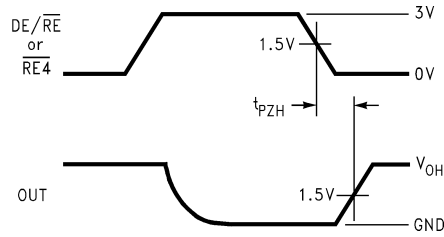


Figure 10. Receiver Differential Propagation Delay Timing



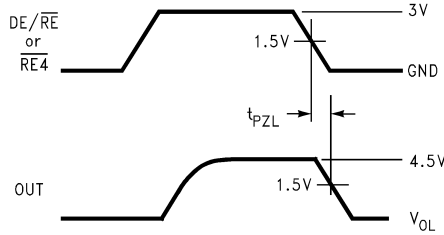
- (1) The input pulse is supplied by a generator having the following characteristics:  $f = 1.0$  MHz, 50% duty cycle,  $\text{trand} \text{tf} < 6.0$  ns,  $Z_O = 50\Omega$ .
- (2)  $C_L$  includes probe and stray capacitance.
- (3) Diodes are 1N916 or equivalent.
- (4) On transceivers 1–3 the driver is loaded with receiver input conditions when DE/RE is high. Do not exceed the package power dissipation limit when testing.

Figure 11.



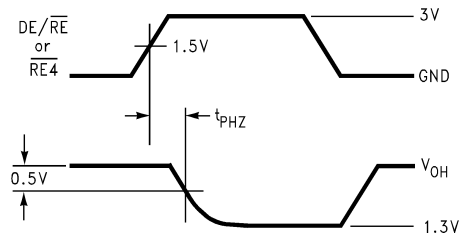
S1 1.5V  
S2 Open  
S3 Closed

Figure 12.



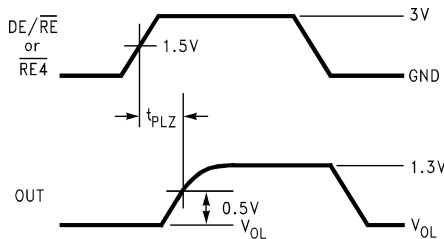
S1 -1.5V  
S2 Closed  
C3 Open

Figure 13.



S1 1.5V  
S2 Closed  
C3 Closed

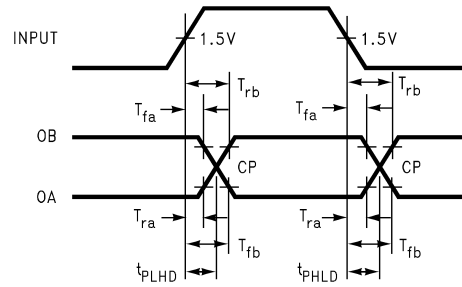
Figure 14.



S1 -1.5V  
S2 Closed  
C3 Closed

Figure 15. Receiver Enable and Disable Timing





$$T_{CP} = \frac{(T_{fb} \times T_{rb}) - (T_{ra} \times T_{fa})}{T_{rb} - T_{ra} - T_{fa} + T_{fb}}$$

T<sub>ra</sub>, T<sub>rb</sub>, T<sub>fa</sub> and T<sub>fb</sub> are propagation delay measurements to the 20% and 80% levels.

T<sub>CP</sub> = Crossing Point

**Figure 16. Propagation Delay Timing for Calculations of Driver Differential Propagation Delays**

## REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format .....	<a href="#">9</a>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS36954M/NOPB	ACTIVE	SOIC	DW	20	36	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	0 to 70	DS36954 M	<a href="#">Samples</a>
DS36954MX/NOPB	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	SN	Level-3-260C-168 HR	0 to 70	DS36954 M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

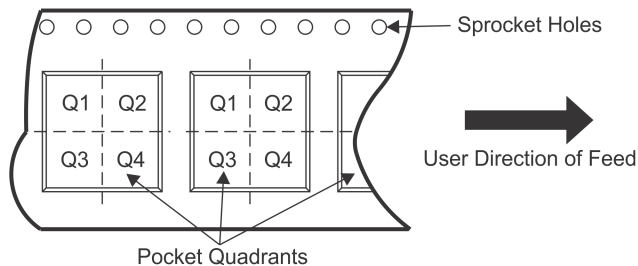
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS36954MX/NOPB	SOIC	DW	20	1000	330.0	24.4	10.9	13.3	3.25	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS36954MX/NOPB	SOIC	DW	20	1000	367.0	367.0	45.0

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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