MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

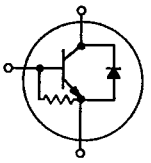
BU508
BU508D
BU508A
BU508AD

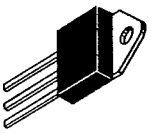
NPN Silicon Power Transistors
Horizontal Deflection

POWER TRANSISTORS
8 AMPERES
1500 VOLTS

. . . specifically designed for use in large screen color deflection circuits.

- Glass Passivated (Patented Photoglass)
- Triple Diffused Mesa Technology for Long Term Stability
- Collector-Emitter Voltage — V_{CE} = 1500 Vdc
- Collector-Emitter Sustaining Voltage — $V_{CEO(sus)}$ = 700 Vdc
- Switching Times with Inductive Loads, t_f = 0.5 μs (Typ) @ I_C = 4.5 A
- Optimum Drive Condition Curves
- Glass Base-Collector Junction
- TO-218 Package for Low Cost Mounting
- Available with Internal Flyback Diode, "D" Suffix


"D" SUFFIX


CASE 340-02
TO-218AC

MAXIMUM RATINGS

Rating	Symbol	All Parts	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	700	Vdc
Collector-Emmiter Voltage	V_{CES}	1500	Vdc
Emitter Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak(1)	I_C I_{CM}	8 15	Adc
Base Current — Continuous Peak(1)	I_B I_{BM}	4 6	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from Case for 5 seconds	T_L	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

3

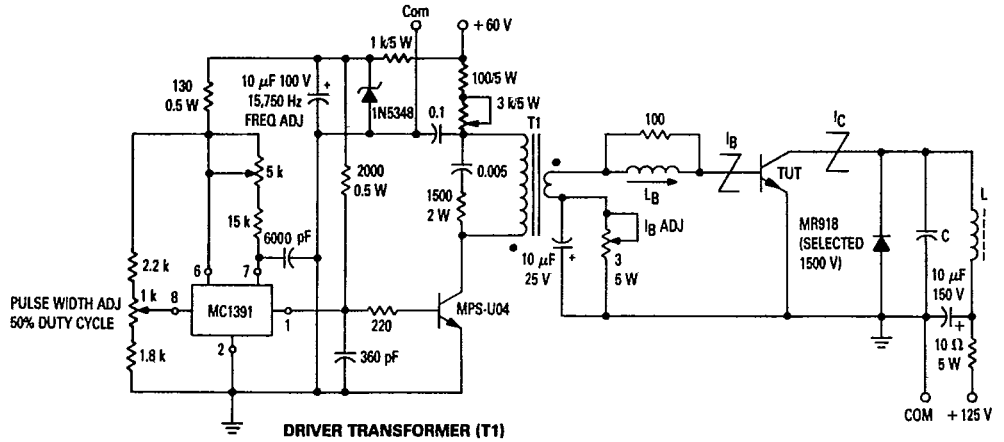
BU508, BU508D, BU508A, BU508AD

T-33-13

ELECTRICAL CHARACTERISTICS (T_C = 25° unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS(1)						
Collector-Emitter sustaining voltage (I_C = 100 mAdc, I_B = 0)		$V_{CEO(sus)}$	700	—	—	Vdc
Collector Cutoff Current (V_{CE} = 1500 Vdc, V_{BE} = 0, T_C = 25°C) (V_{CE} = 1500 Vdc, V_{BE} = 0, T_C = 125°C)		I_{CES}	— —	— —	0.1 2	mAdc
Emitter Base Leakage (V_{EB} = 6 V, I_C = 0)	BU508, A BU508D, AD	I_{EBO}		—	10 300	mAdc
ON CHARACTERISTICS(1)						
DC Current Gain (I_C = 4.5 Adc, V_{CE} = Vdc)		h_{FE}	2.25	—	—	—
Collector-Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)	BU508, D BU508A, AD	$V_{CE(sat)}$	—	—	3 1	Vdc
Base Emitter Saturation Voltage (I_C = 4.5 Adc, I_B = 2 Adc)		$V_{BE(sat)}$	—	—	1.3	Vdc
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$	See Figure 11			
DYNAMIC CHARACTERISTICS						
Current-Gain — Bandwidth Product (I_C = 0.1 Adc, V_{CE} = 5 Vdc, f_{test} = 1 MHz)		f_T	—	7	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)		C_{ob}	—	125	—	pF
SWITCHING CHARACTERISTICS						
Fall Time	(I_C = 4.5 Adc, I_B = 1.8 Adc, LB = 10 μH, see Figure 1)	t_s t_f		8 0.5		μs

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.



I_C A	L mH	C μF
3.5	0.87	0.013
4.5	0.67	0.017

DRIVER TRANSFORMER (T1)

- Ferrox cube pot core #4229P-L00-3C8
- Adjust gap for primary inductance Lp = 70 mH (approximately 5 mil spacer)
- Primary 230T #28 AWG (5 layers)
- Secondary 15T #22 AWG (1 layer)
- Secondary leakage inductance should be less than 3 μH
- Use 3 mil mylar tape between each winding layer

Figure 1. Switching Times Test Circuit

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BASE DRIVE: The Key to Performance

By now, the concept of controlling the shape of the turn-off base current is widely accepted and applied in horizontal deflection design. The problem stems from the fact that good saturation of the output device, prior to turn-off, must be assured. This is accomplished by providing more than enough I_{B1} to satisfy the lowest gain output device h_{FE} at the end of scan I_{CM}. Worst-case component variations and maximum high voltage loading must also be taken into account.

If the base of the output transistor is driven by a very low impedance source, the turn-off base current will reverse very quickly as shown in Figure 2. This results in rapid, but only partial, collector turn-off, because excess carriers become trapped in the high resistivity collector and the transistor is still conductive. This is a high dissipation mode, since the collector voltage is rising very rapidly. The problem is overcome by adding inductance to the base circuit to slow the base current reversal as shown in Figure 3, thus allowing excess carrier recombination in the collector to occur while the base current is still flowing.

Choosing the right L_B is usually done empirically, since the equivalent circuit is complex, and since there are several important variables (I_{CM}, I_{B1}, and h_{FE} at I_{CM}). One method is to plot fall time as a function of L_B, at the desired conditions, for several devices within the h_{FE} specification. A more informative method is to plot power dissipation versus I_{B1} for a range of values of L_B. This kind of analysis shows the parameter which really matters is dissipation, whether caused by switching or by saturation. The negative slope of these curves at the left (low I_{B1}) is caused by saturation losses. The positive slope portion at higher I_{B1}, and low values of L_B is due to switching losses as described above. For very low L_B a very narrow optimum is obtained. This occurs when $I_{B1}\ h_{FE} = I_{CM}$, and therefore would be acceptable only for the "typical" device with constant I_{CM}. As L_B is increased, the curves become broader and flatter above the $I_{B1}\ h_{FE} = I_{CM}$ point as the turn-off "tails" are brought under control. Eventually, if L_B is raised too far, the dissipation all across the curve will rise, due to poor *initiation* of switching rather than tailing. Plotting this type of curve family for devices of different h_{FE}, essentially moves the curves to the left or right according to the relation $I_{B1}\ h_{FE}$ = constant. It then becomes obvious that, for a specified I_{CM}, an L_B can be chosen which will give low dissipation over a range of h_{FE} and/or I_{B1}. The only remaining decision is to pick I_{B1} high enough to accommodate the lowest h_{FE} part specified. Neither L_B nor I_{B1} are absolutely critical, and should be selected for the specific required condition. Similar curves relating to this discussion can be found on Motorola's data sheet for the BU207.

TEST CIRCUIT WAVEFORMS

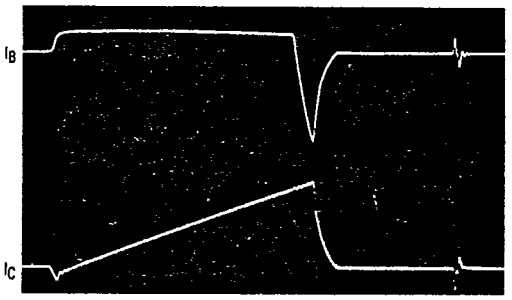

Figure 2.

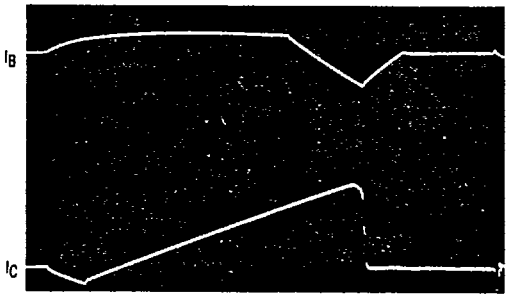

Figure 3.

TEST CIRCUIT OPTIMIZATION

The test circuit may be used to evaluate devices in the conventional manner, i.e., to measure fall time, storage time, and saturation voltage. However, this circuit was designed to evaluate devices by a simple criterion, power supply input. Excessive power input can be caused by a variety of problems, but it is the dissipation in the transistor that is of fundamental importance. Once the required transistor operating current is determined, fixed circuit values may be selected from the table. Factory testing is performed by reading the current meter only, since the input power is proportional to current. No adjustment of the test apparatus is required.

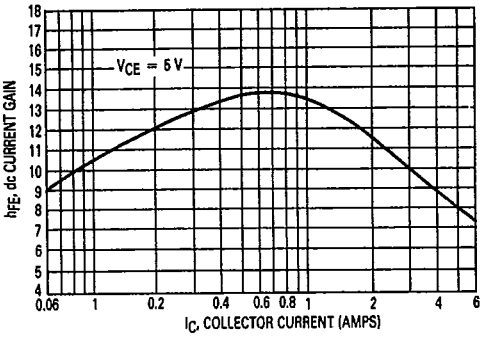

Figure 4. Typical dc Current Gain

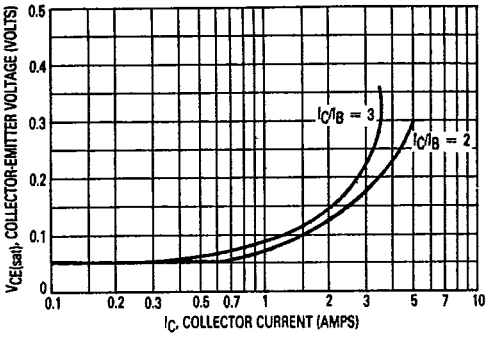

Figure 5. Typical Collector Saturation Voltage

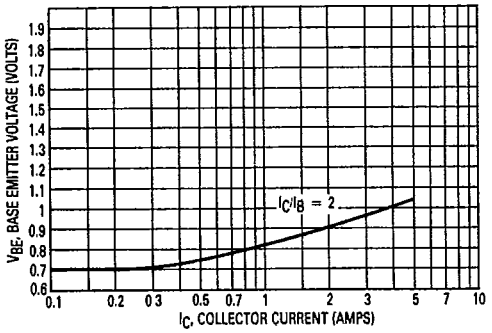

Figure 6. Typical Base Emitter Saturation Voltage

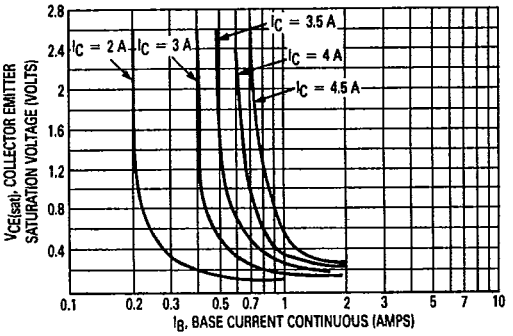

Figure 7. Typical Collector Saturation Region

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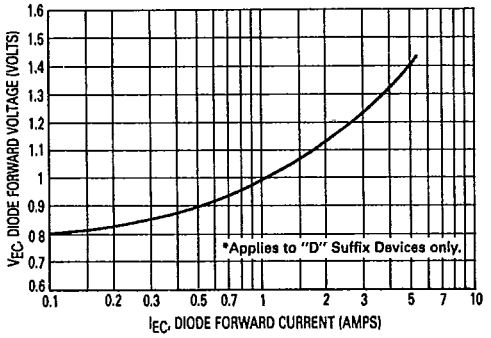


Figure 8. Typical Damper Diode Forward Voltage*

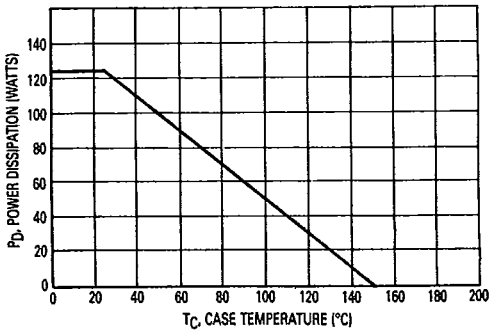


Figure 9. Power-Temperature Derating Curve

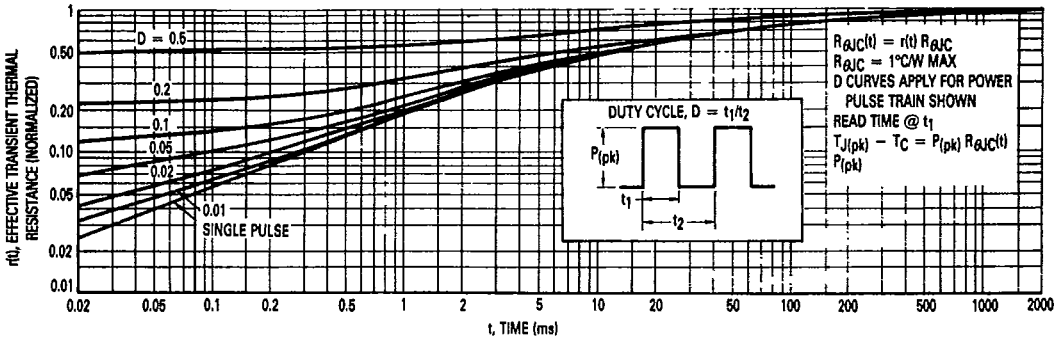


Figure 10. Thermal Response

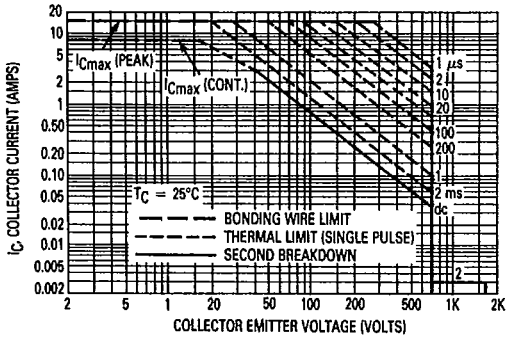
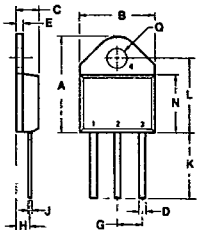


Figure 11. Maximum Forward Biased Safe Operating Area

Note (2) Operation in this area limited to Pulse Width < 20 μs, Duty Cycle < 0.25, R_{BE} < 100 ohms

CASE 340-02
TO-218AC

STYLE 1
PIN 1 BASE 3. EMITTER
2 COLLECTOR 4 COLLECTOR



DIM	MILLIMETERS MIN	MAX	INCHES MIN	MAX
A	20 32	21 08	0 800	0 830
B	15 49	15 90	0 610	0 626
C	4 19	5 08	0 165	0 200
D	1 02	1 65	0 040	0 065
E	1 35	1 65	0 053	0 065
G	5 21	5.72	0 205	0 225
H	2 41	3 20	0 095	0 126
J	0 38	0 64	0 015	0 025
K	12 70	15.49	0 500	0 610
L	15 88	16 51	0 625	0 650
N	12 19	12.70	0 480	0 500
Q	4 04	4 22	0 159	0.166

3