UNITRODE

UCC1913
UCC2913
UCC3913

Negative Voltage Hot Swap Power Manager

FEATURES

- Precision Fault Threshold
- Programmable Average Power Limiting
- Programmable Linear Current Control
- Programmable
- Overcurrent Limit
- Programmable Fault Time
- Fault Output Indication
- Shutdown Control
- Undervoltage Lockout
- 8-Pin SOIC

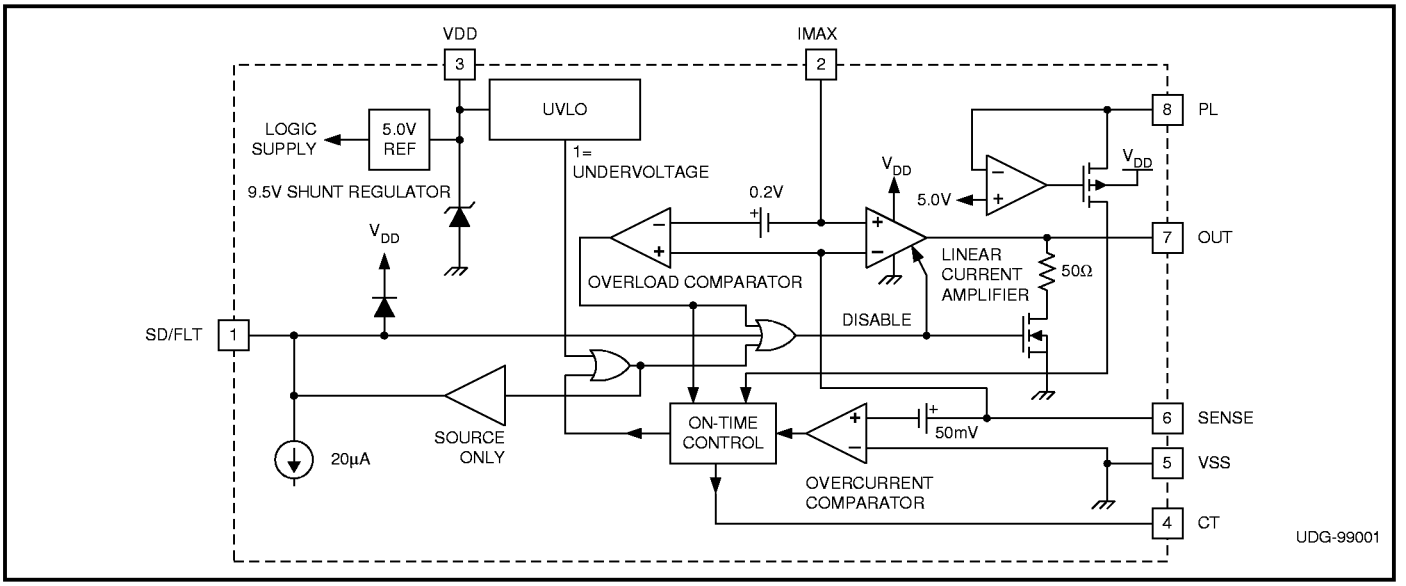
DESCRIPTION

The UCC1913 family of negative voltage circuit breakers provides complete power management, hot swap, and fault handling capability. The IC is referenced to the negative input voltage and is driven through an external resistor connected to ground, which is essentially a current drive as opposed to the traditional voltage drive. The on-board 10V shunt regulator protects the IC from excess voltage and serves as a reference for programming the maximum allowable output sourcing current during a fault. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, soft start time, and average power limiting. In the event of a constant fault, the internal timer will limit the on-time from less than 0.1% to a maximum of 3%. The duty cycle modulates depending on the current into the PL pin, which is a function of the voltage across the FET, and will limit average power dissipation in the FET. The fault level is fixed at 50mV across the current sense amplifier to minimize total dropout. The fault current level is set with an external current sense resistor. The maximum allowable sourcing current is programmed with a voltage divider from VDD to generate a fixed voltage on the IMAX pin. The current level, when the output appears as a current source, is equal to V_{IMAX}/R_{SENSE}. If desired, a controlled current startup can be programmed with a capacitor on the IMAX pin.

When the output current is below the fault level, the output device is switched on. When the output current exceeds the fault level, but is less than the maximum sourcing level programmed by the IMAX pin, the output remains switched on, and the fault timer starts charging CT. Once CT charges to 2.5V, the output device is turned off and performs a retry some time later. When the output current reaches the maximum sourcing current level, the output appears as a current source, limiting the output current to the set value defined by IMAX.

Other features of the UCC1913 family include undervoltage lockout, and 8-pin small outline (SOIC) and Dual-In-Line (DIL) packages.

BLOCK DIAGRAM



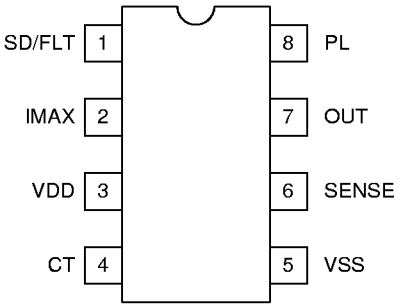
ABSOLUTE MAXIMUM RATINGS

I_{VCC} 50mA
SHUTDOWN Current 10mA
PL Current 10mA
IMAX Input Voltage VCC
Storage Temperature . . . . . –65°C to +150°C
Junction Temperature . . . . . –55°C to +150°C
Lead Temperature (Soldering, 10 sec.) . . . . . +300°C

All voltages are with respect to VSS (The most negative voltage). All currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

CONNECTION DIAGRAMS

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1913; –40°C to +85°C for UCC2913; 0°C to +70°C for UCC3913; I_{VDD} = 2mA, CT = 4.7pF, $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VDD Section					
IDD			1.0	2.0	mA
Regulator Voltage	I_{SOURCE} = 2mA to 10mA	8.5	9.5	10.5	V
UVLO Off Voltage		6	7	8	V
Fault Timing Section					
Overcurrent Threshold	T_J = 25°C	47.5	50	53	mV
	Over Operating Temperature	46	50	53.5	mV
Overcurrent Input Bias			50	500	nA
CT Charge Current	V_{CT} = 1.0V, I_{PL} = 0	–50	–36	–22	µA
	Overload Condition, $V_{SENSE} – V_{IMAX}$ = 300mV	–1.7	–1.2	–0.7	mA
CT Discharge Current	V_{CT} = 1.0V, I_{PL} = 0	0.6	1	1.5	µA
CT Fault Threshold		2.2	2.4	2.6	V
CT Reset Threshold		0.32	0.5	0.62	V
Output Duty Cycle	Fault Condition, I_{PL} = 0	1.7	2.7	3.7	%
Output Section					
Output High Voltage	I_{OUT} = 0A	8.5	10		V
	I_{OUT} = –1mA	6	8		V
Outut Low Voltage	I_{OUT} = 0A; $V_{SENSE} – V_{IMAX}$ = 100mV		0	0.01	V
	I_{OUT} = 2mA; $V_{SENSE} – V_{IMAX}$ = 100mV		0.2	0.6	V
Linear Amplifier Section					
Sense Control Voltage	IMAX = 100mV	85	100	115	mV
	IMAX = 400mV	370	400	430	mV
Input Bias			50	500	nA
Shutdown/Fault Section					
Shutdown Threshold		1.4	1.7	2.0	V
Input Current	Shutdown = 5V	15	25	45	µA
Fault Output High		6	7.5	9	V
Fault Output Low			0	0.01	V
Delay to Output	(Note 1)		150	300	ns

ELECTRICAL CHARACTERISTICS: Unless otherwise stated these specifications apply for T_A = –55°C to +125°C for UCC1913; –40°C to +85°C for UCC2913; 0°C to +70°C for UCC3913, I_{VDD} = 2mA, CT = 4.7pF, $T_A = T_J$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Limiting Section					
V_{SENSE} Regulator Voltage	I_{PL} = 64µA	4.35	4.85	5.35	V
Duty Cycle Control	I_{PL} = 64µA	0.6	1.2	1.7	%
	I_{PL} = 1mA	0.045	0.1	0.17	%
Overload Section					
Delay to Output	(Note 1)		300	500	ns
Output Sink Current	$V_{SENSE} = V_{IMAX}$ = 300mV	40	100		mA
Threshold	Relative to IMAX	140	200	260	mV

Note 1: Guaranteed by design. Not 100% tested in production.

PIN DESCRIPTIONS

CT: A capacitor is connected to this pin in order to set the maximum fault time. The maximum fault time must be more than the time to charge external load capacitance. The maximum fault time is defined as:

$$T_{FAULT} = \frac{(2 \bullet CT)}{I_{CH}}$$

where

$$I_{CH} = 36\mu A + I_{PL},$$

and I_{PL} is the current into the power limit pin. Once the fault time is reached the output will shutdown for a time given by:

$$T_{SD} = 2 \bullet 106 \bullet CT$$

IMAX: This pin programs the maximum allowable sourcing current. Since VDD is a regulated voltage, a voltage divider can be derived from VDD to generate the program level for the IMAX pin. The current level at which the output appears as a current source is equal to the voltage on the IMAX pin over the current sense resistor. If desired, a controlled current startup can be programmed with a capacitor on the imax pin, and a programmed start delay can be achieved by driving the shutdown with an open collector/drain device into an RC network.

OUT: Output drive to the MOSFET pass element.

PL: This feature ensures that the average MOSFET power dissipation is controlled. A resistor is connected from this pin to the drain of the NMOS pass element. When the voltage across the NMOS exceeds 5V, current will flow into the PL pin which adds to the fault timer charge current, reducing the duty cycle from the 3% level. When I_{PL}>>36µA then the average MOSFET power dissipation is given by:

$$P_{FET(avg)} = IMAX \bullet 1 \bullet 10^{-6} \bullet R_{PL}$$

SENSE: Input voltage from the current sense resistor. When there is greater than 50mV across this pin with respect to VSS, then a fault is sensed, and CT starts to charge.

SD/FLT: This pin provides fault output indication and shutdown control. Interface into and out of this pin is usually performed through level shift transistors. When 20µA is sourced into this pin, shutdown drives high causing the output to disable the NMOS pass device. When opened, and under a non-fault condition, the SD/FLT pin will pull to a low state. When a fault is detected by the fault timer, or undervoltage lockout, this pin will drive to a high state, indicating the output FET is off.

VDD: Current driven with a resistor to a voltage at least 10V more positive than VSS. Typically a resistor is connected to ground. The 10V shunt regulator clamps VDD at 10V above the VSS pin, and is also used as an output reference to program the maximum allowable sourcing current.

VSS: Ground reference for the IC and the most negative voltage available.

APPLICATION INFORMATION

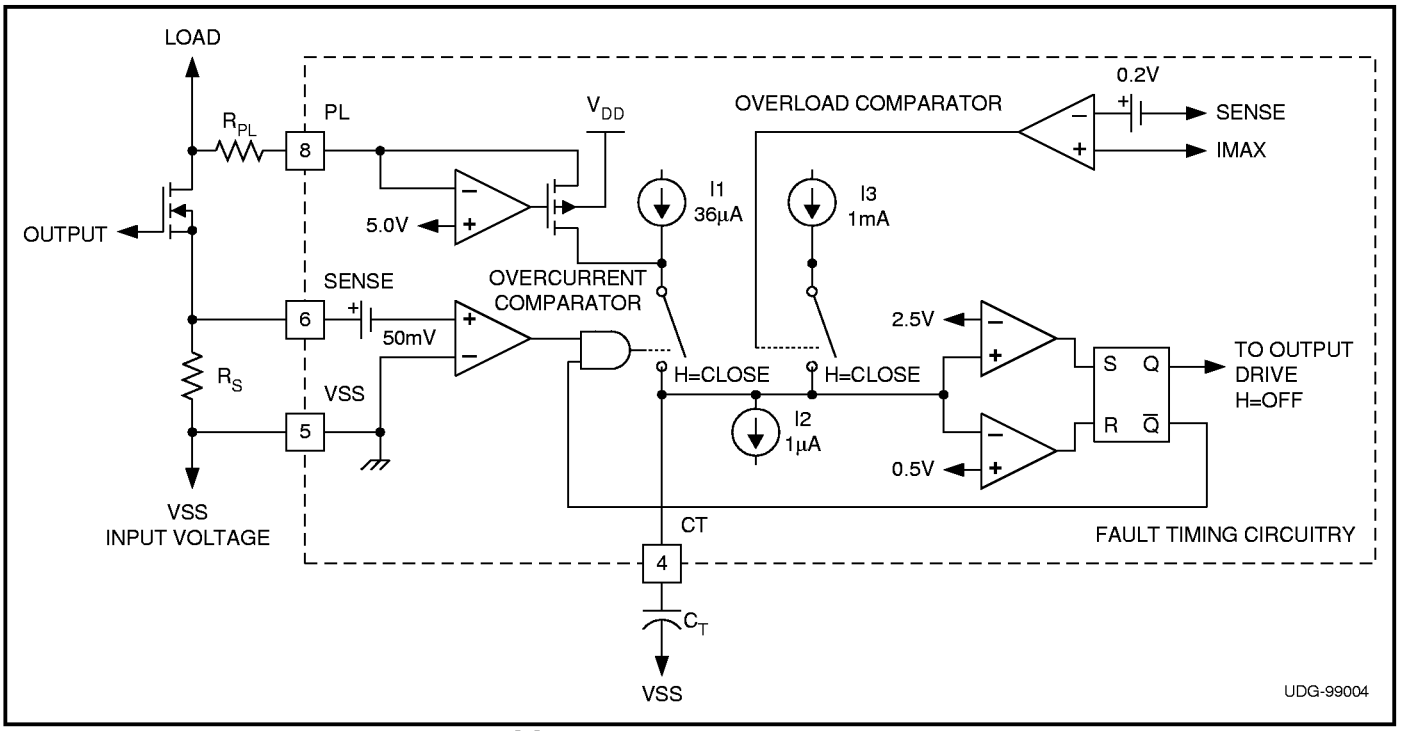


Figure 1. Fault timing circuitry for the UCC1913, including power limit overload.

Figure 1 shows the detailed circuitry for the fault timing function of the UCC1913. For the time being, we will discuss a typical fault mode, therefore, the overload comparator, and current source I3 does not work into the operation. Once the voltage across the current sense resistor, R_S, exceeds 50mV, a fault has occurred. This causes the timing capacitor to charge with a combination of 36µA plus the current from the power limiting amplifier. The PL amplifier is designed to only source current into the CT pin and to begin sourcing current once the voltage across the output FET exceeds 5V. The current I_{PL} is related to the voltage across the FET with the following expression:

$$I_{PL} = \frac{V_{FET} - 5V}{R_{PL}}$$

Where V_{FET} is the voltage across the NMOS pass device.

Later it will be shown how this feature will limit average power dissipation in the pass device. Note that under a condition where the output current is more than the fault level, but less than the max level, V_{OUT} ~ VSS (input voltage), I_{PL} = 0, the CT charging current is 36µA.

During a fault, CT will charge at a rate determined by the internal charging current and the external timing capacitor. Once CT charges to 2.5V, the fault comparator switches and sets the fault latch. Setting of the fault latch causes both the output to switch off and the charging switch to open. CT must now discharge with the 1µA current source, I2, until 0.5V is reached. Once the voltage at CT reaches 0.5V, the fault latch resets, which re-enables the output and allows the fault circuitry to regain control of the charging switch. If a fault is still present, the fault comparator will close the charging switch causing the cycle to begin. Under a constant fault, the duty cycle is given by:

$$Duty\,Cycle = \frac{1\mu A}{I_{PL} + 36\,\mu A}$$

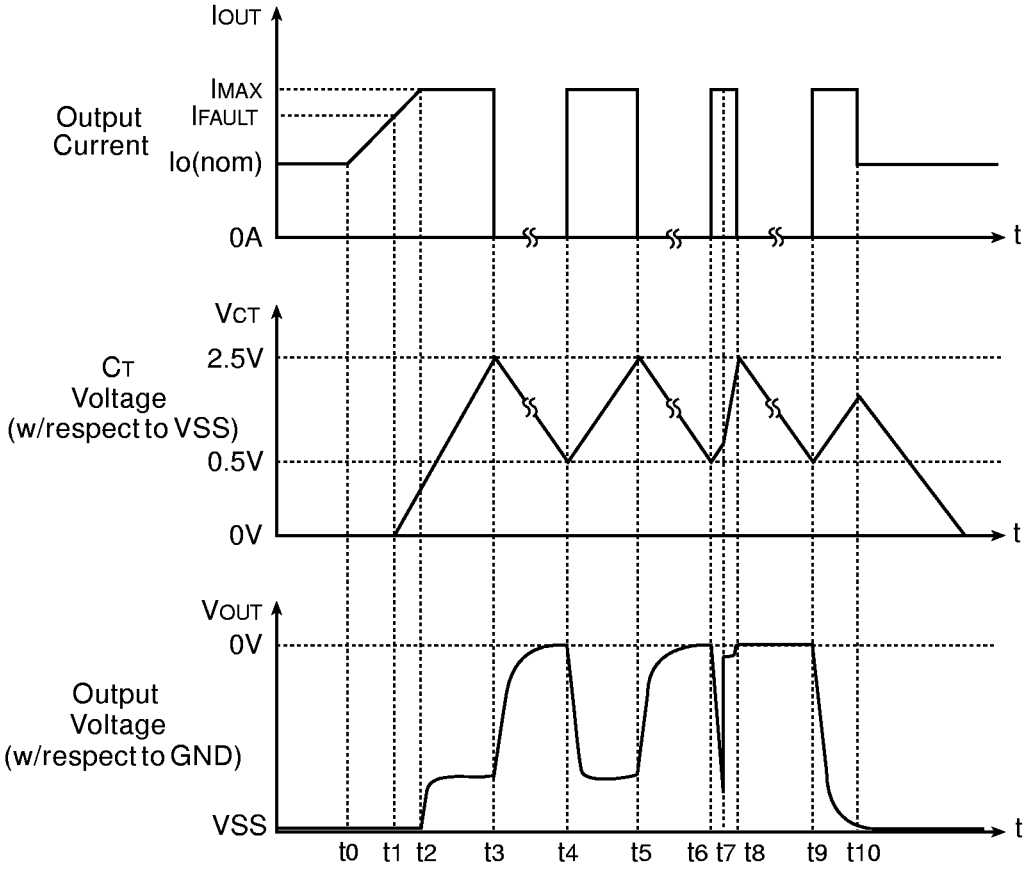
Average power dissipation in the pass element is given by:

$$P_{FET(avg)} = V_{FET} \bullet IMAX \bullet \frac{1\mu A}{I_{PL} + 36\,\mu A}$$

where V_{FET} >> 5V I_{PL} can be approximated as : $\frac{V_{FET}}{R_{PL}}$

and where I_{PL}>>36µA, the duty cycle can be approximated as :

APPLICATION INFORMATION (cont.)



t0: safe condition – output current is nominal, output voltage is at the negative rail, VSS.

t1: fault control reached – output current rises above the programmed fault value, CT begins to charge at ≅ 36µA.

t2: max current reached – output current reaches the programmed maximum level and becomes a constant current with value I_{MAX}.

t3: fault occurs – CT has charged to 2.5V, fault output goes high, the FET turns off allowing no output current to flow, V_{OUT} floats up to ground.

t4: retry – CT has discharged to 0.5V, but fault current is still exceeded, CT begins charging again, FET is on, V_{OUT} pulled down to VSS.

t5: t5 = t3: illustrates 3%duty cycle.

t6: t6 = t4

t7: output short circuit - if V_{OUT} is short circuited to ground, CT charges at a higher rate depending upon the values for VSS and R_{PL}.

t8: fault occurs – output is still short circuited, but the occurrence of a fault turns the FET off so no current is conducted.

t9: t9 = t4; output short circuit released, still in fault mode.

t10: t10 = t0; fault released, safe condition – return to normal operaton of the circuit breaker.

Figure 2. Typical timing diagram.

APPLICATION INFORMATION (cont.)

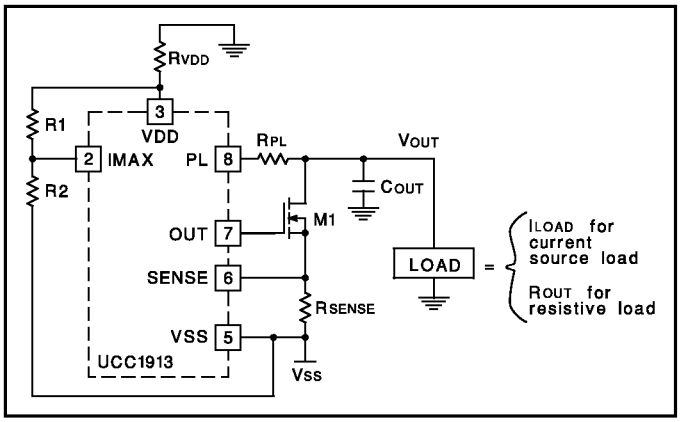


Figure 3.

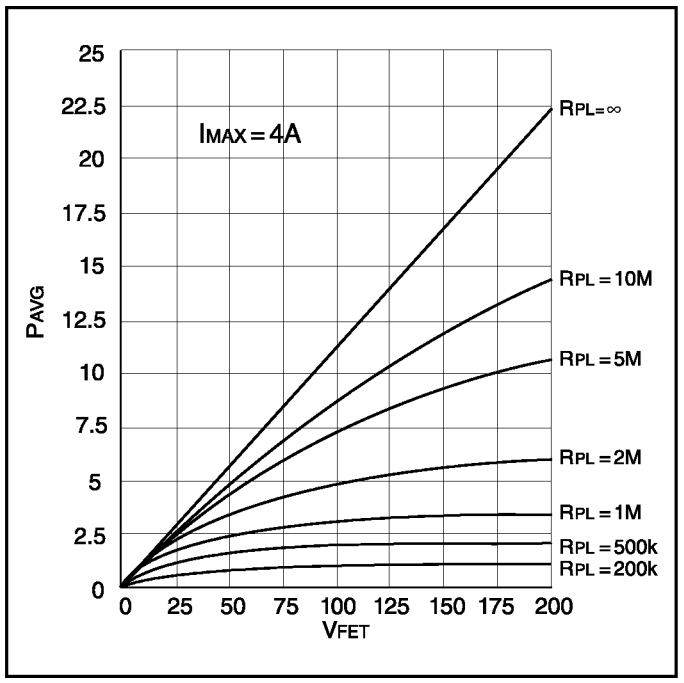


Figure 4. Plot average power vs. FET voltage for increasing values of R_{PL}.

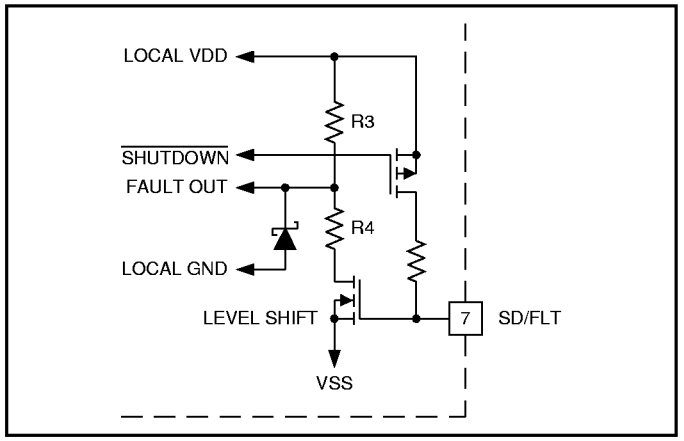


Figure 5. Possible level shift circuitry to interface to the UCC1913.

$$\frac{1\mu A \bullet R_{PL}}{V_{FET}}$$

Therefore, the maximum average power dissipation in the MOSFET can be approximated by:

$$P_{FET(avg)} =$$

$$V_{FET} \bullet IMAX \bullet \frac{1\mu A \bullet R_{PL}}{V_{FET}} = IMAX \bullet 1\mu A \bullet R_{PL}$$

Notice that in the approximation, V_{FET} cancels. therefore, average power dissipation is limited in the NMOS pass element.

Overload Comparator

The linear amplifier in the UCC1913 ensures that the output NMOS does not pass more than I_{MAX} (which is V_{IMAX}/R_S). In the event the output current exceeds the programmed I_{MAX} by 0.2V/R_S, which can only occur if the output FET is not responding to a command from the IC, the CT pin will begin charging with I3, 1mA, and continue to charge to approximately 8V. This allows a constant fault to show up on the SD/FLT pin, and also since the voltage on CT will only charge past 2.5V in an overload fault mode, it can be used for detection of output FET failure or to build in redundancy in the system.

Determining External Component Values

Referring now to Figure 3. To set R_{VDD} the following must be achieved:

$$\frac{V_{IN(min)}}{R_{VDD}} > \frac{10V}{(R1+R2)} + 2mA$$

In order to estimate the minimum timing capacitor, C_T, several things must be taken into account. For example, given the schematic below as a possible (and at this point, a standard) application, certain external component values must be known in order to estimate $C_{T(min)}$.

Now, given the values of C_{OUT}, Load, R_{SENSE}, VSS, and the resistors determining the voltage on the IMAX pin, the user can calculate the approximate startup time of the node V_{OUT}. This startup time must be faster than the time it takes for CT to charge to 2.5V (relative to VSS), and is the basis for estimating the minimum value of CT. In order to determine the value of the sense resistor, R_{SENSE}, assuming the user has determined the fault current, R_{SENSE} can be calculated by:

$$R_{SENSE} = \frac{50mV}{I_{FAULT}}$$

APPLICATION INFORMATION (cont.)

Next, the variable I_{MAX} must be calculated. I_{MAX} is the maximum current that the UCC1913 will allow through the transistor, M1, and it can be shown that during startup with an output capacitor the power MOSFET, M1, can be modeled as a constant current source of value I_{MAX} where:

$$I_{MAX} = \frac{V_{IMAX}}{R_{SENSE}}$$

where V_{IMAX} = voltage on pin IMAX.

Given this information, calculation of the startup time is now possible via the following:

Current Source Load:

$$T_{START} = \frac{C_{OUT} \bullet |VSS|}{I_{MAX} - I_{LOAD}}$$

Resistive Load:

$$T_{START} = C_{OUT} \bullet R_{OUT} \bullet \ell n\left(\frac{I_{MAX} \bullet R_{OUT}}{I_{MAX} \bullet R_{OUT} - |VSS|}\right)$$

Once T_{START} is calculated, the power limit feature of the UCC1913 must be addressed and component values derived. Assuming the user chooses to limit the maximum allowable average power that will be associated with the circuit breaker, the power limiting resistor, R_{PL}, can be easily determined by the following:

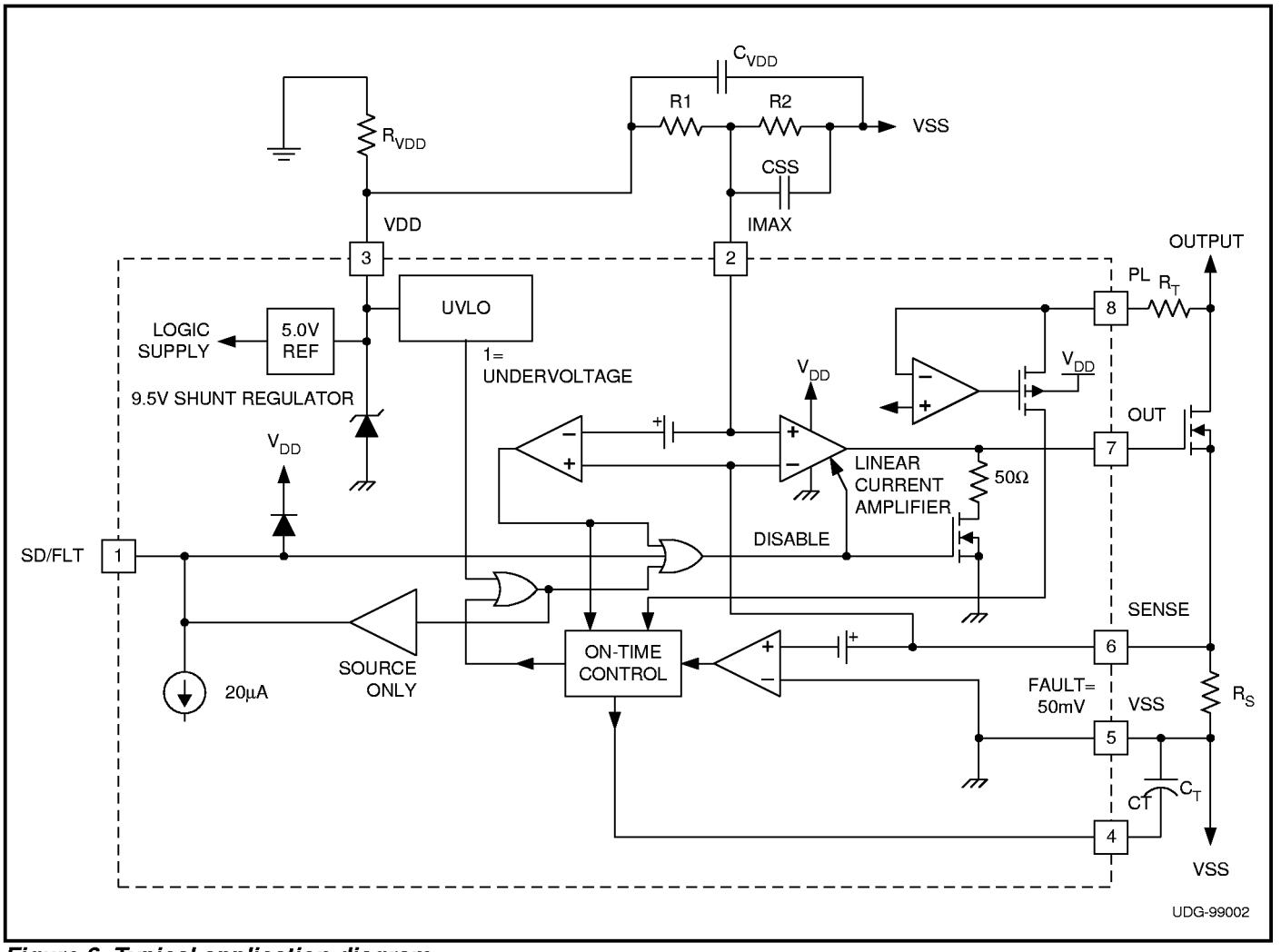


Figure 6. Typical application diagram.

APPLICATION INFORMATION (cont.)

$$R_{PL} = \frac{P_{FET(avg)}}{1\mu A \bullet I_{MAX}}$$

where a minimum R_{PL} exists defined by $R_{PL(min)} = \frac{|VSS|}{5mA}$

Finally, after computing the aforementioned variables, the minimum timing capacitor can be derived as such:

Current Source Load:

$$C_{T(min)} = \frac{(3 \bullet T_{START} \bullet 62\mu A \bullet R_{PL} + |VSS| - 10V)}{10 \bullet R_{PL}}$$

Resistive Load:

$$C_{T(min)} = \frac{3 \bullet T_{START}(31\mu A \bullet R_{PL} + |VSS| - 5V - I_{MAX} \bullet R_{OUT})}{5 \bullet R_{PL}} + \frac{3 \bullet R_{OUT} \bullet |VSS| \bullet C_{OUT}}{5 \bullet R_{PL}}$$

SAFETY RECOMENDATION

Although the UCC3913 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3913 is intended for use in safety critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3913 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot swap benefits of the device.

UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 FAX (603) 424-3460

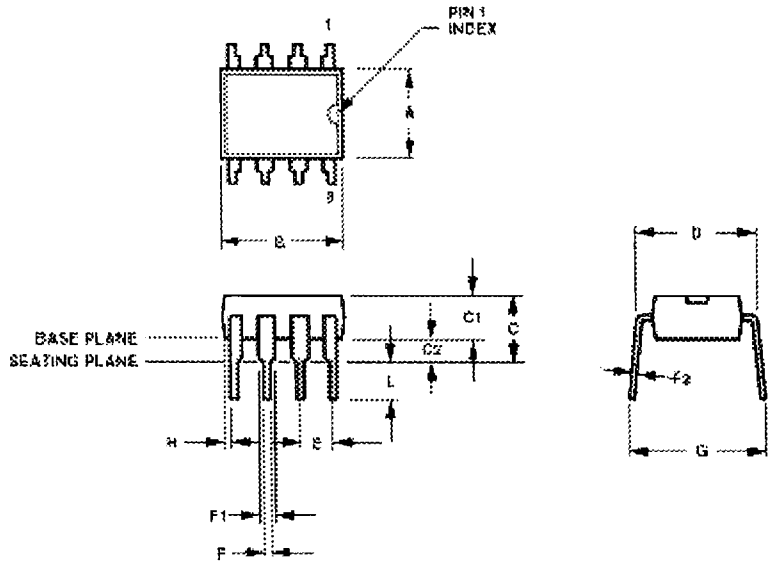
UNITRODE

Mechanical Drawings

Back to Packaging Index

8-PIN PLASTIC DIP ~ N PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	.245	.260	6.22	6.60	1
B	.320	.400	9.40	10.16	1
C	-	.210	-	5.33	
C1	.125	.150	3.18	3.81	
C2	.015	.055	0.38	1.40	2
D	.300	.325	7.62	8.26	3
E	.100 BSC		2.54 BSC		4
F	.014	.022	0.35	0.56	
F1	.045	.070	1.14	1.78	
F2	.008	.014	0.20	0.35	
G	.300	.400	7.62	10.16	5
H	.005	-	0.13	-	
L	.115	.160	2.92	4.06	



NOTES:

1. 'A' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. 'C2' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. 'D' SHALL BE MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO THE BASE PLANE.
4. THE BASIC LEAD SPACING IS 0.100 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.010 IN. OF ITS EXACT TRUE POSITION.
5. 'G' SHALL BE MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
6. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.

P-1

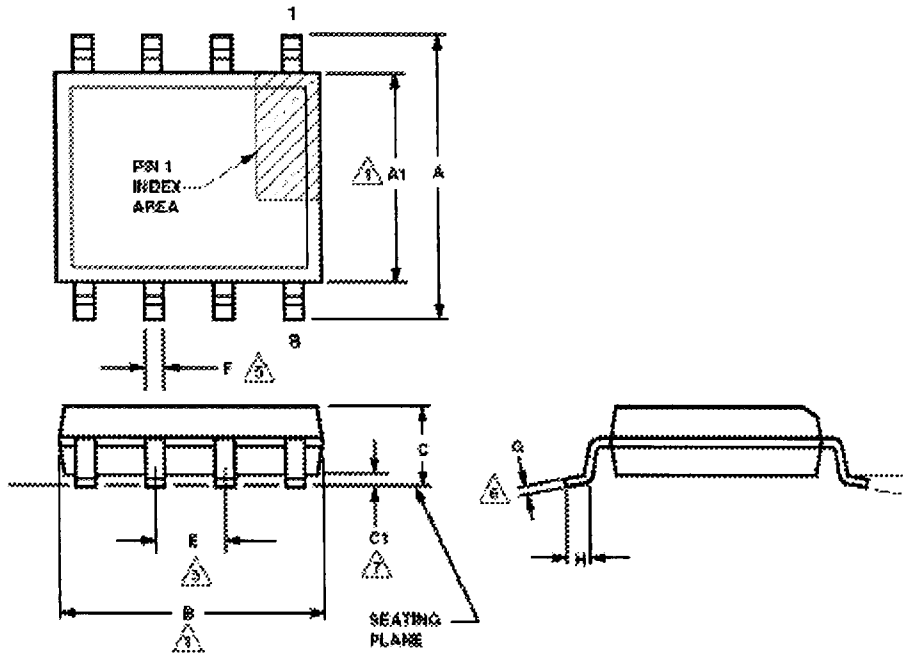
UNITRODE

Mechanical Drawings

Back to Packaging Index

8-PIN SOIC SURFACE MOUNT~ D, DP PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.189	.196	4.80	4.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.23
E	.050 BSC		1.27 BSC	
F	.014	.019	0.35	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

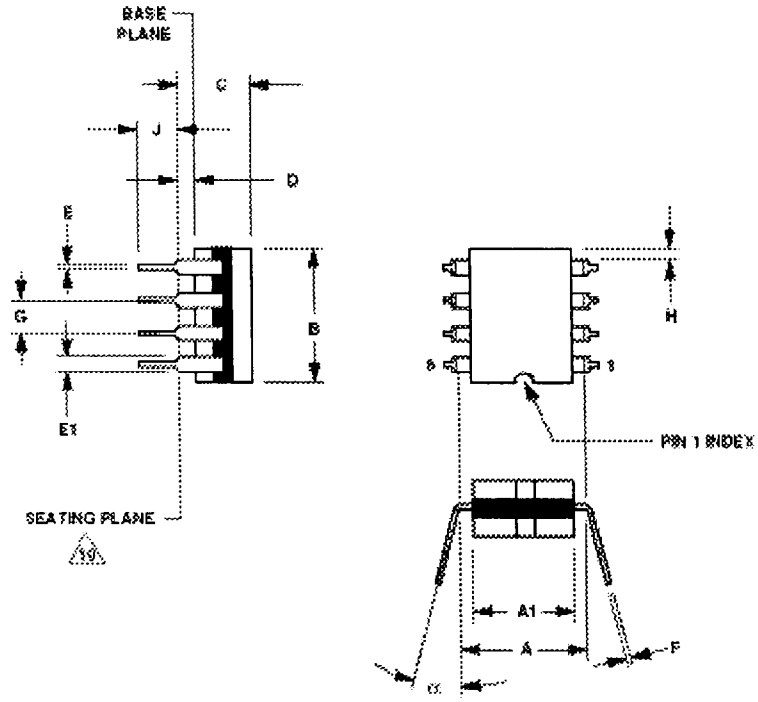
UNITRODE

Mechanical Drawings

Back to Packaging Index

8-PIN CERAMIC DIP ~ J PACKAGE SUFFIX

DIMENSIONS					
	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.290	0.320	7.37	8.13	7
A1	0.220	0.310	5.59	7.87	4
B	-	0.405	-	10.29	4
C	-	0.200	-	5.08	
D	0.015	0.060	0.38	1.52	3
E	0.014	0.026	0.36	0.66	8
E1	0.045	0.065	1.14	1.65	2
F	0.008	0.018	0.20	0.46	8
G	0.100 BSC		2.54 BSC		5
H	0.005	-	0.13	-	6
J	0.125	0.200	3.18	5.08	
α	0°	15°	0°	15°	



NOTES:

1. INDEX AREA: A NOTCH OR A PIN ONE IDENTIFICATION MARK SHALL BE LOCATED ADJACENT TO PIN ONE. THE MANUFACTURER'S IDENTIFICATION SHALL NOT BE USED AS A PIN ONE IDENTIFICATION MARK.
2. THE MINIMUM LIMIT FOR DIMENSION 'E1' MAY BE 0.023 (0.58mm) FOR LEADS NUMBER 1, 4, 5 AND 8 ONLY.
3. DIMENSION 'D' SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
4. THIS DIMENSION ALLOWS FOR OFF-CENTER LID, MENISCUS AND GLASS OVERRUN.
5. THE BASIC PIN SPACING IS 0.100 (2.54mm) BETWEEN CENTERLINES. EACH PIN CENTERLINE SHALL BE LOCATED WITHIN ±0.010 (0.25mm) OF ITS EXACT TRUE POSITION.
6. APPLIES TO ALL FOUR CORNERS (LEADS NUMBER 1, 4, 5 AND 8).
7. DIMENSION 'A' SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS WHEN $\alpha = 0°$.
8. THE MAXIMUM LIMITS OF DIMENSIONS 'E' AND 'F' SHALL BE MEASURED AT THE CENTER OF THE FLAT WHEN SOLDER DIP IS APPLIED.
9. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
10. THE SEATING PLANE IS LOCATED AT THE LOWEST POINT ON THE LEAD AT WHICH THE LEAD WIDTH EXCEEDS 0.040 (1.02mm) MINIMUM, EXCLUDING ANY HALF LEADS AT THE PACKAGE ENDS.