Am27S40/S41

4096 x 4 Bit Generic Series Bipolar IMOX™ PROM
(with ultra fast access time)

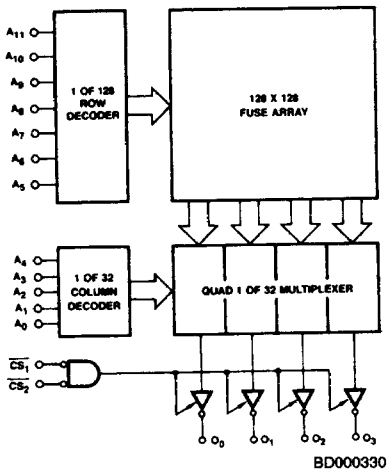
DISTINCTIVE CHARACTERISTICS

- Ultra fast access time "A" version (35ns max) — Fast access time Standard version (50ns max) — allow tremendous system speed improvements
- Platinum-Silicide fuses guarantee high reliability, fast programming and exceptionally high programming yields (typ > 98%)
- AC performance is factory tested utilizing programmed test words and columns
- Voltage and temperature compensated providing extremely flat AC performance over military range
- Member of generic PROM series utilizing standard programming algorithm

GENERAL DESCRIPTION

The Am27S40A, Am27S41A, Am27S40, and Am27S41 are high speed electrically programmable Schottky read only memories. Organized in 4096 x 4 configuration, they are available in both open collector (Am27S40A and Am27S40) and three-state (Am27S41A and Am27S41) output versions. After programming, stored information is read on outputs $O_0 - O_3$ by applying unique binary addresses to $A_0 - A_{11}$ and holding the chip select inputs, $\overline{CS}_1$ and $\overline{CS}_2$, LOW. If either chip select input goes to a logic HIGH, $O_0 - O_3$ go to the OFF or HIGH impedance state.

BLOCK DIAGRAM



PRODUCT SELECTOR GUIDE

Access Time	35ns	50ns		65ns
Temperature Range	C	M	C	M
Open Collector	27S40A	27S40A	27S40	27S40
Three-State	27S41A	27S41A	27S41 27PS41	27S41 27PS41

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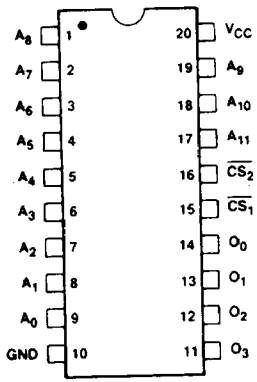
CONNECTION DIAGRAM
Top View

DIP



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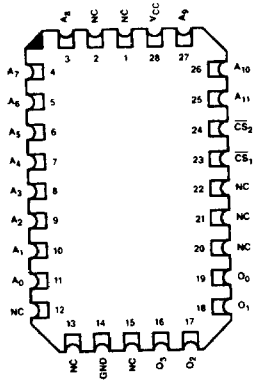
Chip-Pak™



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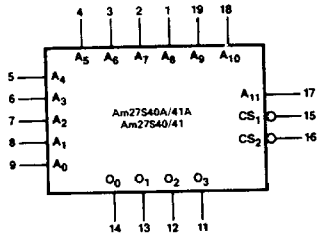
Note: Pin 1 is marked for orientation

LOGIC SYMBOL



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VCC = Pin 20
GND = Pin 10

ORDERING INFORMATION

Am27S40 A P C B

- B — Burn-in Option
  B suffix denotes 160 hour burn-in.
- C — Temperature
  C – Commercial (0°C to +70°C)
  M – Military (–55°C to +125°C)
- P — Package
  D – 20-pin ceramic DIP
  L – 28-pin leadless chip carrier
  P – 20-pin plastic DIP
- A — Speed Select
  See Product Selector Guide
- Am27S40 — Device Type

Am27S40 Am27S40A	Open Collector
Am27S41 Am27S41A	Three State
Am27PS41	Power Switched

Valid Combinations	
Am27S40 Am27S40A Am27S41 Am27S41A Am27PS41	PC, PCB, DC, DCB, LC, LCB, DM, DMB, FM, FMB, LM, LMB

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POWER SWITCHING

The Am27PS41 is a power switched device. When the chip is selected, important internal currents increase from small idling or standby values to their larger selected values. This transition occurs very rapidly, meaning that access times from the powered-down state are only slightly slower than from the powered-up state. Deselected, I_{CC} is reduced to half its full operating amount. Due to this unique feature, there are special considerations which should be followed in order to optimize performance:

1. When the Am27PS41 is selected by a low level on $\overline{CS}_1$, a current surge is placed on the V_{CC} supply due to the power-up feature. In order to minimize the effects of this current transient, it is recommended that a 0.1μf ceramic capacitor be connected from pin 20 to pin 10 at each device. (See Figure 1.)

2. Address access time (t_{AA}) can be optimized if a chip enable set-up time (t_{EAS}) of greater than 25ns is observed. Negative set-up times on chip enable ($t_{EAS} < 0$) should be avoided. (For typical and worse case characteristics, see Figures 2A and 2B.)

OBTAINING PROGRAMMED UNITS

Programmed devices may be purchased from your distributor or Advanced Micro Devices. The program data should be submitted in the form of a punched paper tape and must be accompanied by a written truth table. The punched tape can be delivered with your order or may be transmitted over a TWX machine or a time-sharing terminal. ASCII BPNF is our preferred paper tape format.

Truth tables are also acceptable, but are much less desirable especially for larger density PROMs. Submission of a truth table requires the generation of a punched paper tape at the distributor or factory resulting in longer lead times, greater possibility of error, and higher cost.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Ambient Temperature with
Power Applied ..... −55°C to +125°C
Supply Voltage ..... −0.5V to +7.0V
DC Voltage Applied to Outputs
(Except During Programming) ..... −0.5V to +V_{CC} max
DC Voltage Applied to Outputs
During Programming 21V
Output Current into Outputs During
Programming (Max Duration of 1 sec) 250mA
DC Input Voltage ..... −0.5V to +5.5V
DC Input Current ..... −30mA to +5mA

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

Operating ranges define those limits over which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range unless otherwise specified

Symbol	Parameter	Test Conditions		Min	Typ (Note 1)	Max	Units
V_{OH} (TS Devices only)	Output HIGH Voltage	V_{CC} = MIN, I_{OH} = −2.0mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN, I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}	COM'L			0.45	Volts
			MIL			0.50	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 4)		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 4)				0.8	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX, V_{IN} = 0.45V			−0.020	−0.250	mA
I_{IH}	Input HIGH Current	V_{CC} = MAX, V_{IN} = V_{CC}				40	µA
I_{SC} (TS Devices only)	Output Short Circuit Current	V_{CC} = MAX, V_{OUT} = 0.0V (Note 2)	COM'L	−20	−40	−90	mA
			MIL	−15	−40	−90	
I_{CC}	Power Supply Current	All inputs = GND, V_{CC} = MAX $\overline{CS}_1$ = 2.7V, All other inputs = GND	COM'L		110	165	mA
			MIL		110 50	170 85	
V_I	Input Clamp Voltage	V_{CC} = MIN, I_{IN} = −18mA				−1.2	Volts
I_{CEX}	Output Leakage Current	V_{CC} = MAX $\overline{CS}_1$ = 2.4V	V_O = V_{CC}			40	µA
			V_O = 0.4V			−40	
C_{IN}	Input Capacitance	V_{IN} = 2.0V @ f = 1MHz (Note 3)			5.0		pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0V @ f = 1MHz (Note 3)			8.0		

Notes:

1. Typical limits are at V_{CC} = 5.0V and T_A = 25°C.
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.
3. These parameters are not 100% tested, but are periodically sampled.
4. These are absolute voltages with respect to device ground pin and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

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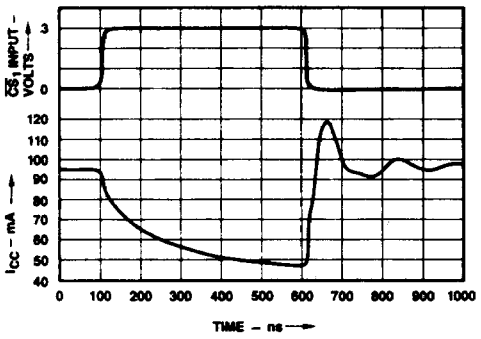
DC OPERATING CHARACTERISTICS

Typical I_{CC} Current Surge without 0.1mF
(I_{CC} is Current Supplied by V_{CC} Power Supply)



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Typical I_{CC} Current Surge with 0.1mF
(I_{CC} is Current Supplied by V_{CC} Power Supply)

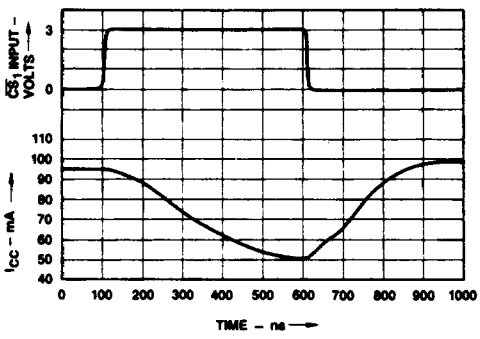

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Figure 1. I_{CC} Current

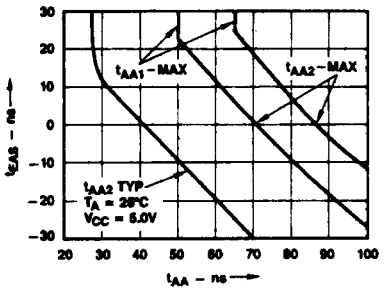

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Figure 2A. t_{AA} versus t_{EAS}

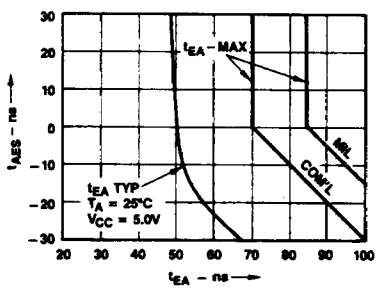

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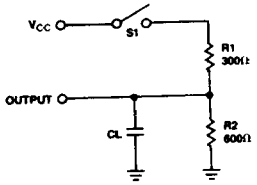
Figure2B. t_{EA} versus t_{AES}

SWITCHING TEST CIRCUIT



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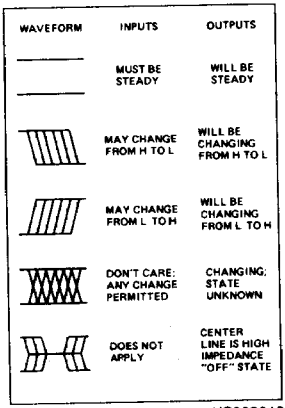
KEY TO SWITCHING WAVEFORMS



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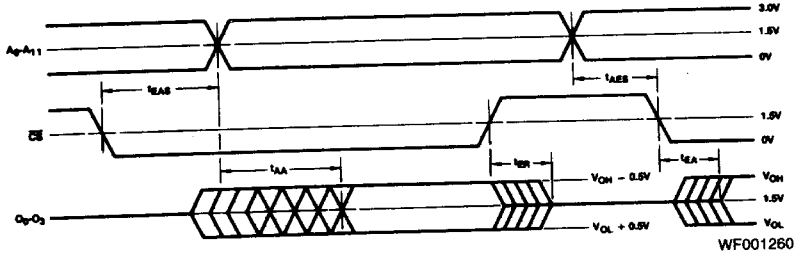
SWITCHING CHARACTERISTICS over operating range unless otherwise specified

No.	Symbol	Description		27S C devices Min	27S C devices Max	27S M devices Min	27S M devices Max	27PS C devices Min	27PS C devices Max	27S M devices Min	27S M devices Max	Units
1	t_{AA}	Address Access Time	STD		50		65		50		65	ns
			A		35		50					
2	t_{EA}	Enable Access Time	STD		25		30		70		85	
			A		25		30					
3	t_{ER}	Enable Recovery Time	STD		25		30		25		30	
			A		25		30					
4	t_{AAPS}	Power Switched Address Access Time (27PS devices only)	STD						70		85	
			A									

Notes:

1. t_{AA} is tested with switch S_1 closed and C_L = 30pF. t_{EAS} is defined as chip enable setup time.
2. For the three-state output, t_{EA} is tested with C_L = 30pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. t_{ER} is tested with C_L = 5pF. HIGH to high impedance tests are made with S_1 open to an output voltage of V_{OH}–0.5V; LOW to high impedance tests are made with S_1 closed to the V_{OL}+0.5V level.

SWITCHING WAVEFORMS



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Note: Level on output while either $\overline{CS}$ is HIGH is determined externally.

For programming information, please see "Guide to the Programming of AMD's Generic Bipolar PROMs", page 2-1.

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