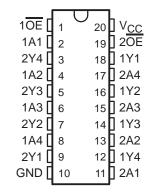- **State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low-Static Power Dissipation**
- **Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C**
- **Latch-Up Performance Exceeds 500 mA Per JEDEC Standard JESD-17**
- **Bus-Hold Data Inputs Eliminate the Need for External Pullup Resistors**
- **Supports Live Insertion**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, Ceramic Chip Carriers (FK), and Ceramic DIPs (J)**
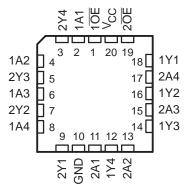
SN54LVT244A . . . J PACKAGE
SN74LVT244A . . . DB, DW, OR PW PACKAGE
(TOP VIEW)

1$\overline{OE}$	1		20	V_{CC}
1A1	2		19	2$\overline{OE}$
2Y4	3		18	1Y1
1A2	4		17	2A4
2Y3	5		16	1Y2
1A3	6		15	2A3
2Y2	7		14	1Y3
1A4	8		13	2A2
2Y1	9		12	1Y4
GND	10		11	2A1

SN54LVT244A . . . FK PACKAGE
(TOP VIEW)

Top pins: 2Y4, 1A1, 1$\overline{OE}$, V_{CC}, 2$\overline{OE}$ (positions 3, 2, 1, 20, 19)

1A2	4		18	1Y1
2Y3	5		17	2A4
1A3	6		16	1Y2
2Y2	7		15	2A3
1A4	8		14	1Y3

Bottom pins: 2Y1, GND, 2A1, 1Y4, 2A2 (positions 9, 10, 11, 12, 13)

description

These octal buffers and line drivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

The ′LVT244A is organized as two 4-bit line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74LVT244A is available in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN54LVT244A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LVT244A is characterized for operation from −40°C to 85°C.
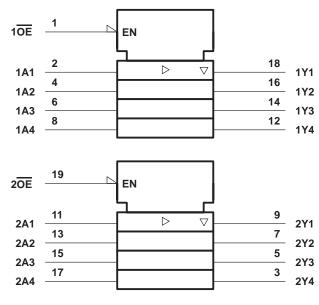
FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

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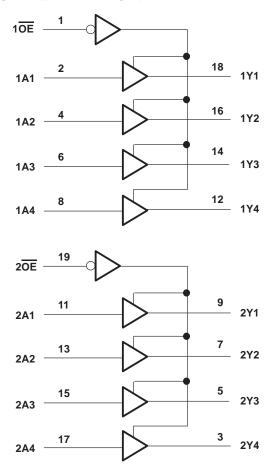## logic symbol†

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} .... −0.5 V to 4.6 V
Input voltage range, V_I (see Note 1) .... −0.5 V to 7 V
Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) .... −0.5 V to 7 V
Current into any output in the low state, I_O: SN54LVT244A .... 96 mA
                                                SN74LVT244A .... 128 mA
Current into any output in the high state, I_O (see Note 2): SN54LVT244A .... 48 mA
                                                            SN74LVT244A .... 64 mA
Input clamp current, I_{IK} (V_I < 0) .... −50 mA
Output clamp current, I_{OK} (V_O < 0) .... −50 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 3): DB package .... 0.6 W
                                                                     DW package .... 1.6 W
                                                                     PW package .... 0.7 W
Storage temperature range .... −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
        2. This current will only flow when the output is in the high state and V_O > V_{CC}.
        3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note.

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recommended operating conditions (see Note 4)

			SN54LVT244A		SN74LVT244A		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4: Unused or floating control inputs must be held high or low.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			SN54LVT244A MIN	SN54LVT244A TYP†	SN54LVT244A MAX	SN74LVT244A MIN	SN74LVT244A TYP†	SN74LVT244A MAX	UNIT
V_{IK}	V_{CC} = 2.7 V,	I_I = −18 mA				−1.2			−1.2	V
V_{OH}	V_{CC} = MIN to MAX‡,	I_{OH} = −100 µA		V_{CC}−0.2			V_{CC}−0.2			V
	V_{CC} = 2.7 V,	I_{OH} = − 8 mA		2.4			2.4			
	V_{CC} = 3 V,	I_{OH} = − 24 mA		2						
	V_{CC} = 3 V,	I_{OH} = −32 mA					2			
V_{OL}	V_{CC} = 2.7 V,	I_{OL} = 100 µA				0.2			0.2	V
	V_{CC} = 2.7 V,	I_{OL} = 24 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 16 mA				0.4			0.4	
	V_{CC} = 3 V,	I_{OL} = 32 mA				0.5			0.5	
	V_{CC} = 3 V,	I_{OL} = 48 mA				0.55				
	V_{CC} = 3 V,	I_{OL} = 64 mA							0.55	
I_I	V_{CC} = 0 or MAX‡,	V_I = 5.5 V				10			10	µA
	V_{CC} = 3.6 V,	V_I = V_{CC} or GND	Control pins			±1			±1	
	V_{CC} = 3.6 V,	V_I = V_{CC}	Data pins			1			1	
	V_{CC} = 3.6 V,	V_I = 0				−5			−5	
I_{off}	V_{CC} = 0,	V_I or V_O = 0 to 4.5 V							±100	µA
$I_{I(hold)}$	V_{CC} = 3 V	V_I = 0.8 V	A inputs	75			75			µA
		V_I = 2 V		−75			−75			
I_{OZH}	V_{CC} = 3.6 V,	V_O = 3 V				5			5	µA
I_{OZL}	V_{CC} = 3.6 V,	V_O = 0.5 V				−5			−5	µA
I_{CC}	V_{CC} = 3.6 V, V_I = V_{CC} or GND	I_O = 0,	Outputs high		0.12	0.5		0.12	0.19	mA
			Outputs low		8.6	14		8.6	12	
			Outputs disabled		0.12	0.5		0.12	0.19	
ΔI_{CC}§	V_{CC} = 3 V to 3.6 V, One input at V_{CC} − 0.6 V, Other inputs at V_{CC} or GND					0.3			0.2	mA
C_i	V_I = 3 V or 0				4			4		pF
C_o	V_O = 3 V or 0				8			8		pF

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

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switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Note 5)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVT244A V_{CC} = 3.3 V $\pm$ 0.3 V		SN54LVT244A V_{CC} = 2.7 V		SN74LVT244A V_{CC} = 3.3 V $\pm$ 0.3 V			SN74LVT244A V_{CC} = 2.7 V		UNIT
			MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
t_{PLH}	A	Y	0.5	4.7		5.2	1	2.5	4.1		5	ns
t_{PHL}			0.5	4.4		5.4	1	2.5	4.1		5.2	
t_{PZH}	$\overline{OE}$	Y	0.8	5.4		6.5	1	2.7	5.2		6.3	ns
t_{PZL}			0.8	5.4		7.6	1.1	3.1	5.2		6.7	
t_{PHZ}	$\overline{OE}$	Y	1.5	6.2		6.9	1.9	3.9	5.6		6.3	ns
t_{PLZ}			1.2	5.5		6	1.8	3.2	5.1		5.6	

NOTE 5: Load circuit and voltage waveforms are shown in Section 1.

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