LMR23630 SIMPLE SWITCHER® 36-V, 3-A Synchronous Step-Down Converter

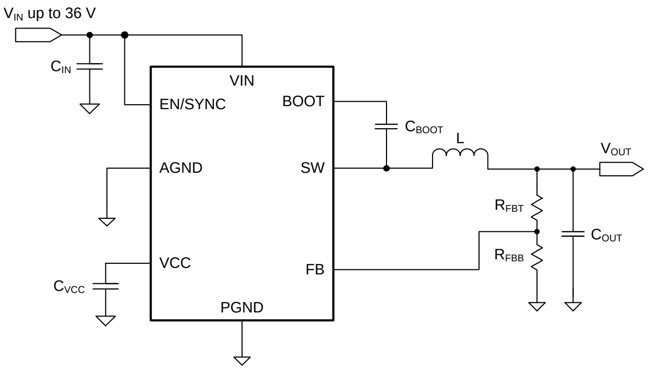
1 Features

- 4-V to 36-V Input Range
- 3-A Continuous Output Current
- Integrated Synchronous Rectification
- Current-Mode Control
- Minimum Switch On-Time: 60 ns
- Internal Compensation for Ease of Use
- 400-kHz Switching Frequency and Adjustable Frequency Options
- PFM and Forced PWM Mode Options
- Frequency Synchronization to External Clock
- 75-µA Quiescent Current at No Load for PFM Option
- Soft Start into a Prebiased Load
- High Duty-Cycle Operation Supported
- Precision Enable Input
- Output Short-Circuit Protection With Hiccup Mode
- Thermal Protection
- 8-Pin HSOIC with PowerPAD™ Package
- 12-Pin WSON Wettable Flanks Package with PowerPAD™
- Create a Custom Design Using the LMR23625 With the WEBENCH® Power Designer

2 Applications

- Factory and Building Automation Systems: PLC CPU, HVAC Control, Elevator Control
- GSM, GPRS Modules for Fleet Management, Smart Grids, and Security
- General Purpose Wide VIN Regulation

Simplified Schematic



3 Description

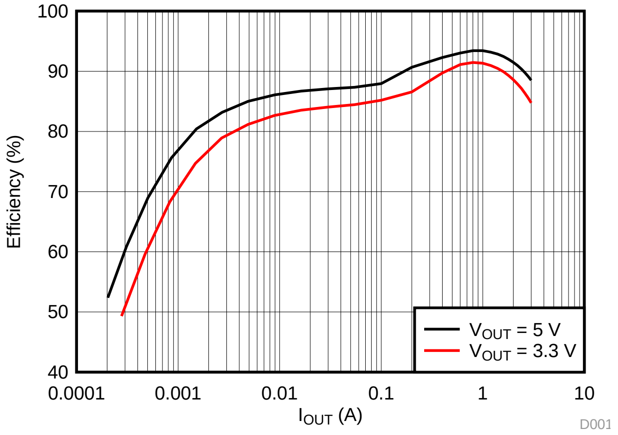
The LMR23630 SIMPLE SWITCHER® is an easy-to-use 36 V, 3 A synchronous step-down regulator. With a wide input range from 4 V to 36 V, it is suitable for various industrial applications for power conditioning from unregulated sources. Peak-current-mode control is employed to achieve simple control-loop compensation and cycle-by-cycle current limiting. A quiescent current of 75 µA makes the device suitable for battery-powered systems. An ultra-low 2 µA shutdown current can further prolong battery life. Internal loop compensation means that the user is free from the tedious task of loop compensation design. This also minimizes the external components. The device has an option for constant frequency FPWM mode to achieve small output-voltage ripple at light load. An extended family (HSOIC) is available in 1-A (LMR23610) and 2.5-A (LMR23625) load-current options in a pin-to-pin compatible package allowing simple, optimum PCB layout. A precision enable input allows simplification of regulator control and system power sequencing. Protection features include cycle-by-cycle current limit, hiccup-mode short-circuit protection, and thermal shutdown due to excessive power dissipation.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMR23630	HSOIC (8)	4.89 mm × 3.90 mm
	WSON (12)	3.00 mm × 3.00 mm

[1] For detail part numbers for all available different options, see the orderable addendum at the end of the data sheet.

Efficiency vs Load
V_{IN} = 12 V, PFM Option



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4 Revision History

Changes from Revision C (June 2017) to Revision D — Page

- Changed HSOIC and WSON Input Range to 4 V to 36 V from 4.5 V for HSOIC and 4 V for WSON 1
- Changed Programmable Logic Controller Power Supply to Factory and Building Automation System... in Applications 1
- Deleted Multi-Function Printers and Industrial Power Supplies and reworded *Applications* 1
- Changed HVAC Systems from Applications to General Purpose Wide VIN Regulation 1
- Added "2.2-µF, 16-V" for VCC pin bypass capacitor 5
- Change the Max Recommend Operating Condition for Iout to be 3-A from 2.5-A 6
- Consolidating all the common EC table characteristic between HSOIC and WSON, for example Operation Input Voltage, VIN_UVLO, I_{EN} and Mnimum turn-on time 7
- Changed Typical Value for VIN_UVLO Rising threshold typical from 3.6-V to 3.7-V and minimum Falling threshold from 3-V to 2.9-V 7
- Changed the operating from "4.5-V" ... to "4-V" in Device Functional Modes 20
- Changed from V_{OUT} = 7 V to 36 V to V_{IN} = 7 V to 36 V on Figure 31 26

Changes from Revision B (April 2017) to Revision C — Page

- Deleted Deleted "Automotive Battery Regulation" and reworded *Applications* 1
- Added WSON Package and Options 1
- Added *Device Comparison Table* 4
- Change EN Abs Max to EN/SYNC Abs Max 6
- Updating ESD Ratings to include HSOIC and WSON 6
- Corrected Equation 17 denominator from "(V_{OUT} x V_{OS})" to "(V_{OUT} + V_{OS})" 24
- clarified equations Equation 23 and Equation 24 29

Changes from Revision A (July 2016) to Revision B **Page**

- Changed spec from 6.0 to 6.2 for max under Current Limit 8
- Changed spec from 4.2 to 4.6 for max under Current Limit 8

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2015) to Revision A **Page**

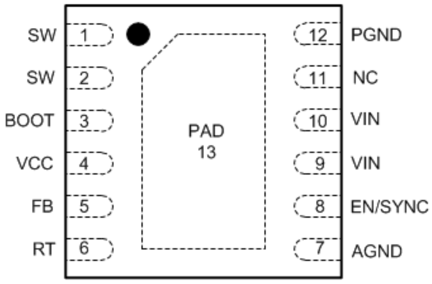
- Changed from Product Preview to Production Data with all the remaining sections added. 1

5 Device Comparison Table

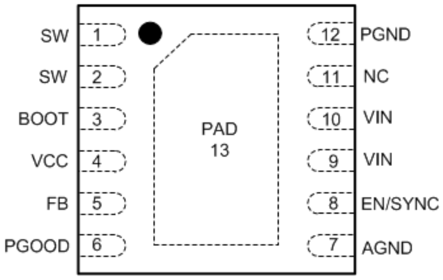
PACKAGE	PART NUMBER	FIXED 400 kHz	ADJUSTABLE FREQUENCY RESISTOR	POWER GOOD	FPWM
HSOIC (8)	LMR23630ADDA	yes	no	no	no
	LMR23630AFDDA	yes	no	no	yes
WSON (12) (Pin 6 is RT)	LMR23630DRR	no	yes	no	no
	LMR23630FDRR	no	yes	no	yes
WSON (12) (Pin 6 is PGOOD)	LMR23630APDRR	yes	no	yes	no

6 Pin Configuration and Functions

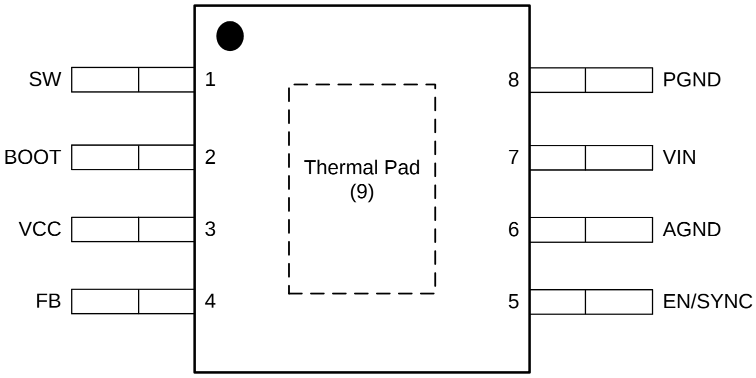
DRR Package
12-Pin WSON With RT and Thermal Pad
Top View



DRR Package
12-Pin WSON With PGOOD and Thermal Pad
Top View



DDA Package
8-Pin HSOIC
Top View



Pin Functions

PIN				I/O [1]	DESCRIPTION
HSO IC	WSON With RT	WSON With PGOOD	NAME		
1	1, 2	1, 2	SW	P	Switching output of the regulator. Internally connected to both power MOSFETs. Connect to power inductor.
2	3	3	BOOT	P	Boot-strap capacitor connection for high-side driver. Connect a high quality 100nF or 470nF capacitor from BOOT to SW.
3	4	4	VCC	P	Internal bias supply output for bypassing. Connect 2.2-µF, 16-V bypass capacitor from this pin to AGND. Do not connect external loading to this pin. Never short this pin to ground during operation.
4	5	5	FB	A	Feedback input to regulator, connect the midpoint of feedback resistor divider to this pin.
N/A	6	N/A	RT	A	Connect a resistor RT from this pin to AGND to program switching frequency. Leave floating for 400-kHz default switching frequency.
N/A	N/A	6	PGOOD	A	Open drain output for power-good flag. Use a 10-kΩ to 100-kΩ pullup resistor to logic rail or other DC voltage no higher than 12 V.
5	8	8	EN/SYNC	A	Enable input to regulator. High = On, Low = Off. Can be connected to VIN. Do not float. Adjust the input undervoltage lockout with two resistors. The internal oscillator can be synchronized to an external clock by coupling a positive pulse into this pin through a small coupling capacitor. See *Enable/Sync* for details.
6	7	7	AGND	G	Analog ground pin. Ground reference for internal references and logic. Connect to system ground.
7	9, 10	9, 10	VIN	P	Input supply voltage.
8	12	12	PGND	G	Power ground pin, connected internally to the low side power FET. Connect to system ground, PAD, AGND, ground pins of C_{IN} and C_{OUT}. Path to C_{IN} must be as short as possible.
9	13	13	PAD	G	Low impedance connection to AGND. Connect to PGND on PCB. Major heat dissipation path of the die. Must be used for heat sinking to ground plane on PCB.
N/A	11	11	NC	N/A	Not for use. Leave this pin floating.

(1) A = Analog, P = Power, G = Ground.

7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted) (1)

PARAMETER		MIN	MAX	UNIT
Input voltages	VIN to PGND	–0.3	42	V
	EN/SYNC to AGND	–5.5	V_{IN}+ 0.3	
	FB to AGND	–0.3	4.5	
	RT to AGND	–0.3	4.5	
	PGOOD to AGND	–0.3	15	
	AGND to PGND	–0.3	0.3	
Output voltages	SW to PGND	–1	V_{IN} + 0.3	V
	SW to PGND less than 10 ns transients	–5	42	
	BOOT to SW	–0.3	5.5	
	VCC to AGND	–0.3	4.5 (2)	
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In shutdown mode, the VCC to AGND maximum value is 5.25 V.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) for HSOIC (1)	±2000	V
		Human-body model (HBM) for WSON with RT and PGOOD (1)	±2500	
		Charged-device model (CDM) for HSOIC and WSON RT (2)	±1000	
		Charged-device model (CDM) for WSON PGOOD (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	4	36	V
	EN/SYNC	–5	36	
	FB	–0.3	1.2	
	PGOOD	–0.3	12	
Input current	PGOOD pin current	0	1	mA
Output voltage	V_{OUT}	1	28	V
Output current	I_{OUT}	0	3	A
Temperature	Operating junction temperature, T_J	–40	125	°C

(1) Operating Ratings indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see *Electrical Characteristics*.

7.4 Thermal Information

THERMAL METRIC (1) (2)		DDA (8 PINS)	DRR (12 PINS)	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.0	41.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.9	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.4	16.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.8	39.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.6	3.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	16.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) Determine power rating at a specific ambient temperature T_A with a maximum junction temperature (T_J) of 125°C (see *Recommended Operating Conditions*).

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VIN PIN)						
V_{IN}	Operation input voltage		4		36	V
VIN_UVLO	Undervoltage lockout thresholds	Rising threshold	3.3	3.7	3.9	V
		Falling threshold	2.9	3.3	3.5	
I_{SHDN}	Shutdown supply current	V_{EN} = 0 V, V_{IN} = 12 V, T_J = –40°C to 125°C		2	4	µA
I_Q	Operating quiescent current (non-switching)	V_{IN} =12 V, V_{FB} = 1.1 V, T_J = –40°C to 125°C, PFM mode		75		µA
ENABLE (EN/SYNC PIN)						
V_{EN_H}	Enable rising threshold voltage		1.4	1.55	1.7	V
V_{EN_HYS}	Enable hysteresis voltage			0.4		V
V_{WAKE}	Wake-up threshold		0.4			V
I_{EN}	Input leakage current at EN pin	V_{IN} = 4 V to 36 V, V_{EN}= 2 V		10	100	nA nA
		V_{IN} = 4 V to 36 V, V_{EN}= 36 V			1	µA µA
VOLTAGE REFERENCE (FB PIN)						
V_{REF}	Reference voltage	V_{IN} = 4.0 V to 36 V, T_J = 25 °C	0.985	1	1.015	V
		V_{IN} = 4.0 V to 36 V, T_J = –40°C to 125°C	0.98	1	1.02	V
I_{LKG_FB}	Input leakage current at FB pin	V_{FB}= 1 V		10		nA

Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25 °C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD (PGOOD PIN)						
V_{PG_OV}	Power-good flag overvoltage tripping threshold	% of reference voltage	104%	107%	110%	
V_{PG_UV}	Power-good flag undervoltage tripping threshold	% of reference voltage	92%	94%	96.5%	
V_{PG_HYS}	Power-good flag recovery hysteresis	% of reference voltage		1.5%		
$V_{IN\_PG\_MIN}$	Minimum V_{IN} for valid PGOOD output	50 μA pullup to PGOOD pin, V_{EN} = 0 V, T_J = 25°C			1.5	V
V_{PG_LOW}	PGOOD low level output voltage	50 μA pullup to PGOOD pin, V_{IN} = 1.5 V, V_{EN} = 0 V			0.4	V
		0.5 mA pullup to PGOOD pin, V_{IN} = 13.5 V, V_{EN} = 0 V			0.4	V
INTERNAL LDO (VCC PIN)						
V_{CC}	Internal LDO output voltage			4.1		V
VCC_UVLO	VCC undervoltage lockout thresholds	Rising threshold	2.8	3.2	3.6	V
		Falling threshold	2.4	2.8	3.2	
CURRENT LIMIT						
I_{HS_LIMIT}	Peak inductor current limit	HSOIC package	3.8	5	6.2	A
		WSON package	4	5.5	6.6	
I_{LS_LIMIT}	Valley inductor current limit	HSOIC package	2.9	3.6	4.6	A
		WSON package	2.9	3.6	4.2	
I_{L_ZC}	Zero cross current limit	HSOIC and WSON package		–0.04		A
I_{L_NEG}	Negative current limit (FPWM option)	SOIC and WSON package	–2.7	–2	–1.3	A
INTEGRATED MOSFETS						
$R_{DS\_ON\_HS}$	High-side MOSFET ON-resistance	SOIC package, V_{IN} = 12 V, I_{OUT} = 1 A		185		mΩ
		WSON package, V_{IN} = 12 V, I_{OUT} = 1 A		160		
$R_{DS\_ON\_LS}$	Low-side MOSFET ON-resistance	SOIC package, V_{IN} = 12 V, I_{OUT} = 1 A		105		mΩ
		WSON package, V_{IN} = 12 V, I_{OUT} = 1 A		95		
THERMAL SHUTDOWN						
T_{SHDN}	Thermal shutdown threshold		162	170	178	°C
T_{HYS}	Hysteresis			15		°C

7.6 Timing Requirements

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
HICCUP MODE						
N_{OC} (1)	Number of cycles that LS current limit is tripped to enter hiccup mode			64		Cycles
T_{OC}	Hiccup retry delay time	SOIC package		5		ms
		WSON package		10		
SOFT START						
T_{SS}	Internal soft-start time	SOIC package, the time of internal reference to increase from 0 V to 1 V		2		ms
		WSON package, the time of internal reference to increase from 0 V to 1 V		6		ms
POWER GOOD						
T_{PGOOD_RISE}	Power-good flag rising transition deglitch delay			150		µs
T_{PGOOD_FALL}	Power-good flag falling transition deglitch delay			18		µs

(1) Ensured by design.

7.7 Switching Characteristics

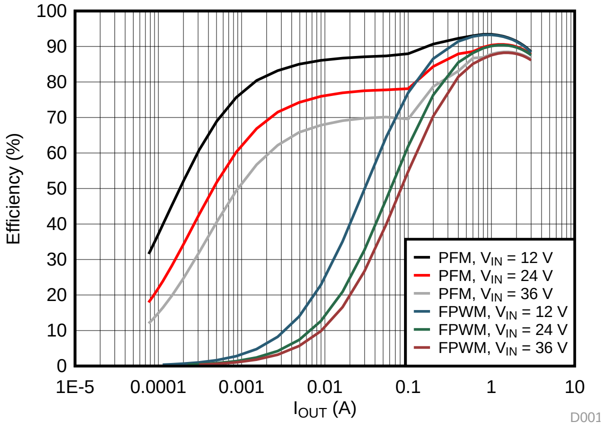
Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
SW (SW PIN)						
T_{ON_MIN}	Minimum turnon time	WSON package		60	90	ns
T_{OFF_MIN} (1)	Minimum turnoff time			100		ns
OSCILLATOR (RT and EN/SYNC PIN)						
$f_{SW\_DEFAULT}$	Oscillator default frequency	Fixed frequency version or RT pin open circuit	340	400	460	kHz
f_{ADJ}	Minimum adjustable frequency	R_T = 198 kΩ with 1% accuracy	150	200	250	kHz
	Maximum adjustable frequency	R_T = 17.8 kΩ with 1% accuracy	1750	2150	2425	kHz
f_{SYNC}	SYNC frequency range		200		2200	kHz
V_{SYNC}	Amplitude of SYNC clock AC signal (measured at SYNC pin)		2.8		5.5	V
T_{SYNC_MIN}	Minimum sync clock ON-time and OFF-time			100		ns

(1) Specified by design.

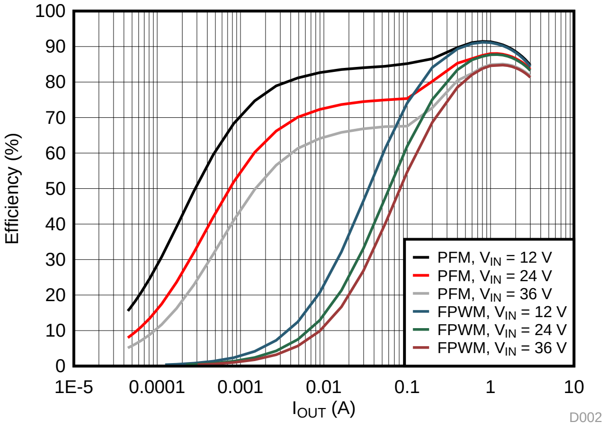
7.8 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT} = 150 µF, T_A = 25°C.



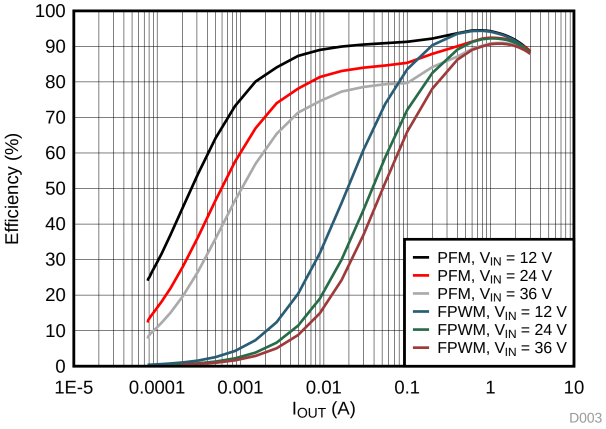
f_{SW} = 400 kHz V_{OUT} = 5 V

Figure 1. Efficiency vs Load Current



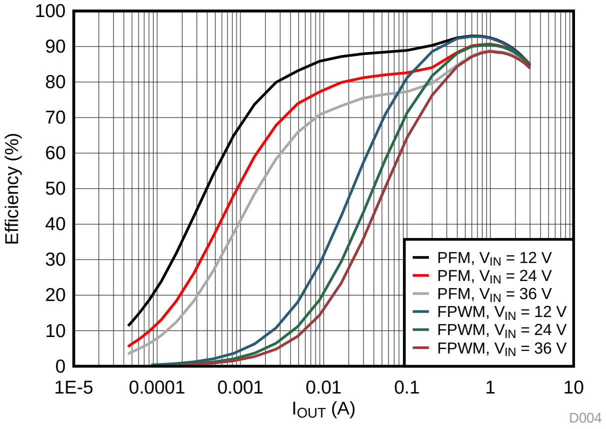
f_{SW} = 400 kHz V_{OUT} = 3.3 V

Figure 2. Efficiency vs Load Current



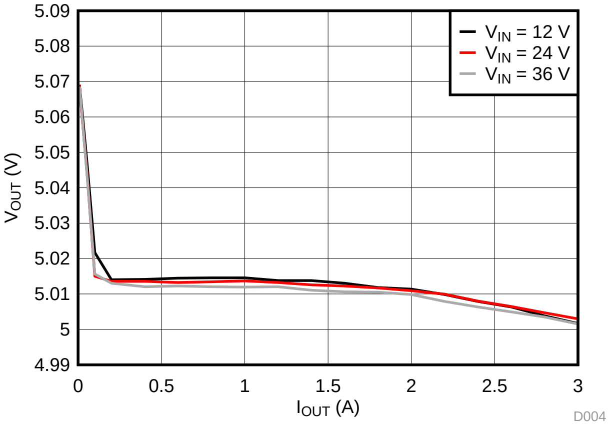
f_{SW} = 200 kHz
(Sync)
V_{OUT} = 5 V

Figure 3. Efficiency vs Load Current



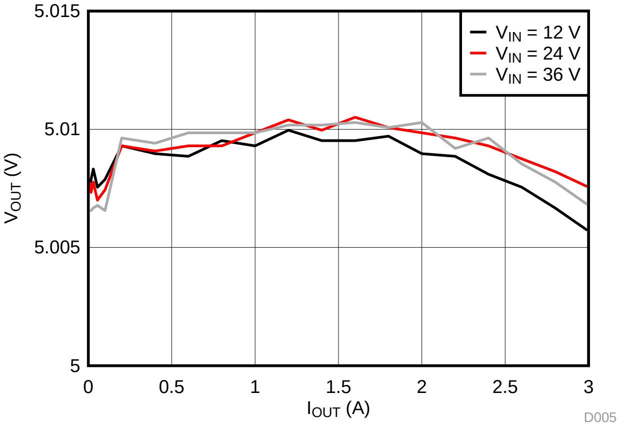
f_{SW} = 200 kHz
(Sync)
V_{OUT} = 3.3 V

Figure 4. Efficiency vs Load Current



PFM version V_{OUT} = 5 V

Figure 5. Load Regulation

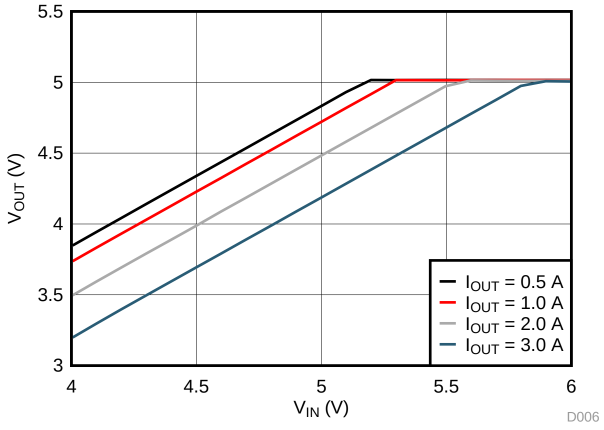


FPWM Version V_{OUT} = 5 V

Figure 6. Load Regulation

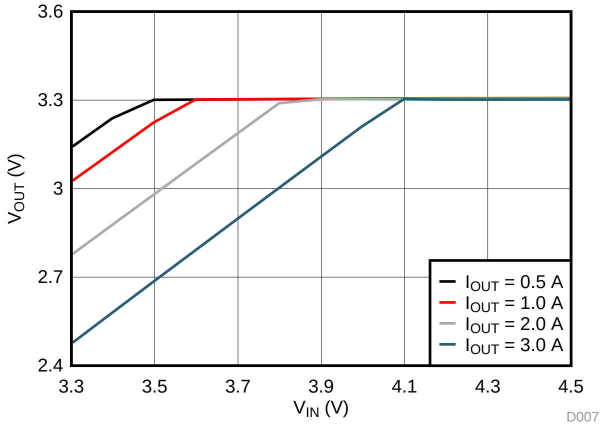
Typical Characteristics (continued)

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT} = 150 µF, T_A = 25°C.



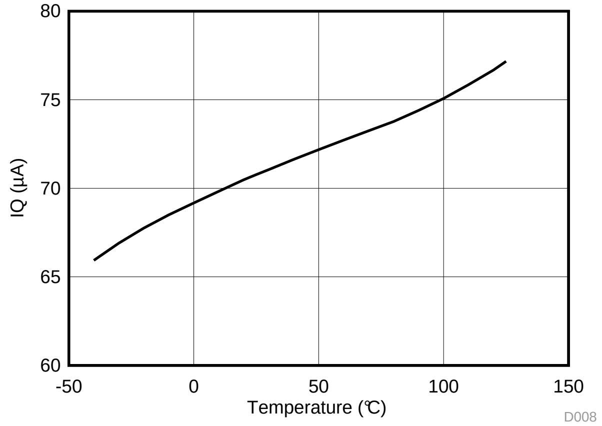
V_{OUT} = 5 V

Figure 7. Dropout Curve



V_{OUT} = 3.3 V

Figure 8. Dropout Curve



V_{IN} = 12 V V_{FB} = 1.1 V

Figure 9. I_Q vs Junction Temperature

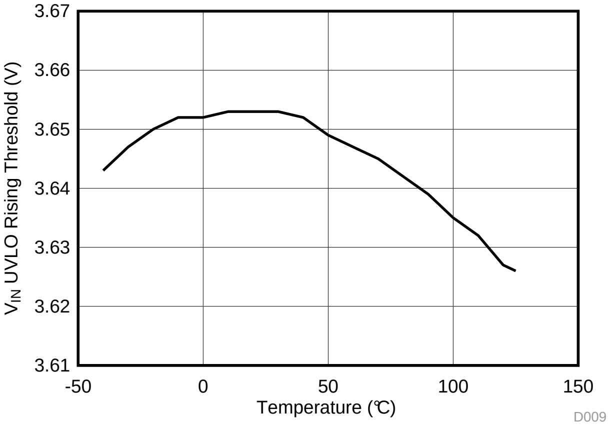


Figure 10. VIN UVLO Rising Threshold vs Junction Temperature

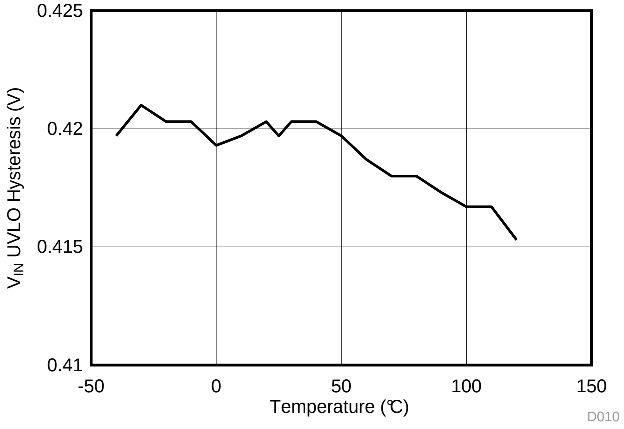
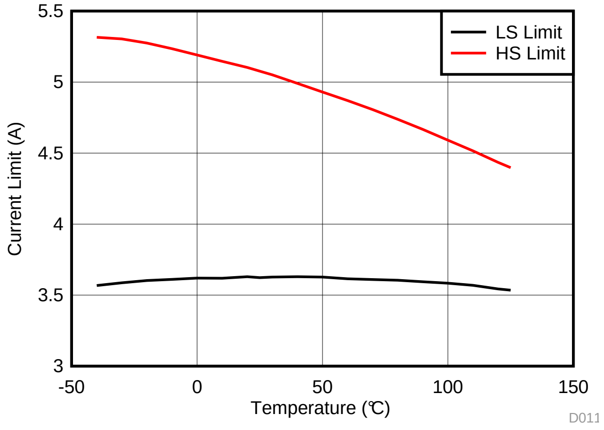


Figure 11. VIN UVLO Hysteresis vs Junction Temperature



V_{IN} = 12 V

Figure 12. HS and LS Current Limit vs Junction Temperature

8 Detailed Description

8.1 Overview

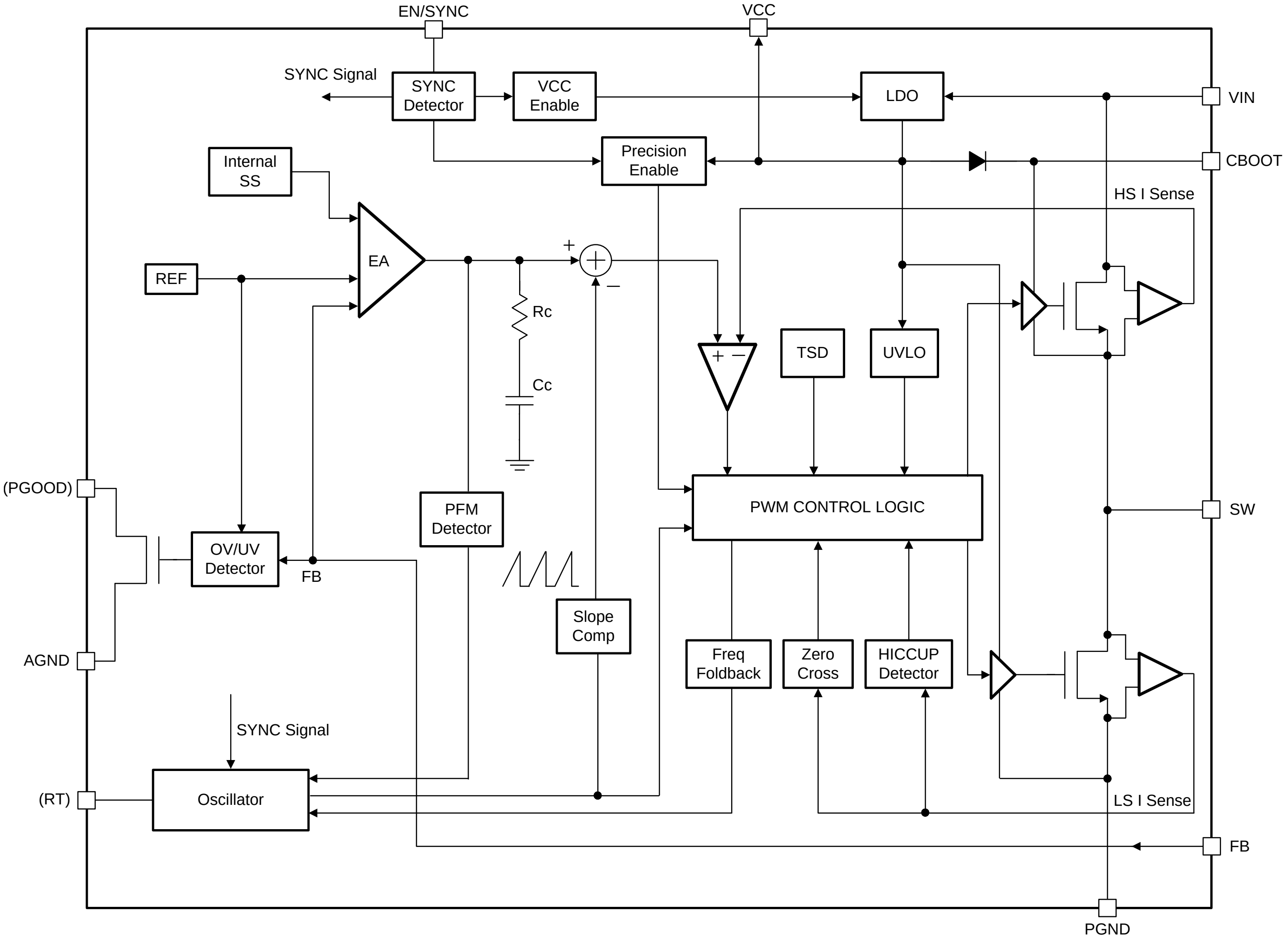
The LMR23630 SIMPLE SWITCHER® regulator is an easy-to-use synchronous step-down DC-DC converter operating from 4-V to 36-V supply voltage. The device delivers up to 3-A DC load current with good thermal performance in a small solution size. For both the HSOIC and WSON packages, an extended family is available in multiple current options from 1 A to 3 A in pin-to-pin compatible packages.

The LMR23630 employs constant frequency peak-current-mode control. The device enters PFM mode at light load to achieve high efficiency. A user-selectable FPWM version is provided to achieve low output voltage ripple, tight output voltage regulation, and constant switching frequency. The switching frequency is 400 kHz for the fixed-frequency version. For the version which has RT pin, the switching frequency is adjustable from 200 kHz to 2.2 MHz. The device is internally compensated, which reduces design time and requires few external components. The LMR23630 is capable of synchronization to an external clock within the range of 200 kHz to 2.2 MHz.

Additional features such as precision enable, power-good flag, and internal soft-start provide a flexible and easy-to-use solution for a wide range of applications. Protection features include thermal shutdown, VIN and VCC undervoltage lockout, cycle-by-cycle current limit, and hiccup-mode short-circuit protection.

The family requires very few external components and has a pinout designed for simple, optimum PCB layout.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency Peak Current Mode Control

The following operating description of the LMR23630 refers to the *Functional Block Diagram* and to the waveforms in Figure 13. The LMR23630 is a step-down synchronous buck regulator with integrated high-side (HS) and low-side (LS) switches (synchronous rectifier). The LMR23630 supplies a regulated output voltage by turning on the HS and LS NMOS switches with controlled duty cycle. During high-side switch ON-time, the SW pin voltage swings up to approximately V_{IN}, and the inductor current i_L increase with linear slope (V_{IN} – V_{OUT}) / L. When the HS switch is turned off by the control logic, the LS switch is turned on after an anti-shoot-through dead time. Inductor current discharges through the LS switch with a slope of $-V_{OUT}$ / L. The control parameter of a buck converter is defined as duty cycle D = t_{ON} / T_{SW}, where t_{ON} is the high-side switch ON-time and T_{SW} is the switching period. The regulator control loop maintains a constant output voltage by adjusting the duty cycle D. In an ideal buck converter, where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage: D = V_{OUT} / V_{IN}.

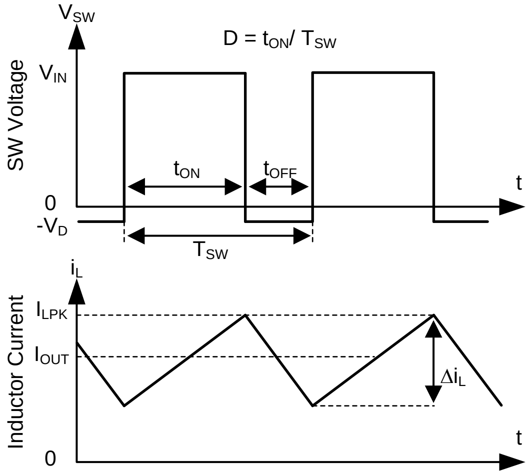


Figure 13. SW Node and Inductor Current Waveforms in Continuous Conduction Mode (CCM)

The LMR23630 employs fixed-frequency peak-current-mode control. A voltage feedback loop is used to get accurate DC voltage regulation by adjusting the peak current command based on voltage offset. The peak inductor current is sensed from the high-side switch and compared to the peak current threshold to control the ON-time of the high-side switch. The voltage feedback loop is internally compensated, which allows for fewer external components, makes it easy to design, and provides stable operation with almost any combination of output capacitors. The regulator operates with fixed switching frequency at normal load condition. At light load condition, the LMR23630 operates in PFM mode to maintain high efficiency (PFM option) or in FPWM mode for low output-voltage ripple, tight output-voltage regulation, and constant switching frequency (FPWM option).

8.3.2 Adjustable Frequency

The switching frequency can be programmed for the adjustable-switching-frequency version of LMR23630 by the impedance R_T from the RT pin to ground. The frequency is inversely proportional to the R_T resistance. The RT pin can be left floating and the LMR23630 operates at 400-kHz default switching frequency. The RT pin is not designed to be shorted to ground. For a desired frequency, typical R_T resistance can be found by Equation 1. Table 1 gives typical R_T values for a given f_{SW}.

$$R_T(k\Omega) = 40200 / f_{SW}(kHz) - 0.6 \quad (1)$$

Feature Description (continued)

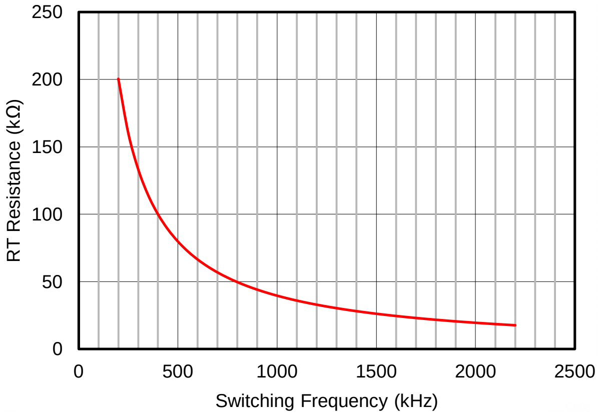


Figure 14. RT vs Frequency Curve

Table 1. Typical Frequency Setting RT Resistance

f_{SW} (kHz)	R_T (kΩ)
200	200
350	115
500	78.7
750	53.6
1000	39.2
1500	26.1
2000	19.6
2200	17.8

8.3.3 Adjustable Output Voltage

A precision 1-V reference voltage is used to maintain a tightly regulated output voltage over the entire operating temperature range. The output voltage is set by a resistor divider from output voltage to the FB pin. TI recommends using 1% tolerance resistors with a low temperature coefficient for the FB divider. Select the lowside resistor RFBB for the desired divider current and use Equation 2 to calculate high-side R_{FBT}. R_{FBT} in the range from 10 kΩ to 100 kΩ is recommended for most applications. A lower RFBT value can be used if static loading is desired to reduce VOUT offset in PFM operation. Lower RFBT will reduce efficiency at very light load. Less static current goes through a larger RFBT and might be more desirable when light load efficiency is critical. However, RFBT larger than 1 MΩ is not recommended because it makes the feedback path more susceptible to noise. Larger RFBT value requires more carefully designed feedback path on the PCB. The tolerance and temperature variation of the resistor dividers affect the output voltage regulation.

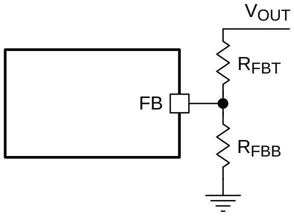


Figure 15. Output Voltage Setting

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \tag{2}$$

8.3.4 Enable/Sync

The voltage on the EN/SYNC pin controls the ON or OFF operation of LMR23630. A voltage less than 1 V (typical) shuts down the device while a voltage higher than 1.6 V (typical) is required to start the regulator. The EN/SYNC pin is an input and cannot be left open or floating. The simplest way to enable the operation of the LMR23630 is to connect the EN to V_{IN}. This allows self-start-up of the LMR23630 when V_{IN} is within the operation range.

Many applications can benefit from the employment of an enable divider R_{ENT} and R_{ENB} (Figure 16) to establish a precision system UVLO level for the converter. System UVLO can be used for supplies operating from utility power as well as battery power. It can be used for sequencing, ensuring reliable operation, or supply protection, such as a battery discharge level. An external logic signal can also be used to drive EN input for system sequencing and protection.

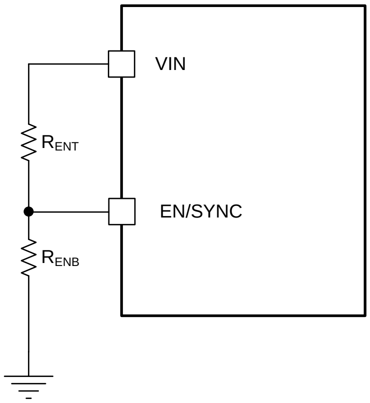


Figure 16. System UVLO by Enable Divider

The EN pin also can be used to synchronize the internal oscillator to an external clock. The internal oscillator can be synchronized by AC-coupling a positive edge into the EN pin. The AC-coupled peak-to-peak voltage at the EN pin must exceed the SYNC amplitude threshold of 2.8 V (typical) to trip the internal synchronization pulse detector, and the minimum SYNC clock ON-time and OFF-time must be longer than 100 ns (typical). A 3.3-V or a higher amplitude pulse signal coupled through a 1-nF capacitor C_{SYNC} is a good starting point. Keeping R_{ENT} // R_{ENB} (R_{ENT} parallel with R_{ENB}) in the 100 kΩ range is a good choice. R_{ENT} is required for this synchronization circuit, but R_{ENB} can be left unmounted if system UVLO is not needed. LMR23630 switching action can be synchronized to an external clock from 200 kHz to 2.2 MHz. Figure 18 and Figure 19 show the device synchronized to an external system clock.

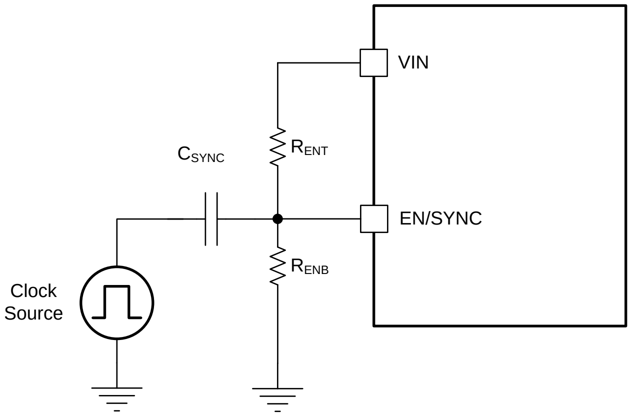


Figure 17. Synchronize to External Clock

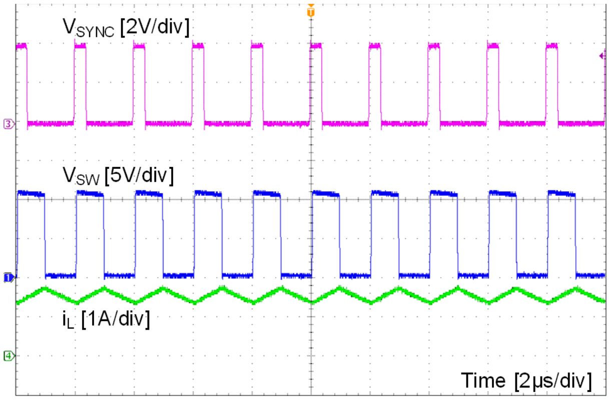


Figure 18. Synchronizing in PWM Mode

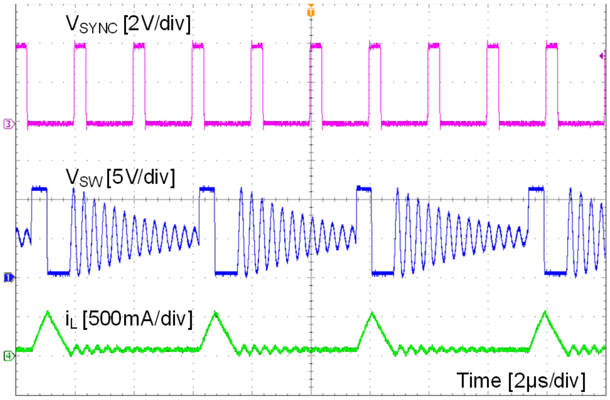


Figure 19. Synchronizing in PFM Mode

8.3.5 VCC, UVLO

The LMR23630 integrates an internal LDO to generate V_{CC} for control circuitry and MOSFET drivers. The nominal voltage for V_{CC} is 4.1 V. The VCC pin is the output of an LDO and must be properly bypassed. Place a high-quality ceramic capacitor with a value of 2.2 µF to 10 µF, 16 V or higher rated voltage as close as possible to VCC and grounded to the exposed PAD and ground pins. The VCC output pin must not be loaded, or shorted to ground during operation. Shorting VCC to ground during operation may cause damage to the LMR23630.

VCC undervoltage lockout (UVLO) prevents the LMR23630 from operating until the V_{CC} voltage exceeds 3.3 V (typical). The VCC UVLO threshold has 400 mV (typical) of hysteresis to prevent undesired shutdown due to temporary V_{IN} drops.

8.3.6 Minimum ON-time, Minimum OFF-time and Frequency Foldback at Dropout Conditions

Minimum ON-time, T_{ON_MIN}, is the smallest duration of time that the HS switch can be on. T_{ON_MIN} is typically 60 ns in the LMR23630. Minimum OFF-time, T_{OFF_MIN}, is the smallest duration that the HS switch can be off. T_{OFF_MIN} is typically 100 ns in the LMR23630. In CCM operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range given a selected switching frequency.

The minimum duty cycle allowed is:

$$D_{MIN} = T_{ON\_MIN} \times f_{SW} \tag{3}$$

And the maximum duty cycle allowed is:

$$D_{MAX} = 1 - T_{OFF\_MIN} \times f_{SW} \tag{4}$$

Given fixed T_{ON_MIN} and T_{OFF_MIN}, the higher the switching frequency the narrower the range of the allowed duty cycle. In the LMR23630, a frequency foldback scheme is employed to extend the maximum duty cycle when T_{OFF_MIN} is reached. The switching frequency decreases once longer duty cycle is needed under low V_{IN} conditions. Wide range of frequency foldback allows the LMR23630 output voltage stay in regulation with a much lower supply voltage V_{IN}. This leads to a lower effective dropout voltage.

Given an output voltage, the choice of the switching frequency affects the allowed input voltage range, solution size and efficiency. The maximum operation supply voltage can be found by:

$$V_{IN\_MAX} = \frac{V_{OUT}}{\left(f_{SW} \times T_{ON\_MIN}\right)} \tag{5}$$

At lower supply voltage, the switching frequency decreases once T_{OFF_MIN} is tripped. The minimum V_{IN} without frequency foldback can be approximated by:

$$V_{IN\_MIN} = \frac{V_{OUT}}{\left(1 - f_{SW} \times T_{OFF\_MIN}\right)} \tag{6}$$

Taking considerations of power losses in the system with heavy load operation, V_{IN_MAX} is higher than the result calculated in Equation 5. With frequency foldback, V_{IN_MIN} is lowered by decreased f_{SW}.

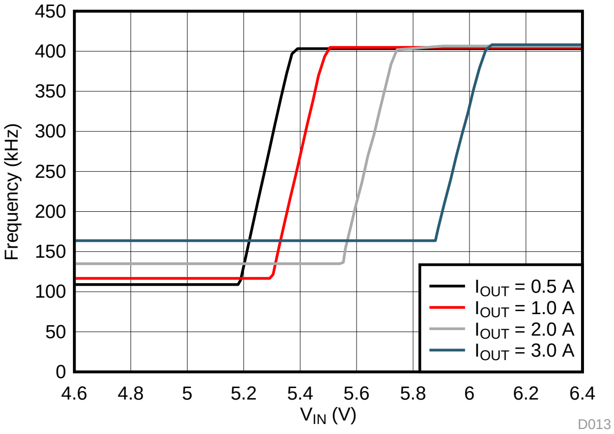


Figure 20. Frequency Foldback at Dropout (V_{OUT} = 5 V, f_{SW} = 400 kHz)

8.3.7 Power Good (PGOOD)

The power-good version of LMR23630 has a built in power-good flag shown on PGOOD pin to indicate whether the output voltage is within its regulation level. The PGOOD signal can be used for start-up sequencing of multiple rails or fault protection. The PGOOD pin is an open-drain output that requires a pullup resistor to an appropriate DC voltage. Voltage detected by the PGOOD pin must never exceed 15 V, and limit the maximum current into this pin to 1 mA. A typical range of pullup resistor value is 10 kΩ to 100 kΩ.

When the FB voltage is within the power-good band, +6% above and –6% below the internal reference voltage V_{REF} typically, the PGOOD switch is turned off, and the PGOOD voltage is as high as the pulled-up voltage. When the FB voltage is outside of the tolerance band, +7% above or –7% below V_{REF} typically, the PGOOD switch is turned on, and the PGOOD pin voltage is pulled low to indicate power bad. A glitch filter prevents false flag operation for short excursions in the output voltage, such as during line and load transients. The values for the various filter and delay times can be found in the *Timing Requirements* table. Power-good operation can best be understood by reference to Figure 21.

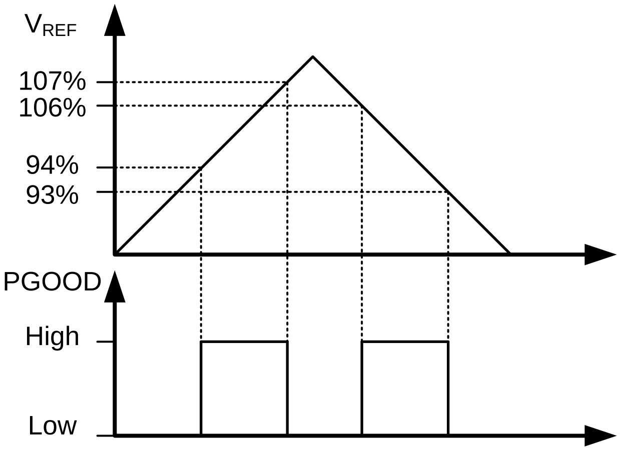


Figure 21. Power-Good Flag

8.3.8 Internal Compensation and C_{FF}

The LMR23630 is internally compensated as shown in *Functional Block Diagram*. The internal compensation is designed so that the loop response is stable over the entire operating frequency and output voltage range. Depending on the output voltage, the compensation loop phase margin can be low with all ceramic capacitors. TI recommends an external feed-forward capacitor C_{FF} be placed in parallel with the top resistor divider R_{FBT} for optimum transient performance.

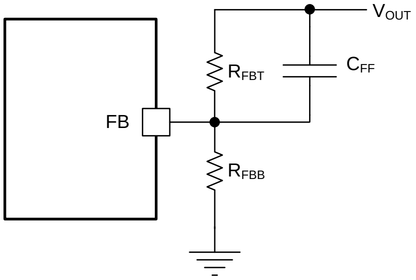


Figure 22. Feed-forward Capacitor for Loop Compensation

The feed-forward capacitor C_{FF} in parallel with R_{FBT} places an additional zero before the crossover frequency of the control loop to boost phase margin. The zero frequency can be found by:

$$f_{Z\_CFF} = \frac{1}{\left(2\pi \times C_{FF} \times R_{FBT}\right)} \tag{7}$$

An additional pole is also introduced with C_{FF} at the frequency of:

$$f_{P\_CFF} = \frac{1}{\left(2\pi \times C_{FF} \times R_{FBT} // R_{FBB}\right)} \tag{8}$$

The zero f_{Z_CFF} adds phase boost at the crossover frequency and improves transient response. The pole $f_{P\text{-}CFF}$ helps maintaining proper gain margin at frequency beyond the crossover. Table 2 lists the combination of C_{OUT}, C_{FF} and R_{FBT} for typical applications, designs with similar C_{OUT} but R_{FBT} other than recommended value, adjust C_{FF} such that (C_{FF} × R_{FBT}) is unchanged and adjust R_{FBB} such that (R_{FBT} / R_{FBB}) is unchanged.

Designs with different combinations of output capacitors need different C_{FF}. Different types of capacitors have different equivalent series resistance (ESR). Ceramic capacitors have the smallest ESR and need the most CFF. Electrolytic capacitors have much larger ESR than ceramic, and the ESR zero frequency location would be low enough to boost the phase up around the crossover frequency. Designs that use mostly electrolytic capacitors at the output may not need any CFF. The location of this ESR zero frequency can be calculated with Equation 9:

$$f_{Z\_ESR} = \frac{1}{\left(2\pi \times C_{OUT} \times ESR\right)} \tag{9}$$

The C_{FF} creates a time constant with R_{FBT} that couples in the attenuate output voltage ripple to the FB node. If the C_{FF} value is too large, it can couple too much ripple to the FB and affect V_{OUT} regulation. Therefore, calculate C_{FF} based on output capacitors used in the system. At cold temperatures, the value of C_{FF} might change based on the tolerance of the chosen component. This may reduce its impedance and ease noise coupling on the FB node. To avoid this, more capacitance can be added to the output or the value of C_{FF} can be reduced.

8.3.9 Bootstrap Voltage (BOOT)

The LMR23630 provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and the low-side switch conducts. The recommended value of the BOOT capacitor is 0.1 µF to 0.47 µF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 16 V or higherfor stable performance over temperature and voltage.

8.3.10 Overcurrent and Short-Circuit Protection

The LMR23630 is protected from over-current conditions by cycle-by-cycle current limit on both the peak and valley of the inductor current. Hiccup mode will be activated if a fault condition persists to prevent over-heating.

High-side MOSFET overcurrent protection is implemented by the nature of the peak-current-mode control. The HS switch current is sensed when the HS is turned on after a set blanking time. The HS switch current is compared to the output of the error amplifier (EA) minus slope compensation every switching cycle. See the *Functional Block Diagram* for more details. The peak current of HS switch is limited by a clamped maximum peak current threshold I_{HS_LIMIT} which is constant. Thus, the peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty cycle range.

The current going through LS MOSFET is also sensed and monitored. When the LS switch turns on, the inductor current begins to ramp down. The LS switch is not turned OFF at the end of a switching cycle if its current is above the LS current limit I_{LS_LIMIT}. The LS switch is kept ON so that inductor current keeps ramping down, until the inductor current ramps below the LS current limit I_{LS_LIMIT}. Then the LS switch is turned OFF, and the HS switch is turned on after a dead time. This is somewhat different than the more typical peak current limit and results in Equation 10 for the maximum load current.

$$I_{OUT\_MAX} = I_{LS\_LIMIT} + \frac{(V_{IN} - V_{OUT})}{2 \times f_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}} \tag{10}$$

If the current of the LS switch is higher than the LS current limit for 64 consecutive cycles, hiccup current protection mode is activated. In hiccup mode, the regulator is shut down and kept off for 5 ms typically before the LMR23630 tries to start again. If overcurrent or short-circuit fault condition still exist, hiccup will repeat until the fault condition is removed. Hiccup mode reduces power dissipation under severe overcurrent conditions, prevents over-heating and potential damage to the device.

For FPWM version, the inductor current is allowed to go negative. If this current exceed I_{L_NEG}, the LS switch is turned off until the next clock cycle. This is used to protect the LS switch from excessive negative current.

8.3.11 Thermal Shutdown

The LMR23630 provides an internal thermal shutdown to protect the device when the junction temperature exceeds 170°C (typical). The device is turned off when thermal shutdown activates. Once the die temperature falls below 155°C (typical), the device reinitiates the power-up sequence controlled by the internal soft-start circuitry.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control for the LMR23630. When V_{EN} is below 1 V (typical), the device is in shutdown mode. The LMR23630 also employs VIN and VCC UVLO protection. If V_{IN} or V_{CC} voltage is below their respective UVLO level, the regulator is turned off.

8.4.2 Active Mode

The LMR23630 is in active mode when V_{EN} is above the precision enable threshold, V_{IN} and V_{CC} are above their respective UVLO level. The simplest way to enable the LMR23630 is to connect the EN pin to VIN pin. This allows self startup when the input voltage is in the operating range 4 V to 36 V. See to *VCC, UVLO and Enable/Sync* for details on setting these operating levels.

In active mode, depending on the load current, the LMR23630 is in one of four modes:

1. Continuous conduction mode (CCM) with fixed switching frequency when load current is above half of the peak-to-peak inductor current ripple (for both PFM and FPWM options).
2. Discontinuous conduction mode (DCM) with fixed switching frequency when load current is lower than half of the peak-to-peak inductor current ripple in CCM operation (only for PFM option).
3. Pulse frequency modulation mode (PFM) when switching frequency is decreased at very light load (only for PFM option).
4. Forced pulse width modulation mode (FPWM) with fixed switching frequency even at light load (only for FPWM option).

8.4.3 CCM Mode

CCM operation is employed in the LMR23630 when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode, and the maximum output current of 3 A can be supplied by the LMR23630.

8.4.4 Light Load Operation (PFM Version)

For PFM version, when the load current is lower than half of the peak-to-peak inductor current in CCM, the LMR23630 operates in DCM, also known as diode emulation mode (DEM). In DCM, the LS switch is turned off when the inductor current drops to I_{L_ZC} (–40 mA typical). Both switching losses and conduction losses are reduced in DCM, compared to forced PWM operation at light load.

At even lighter current loads, PFM is activated to maintain high efficiency operation. When either the minimum HS switch ON-time (t_{ON_MIN}) or the minimum peak inductor current I_{PEAK_MIN} (300 mA typ) is reached, the switching frequency decreases to maintain regulation. In PFM, switching frequency is decreased by the control loop when load current reduces to maintain output voltage regulation. Switching loss is further reduced in PFM operation due to less frequent switching actions. The external clock synchronizing is not valid when the LMR23630 device enters into PFM mode.

8.4.5 Light Load Operation (FPWM Version)

For FPWM version, LMR23630 is locked in PWM mode at full load range. This operation is maintained, even at no-load, by allowing the inductor current to reverse its normal direction. This mode trades off reduced light load efficiency for low output voltage ripple, tight output voltage regulation, and constant switching frequency. In this mode, a negative current limit of I_{L_NEG} is imposed to prevent damage to the regulators low side FET. When in FPWM mode the converter synchronizes to any valid clock signal on the EN/SYNC input.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The LMR23630 is a step-down DC-to-DC regulator. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3 A. The following design procedure can be used to select components for the LMR23630. Alternately, the WEBENCH® software may be used to generate complete designs. When generating a design, the WEBENCH® software utilizes iterative design procedure and accesses comprehensive databases of components. See www.ti.com for more details.

9.2 Typical Applications

The LMR23630 only requires a few external components to convert from a wide voltage-range supply to a fixed output voltage. Figure 23 shows a basic schematic.

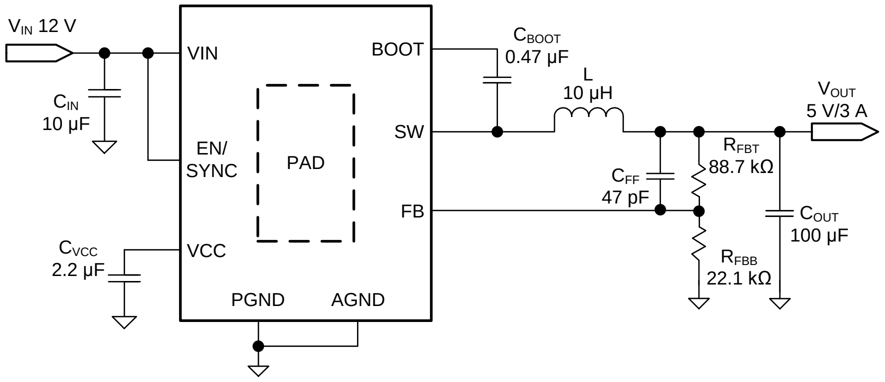


Figure 23. LM23630 Application Circuit

The external components must fulfill the needs of the application, but also the stability criteria of the device control loop. Table 2 can be used to simplify the output filter component selection.

Table 2. L, C_{OUT}, and C_{FF} Typical Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH) (1)	C_{OUT} (µF) (2)	C_{FF} (pF)	R_{FBT} (kΩ) (3) (4)
200	3.3	15	300	150	51
	5	18	200	100	88.7
	12	33	100	See (5)	243
	24	33	47	See (5)	510
400	3.3	6.8	150	75	51
	5	10	100	47	88.7
	12	15	68	See (5)	243
	24	15	47	See (5)	510

(1) Inductance value is calculated based on V_{IN} = 36 V.
(2) All the C_{OUT} values are after derating. Add more when using ceramic capacitors.
(3) R_{FBT} = 0 Ω for V_{OUT} = 1 V. R_{FBB} = 22.1 kΩ for all other V_{OUT} setting.
(4) For designs with R_{FBT} other than recommended value, please adjust C_{FF} such that (C_{FF} × R_{FBT}) is unchanged and adjust R_{FBB} such that (R_{FBT} / R_{FBB}) is unchanged.
(5) High ESR C_{OUT} gives enough phase boost and C_{FF} not needed.

Typical Applications (continued)

Table 2. L, C_{OUT}, and C_{FF} Typical Values (continued)

f_{SW} (kHz)	V_{OUT} (V)	L (µH) (1)	C_{OUT} (µF) (2)	C_{FF} (pF)	R_{FBT} (kΩ) (3)(4)
1000	3.3	3.3	68	39	51
	5	4.7	47	25	88.7
2200	3.3	2.2	47	33	51
	5	2.2	33	18	88.7

9.2.1 Design Requirements

Detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Example Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage, V_{IN}	12 V typical, range from 8 V to 28 V
Output voltage, V_{OUT}	5 V
Maximum output current I_{O_MAX}	3 A
Transient response 0.2 A to 2.5 A	5%
Output voltage ripple	50 mV
Input voltage ripple	400 mV
Switching frequency f_{SW}	400 kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR23625 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Output Voltage Setpoint

The output voltage of LMR23630 is externally adjustable using a resistor divider network. The divider network is comprised of top feedback resistor R_{FBT} and bottom feedback resistor R_{FBB}. Equation 11 is used to determine the output voltage:

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (11)$$

Choose the value of R_{FBB} to be 22.1 kΩ. With the desired output voltage set to 5 V and the V_{REF} = 1 V, the R_{FBB} value can then be calculated using Equation 11. The formula yields to a value 88.7 kΩ.

9.2.2.3 Switching Frequency

The default switching frequency of the LMR23630 is 400 kHz. For other switching frequency, the device must be synchronized to an external clock, see *Enable/Sync* for more details.

9.2.2.4 Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the rated current. The inductance is based on the desired peak-to-peak ripple current Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance L_{MIN}. Use Equation 13 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current of the device. A reasonable value of K_{IND} should be 20% to 40%. During an instantaneous short or overcurrent operation event, the RMS and peak inductor current can be high. The inductor current rating should be higher than the current limit of the device.

$$\Delta i_L = \frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT}\right)}{V_{IN\_MAX} \times L \times f_{SW}} \tag{12}$$

$$L_{MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times f_{SW}} \tag{13}$$

In general, it is preferable to choose lower inductance in switching power supplies, because it usually corresponds to faster transient response, smaller DCR, and reduced size for more compact designs. However, inductance that is too low can generate an inductor current ripple that is too high so that overcurrent protection at the full load could be falsely triggered. It also generates more conduction loss and inductor core loss. Larger inductor current ripple also implies larger output voltage ripple with same output capacitors. With peak current mode control, TI does not recommend having an inductor current ripple that is too small. A larger peak-current ripple improves the comparator signal-to-noise ratio.

For this design example, choose K_{IND} = 0.4, the minimum inductor value is calculated to be 8.56 µH. Choose the nearest standard 8.2 µH ferrite inductor with a capability of 4-A RMS current and 6-A saturation current.

9.2.2.5 Output Capacitor Selection

Choose the output capacitor(s), C_{OUT}, with care because it directly affects the steady-state output-voltage ripple, loop stability, and the voltage over/undershoot during load-current transients.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the equivalent series resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \tag{14}$$

The other is caused by the inductor current ripple charging and discharging the output capacitors:

$$\Delta V_{OUT\_C} = \frac{\Delta i_L}{\left(8 \times f_{SW} \times C_{OUT}\right)} = \frac{K_{IND} \times I_{OUT}}{\left(8 \times f_{SW} \times C_{OUT}\right)} \tag{15}$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of two peaks.

Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The control loop of the regulator usually needs four or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for four clock cycles to maintain the output voltage within the specified range. Equation 16 shows the minimum output capacitance needed for specified output undershoot. When a sudden large load decrease happens, the output capacitors absorb energy stored in the inductor. which results in an output voltage overshoot. Equation 17 calculates the minimum capacitance required to keep the voltage overshoot within a specified range.

$$C_{OUT} > \frac{4 \times (I_{OH} - I_{OL})}{f_{SW} \times V_{US}} \quad (16)$$

$$C_{OUT} > \frac{I_{OH}^2 - I_{OL}^2}{(V_{OUT} + V_{OS})^2 - V_{OUT}^2} \times L$$

where

- I_{OL} = Low level output current during load transient
- I_{OH} = High level output current during load transient
- V_{US} = Target output voltage undershoot
- V_{OS} = Target output voltage overshoot (17)

For this design example, the target output ripple is 50 mV. Presuppose $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 50 mV, and chose K_{IND} = 0.4. Equation 14 yields ESR no larger than 41.7 mΩ and Equation 15 yields C_{OUT} no smaller than 7.5 µF. For the target over/undershoot range of this design, $V_{US} = V_{OS} = 5\% \times V_{OUT}$ = 250 mV. The C_{OUT} can be calculated to be no smaller than 108 µF and 28.5 µF by Equation 16 and Equation 17, respectively. Consider of derating, one 47-µF, 16-V and one 100-µF, 10-V ceramic capacitor with 5-mΩ ESR are used in parallel.

9.2.2.6 Feed-Forward Capacitor

The LMR23630 is internally compensated. Depending on the V_{OUT} and frequency f_{SW}, if the output capacitor C_{OUT} is dominated by low-ESR (ceramic types) capacitors, it could result in low phase margin. To improve the phase boost an external feed-forward capacitor C_{FF} can be added in parallel with R_{FBT}. C_{FF} is chosen such that phase margin is boosted at the crossover frequency without C_{FF}. A simple estimation for the crossover frequency (f_X) without C_{FF} is shown in Equation 18, assuming C_{OUT} has very small ESR, and C_{OUT} value is after derating.

$$f_X = \frac{8.32}{V_{OUT} \times C_{OUT}} \quad (18)$$

Equation 19 for C_{FF} was tested:

$$C_{FF} = \frac{1}{4\pi \times f_X \times R_{FBT}} \quad (19)$$

For designs with higher ESR, C_{FF} is not needed when C_{OUT} has very high ESR and C_{FF} calculated from Equation 19 must reduced with medium ESR. Table 2 can be used as a quick starting point.

For the application in this design example, a 47-pF, 50-V, COG capacitor is selected.

9.2.2.7 Input Capacitor Selection

The LMR23630 device requires high-frequency input decoupling capacitor(s) and a bulk input capacitor, depending on the application. The typical recommended value for the high-frequency decoupling capacitor is 4.7 µF to 10 µF. TI recommends a high-quality ceramic capacitor type X5R or X7R with sufficiency voltage rating. To compensate the derating of ceramic capacitors, a voltage rating twice the maximum input voltage is recommended. Additionally, some bulk capacitance can be required, especially if the LMR23630 circuit is not located within approximately 5 cm from the input voltage source. This capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace. For this design, two 4.7-µF, 50-V, X7R ceramic capacitors are used. A 0.1-µF for high-frequency filtering and place it as close as possible to the device pins.

9.2.2.8 Bootstrap Capacitor Selection

Every LMR23630 design requires a bootstrap capacitor (C_{BOOT}). TI recommends a capacitor of 0.47 µF, ated 16 V or higher. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability.

9.2.2.9 VCC Capacitor Selection

The VCC pin is the output of an internal LDO for LMR23630. To insure stability of the device, place a minimum of 2.2-µF, 16V, X7R capacitor from this pin to ground.

9.2.2.10 *Undervoltage Lockout Setpoint*

The system undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. The following equation can be used to determine the V_{IN} UVLO level.

$$V_{IN\_RISING} = V_{ENH} \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{20}$$

The EN rising threshold (V_{ENH}) for LMR23630 is set to be 1.55 V (typical). Choose the value of R_{ENB} to be 287 kΩ to minimize input current from the supply. If the desired V_{IN} UVLO level is at 6 V, then the value of R_{ENT} can be calculated using Equation 21:

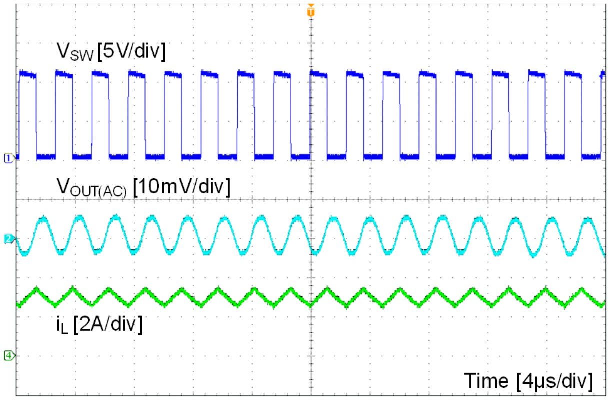
$$R_{ENT} = \left(\frac{V_{IN\_RISING}}{V_{ENH}} - 1 \right) \times R_{ENB} \tag{21}$$

Equation 21 yields a value of 820 kΩ. The resulting falling UVLO threshold, equals 4.4 V, can be calculated by Equation 22, where EN hysteresis (V_{EN_HYS}) is 0.4 V (typical).

$$V_{IN\_FALLING} = \left(V_{ENH} - V_{EN\_HYS} \right) \times \frac{R_{ENT} + R_{ENB}}{R_{ENB}} \tag{22}$$

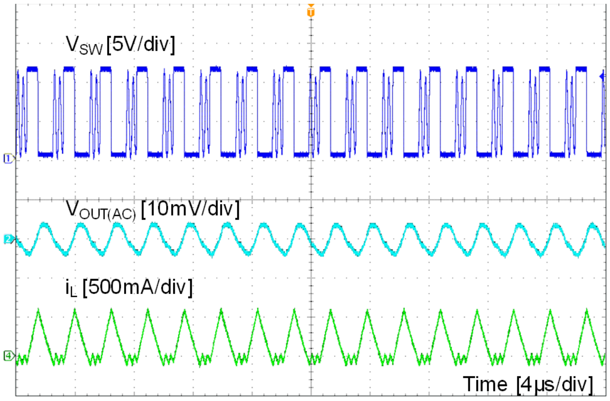
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT} = 150 µF, T_A = 25 °C.



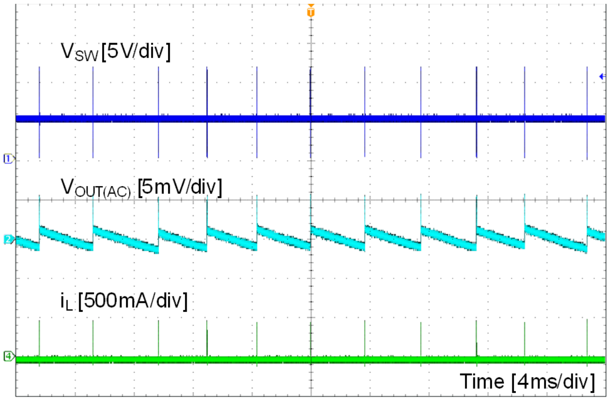
V_{OUT} = 5 V I_{OUT} = 3 A f_{SW} = 400 kHz

Figure 24. CCM Mode



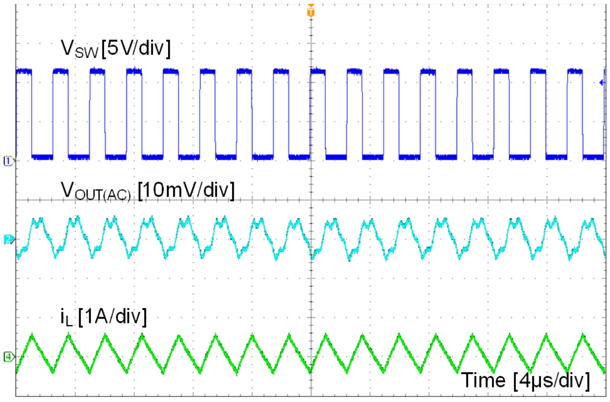
V_{OUT} = 5 V I_{OUT} = 150 mA f_{SW} = 400 kHz

Figure 25. DCM Mode



V_{OUT} = 5 V I_{OUT} = 0 mA f_{SW} = 400 kHz

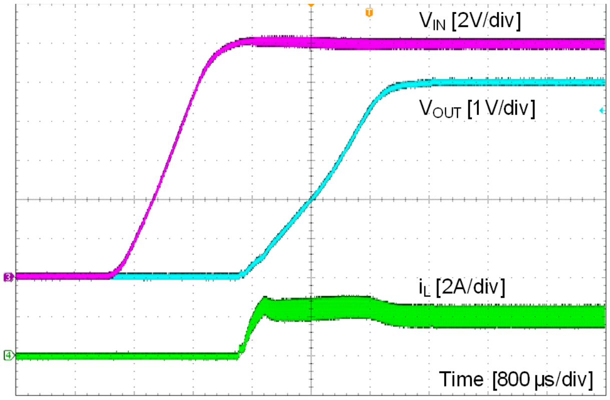
Figure 26. PFM Mode



V_{OUT} = 5 V I_{OUT} = 0 mA f_{SW} = 400 kHz

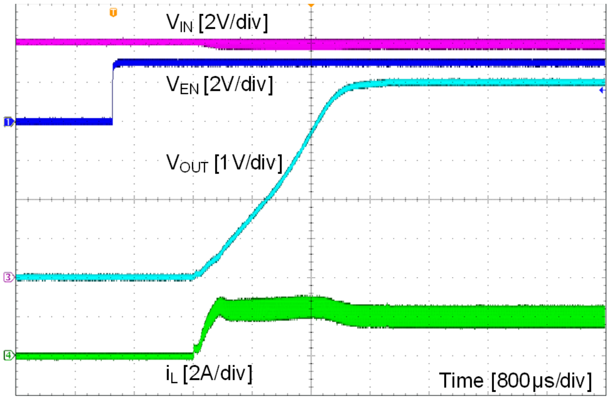
Figure 27. FPWM Mode

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 400 kHz, L = 8.2 µH, C_{OUT} = 150 µF, T_A = 25 °C.



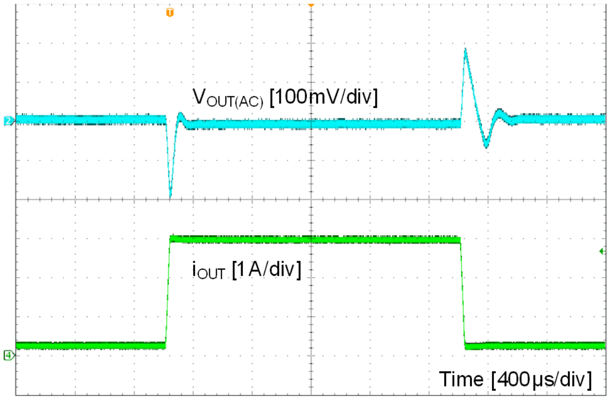
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 2 A

Figure 28. Start Up by V_{IN}



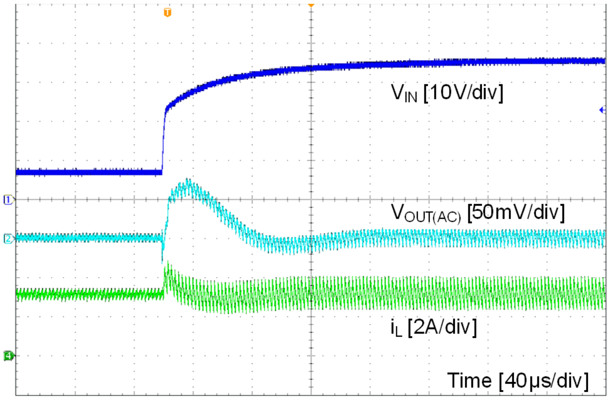
V_{IN} = 12 V V_{OUT} = 5 V I_{OUT} = 2 A

Figure 29. Start Up by EN



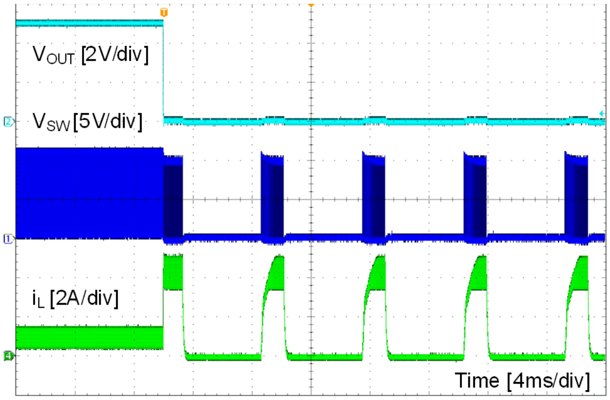
V_{IN} = 12 V I_{OUT} = 0.3 A to 3 A, 100 mA / µs
V_{OUT} = 5 V

Figure 30. Load Transient



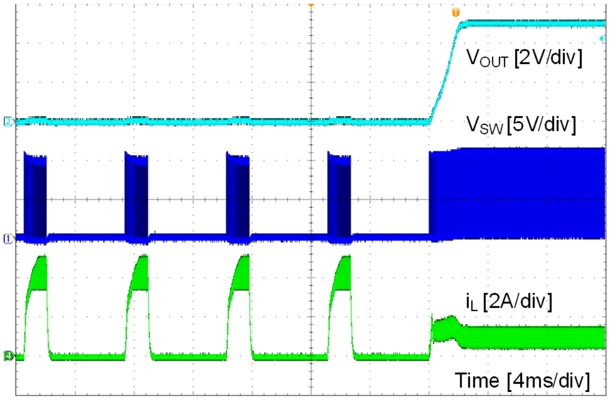
V_{OUT} = 5 V V_{IN} = 7 V to 36 V, 2 V / µs
I_{OUT} = 3 A

Figure 31. Line Transient



V_{OUT} = 5 V I_{OUT} = 1 A to short

Figure 32. Short Protection



V_{OUT} = 5 V I_{OUT} = short to 1 A

Figure 33. Short Recovery

10 Power Supply Recommendations

The LMR23630 is designed to operate from an input voltage supply range between 4.5 V and 36 V for the HSOIC package and 4 V to 36 V for the WSON package. This input supply must be able to withstand the maximum input current and maintain a stable voltage. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LMR23630 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMR23630, additional bulk capacitance may be required in addition to the ceramic input capacitors. The amount of bulk capacitance is not critical, but a 47-μF or 100-μF electrolytic capacitor is a typical choice.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines will help users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The input bypass capacitor C_{IN} must be placed as close as possible to the VIN and PGND pins. Grounding for both the input and output capacitors should consist of localized top side planes that connect to the PGND pin and PAD.
2. Place bypass capacitors for V_{CC} close to the VCC pin and ground the bypass capacitor to device ground.
3. Minimize trace length to the FB pin net. Both feedback resistors, R_{FBT} and R_{FBB} should be located close to the FB pin. Place C_{FF} directly in parallel with R_{FBT}. If V_{OUT} accuracy at the load is important, make sure V_{OUT} sense is made at the load. Route V_{OUT} sense path away from noisy nodes and preferably through a layer on the other side of a shielded layer.
4. Use ground plane in one of the middle layers as noise shielding and heat dissipation path.
5. Have a single point ground connection to the plane. The ground connections for the feedback and enable components should be routed to the ground plane. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior.
6. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. Provide adequate device heat-sinking. Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has multiple copper layers, these thermal vias can also be connected to inner layer heat-spreading ground planes. Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125 °C.

11.2 Layout Example

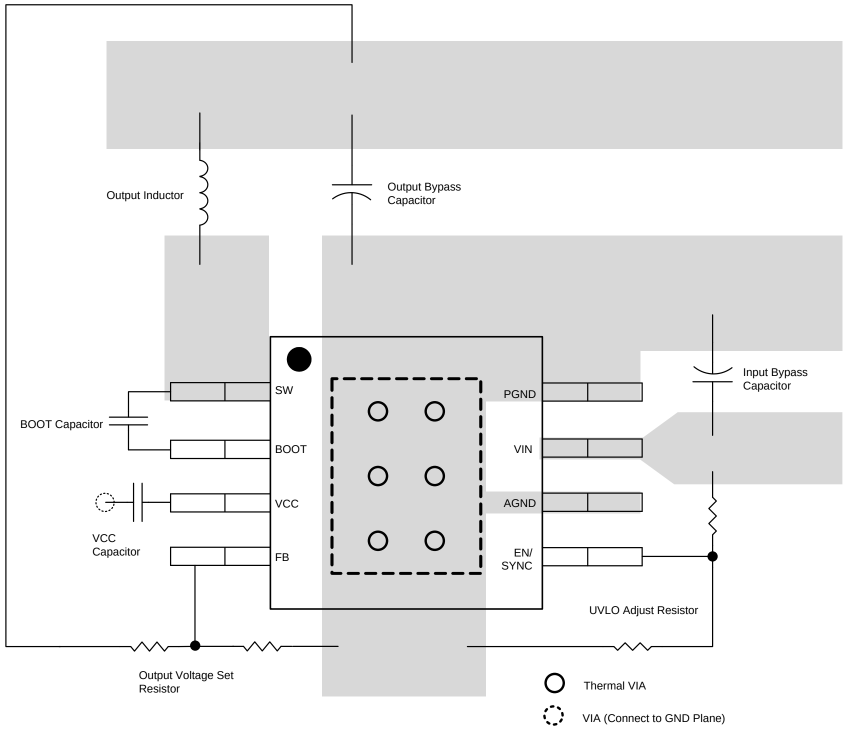


Figure 34. Sample HSOIC Package Layout

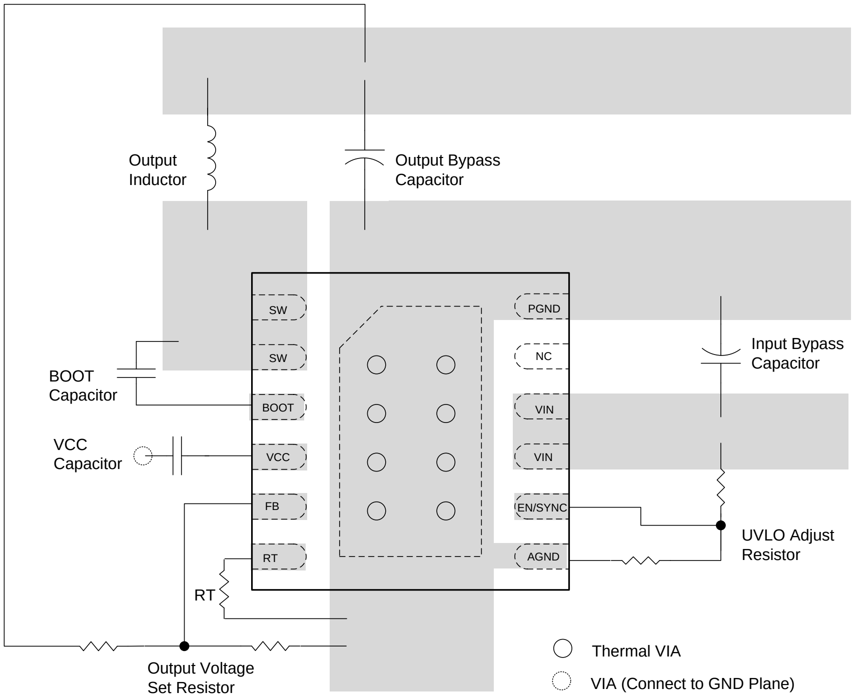


Figure 35. Sample WSON Package Layout

11.3 Compact Layout for EMI Reduction

Radiated EMI is generated by the high di/dt components in pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more EMI is generated. High frequency ceramic bypass capacitors at the input side provide primary path for the high di/dt components of the pulsing current. Placing ceramic bypass capacitor(s) as close as possible to the VIN and PGND pins is the key to EMI reduction.

The SW pin connecting to the inductor must be as short as possible and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) high current conduction path to minimize parasitic resistance. Place the output capacitors close to the V_{OUT} end of the inductor and closely grounded to PGND pin and exposed PAD.

Place the bypass capacitors on VCC as close as possible to the pin and closely grounded to PGND and the exposed PAD.

11.4 Ground Plane and Thermal Considerations

TI recommends using one of the middle layers as a solid ground plane. Ground plane provides shielding for sensitive circuits and traces. It also provides a quiet reference potential for the control circuitry. Connect the AGND and PGND pins to the ground plane using vias right next to the bypass capacitors. PGND pin is connected to the source of the internal LS switch. They must be connected directly to the grounds of the input and output capacitors. The PGND net contains noise at switching frequency and may bounce due to load variations. PGND trace, as well as VIN and SW traces, must be constrained to one side of the ground plane. The other side of the ground plane contains much less noise and should be used for sensitive routes.

TI also recommends providing adequate device heat sinking by utilizing the PAD of the device as the primary thermal path. Use a minimum 4 by 2 array of 12 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias should be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top of, 2 oz / 1 oz / 1 oz / 2 oz. Four-layer boards with enough copper thickness provides low current conduction impedance, proper shielding, and lower thermal resistance.

The thermal characteristics of the LMR23630 are specified using the parameter $R_{\theta JA}$, which characterize the junction temperature of silicon to the ambient temperature in a specific system. Although the value of $R_{\theta JA}$ is dependent on many variables, it still can be used to approximate the operating junction temperature of the device. To obtain an estimate of the device junction temperature, one may use the following relationship:

$$T_J = P_D \times R_{\theta JA} + T_A \quad (23)$$

$$P_D = V_{IN} \times I_{IN} \times (1 - \text{Efficiency}) - 1.1 \times I_{OUT}^2 \times \text{DCR in watt}$$

where

- T_J = junction temperature in °C
- P_D = device power dissipation in watt
- $R_{\theta JA}$ = junction-to-ambient thermal resistance of the device in °C/W
- T_A = ambient temperature in °C
- DCR = inductor DC parasitic resistance in ohm (24)

The maximum operating junction temperature of the LMR23630 is 125°C. $R_{\theta JA}$ is highly related to PCB size and layout, as well as environmental factors such as heat sinking and air flow.

11.5 Feedback Resistors

To reduce noise sensitivity of the output voltage feedback path, it is important to place the resistor divider and C_{FF} close to the FB pin, rather than close to the load. The FB pin is the input to the error amplifier, so it is a high impedance node and very sensitive to noise. Placing the resistor divider and C_{FF} closer to the FB pin reduces the trace length of FB signal and reduces noise coupling. The output node is a low impedance node, so the trace from V_{OUT} to the resistor divider can be long if short path is not available.

If voltage accuracy at the load is important, make sure voltage sense is made at the load. Doing so corrects for voltage drops along the traces and provide the best output accuracy. The voltage sense trace from the load to the feedback resistor divider should be routed away from the SW node path and the inductor to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high value resistors are used to set the output voltage. TI recommends routing the voltage sense trace and place the resistor divider on a different layer than the inductor and SW node path, such that there is a ground plane in between the feedback trace and inductor/SW node polygon. This provides further shielding for the voltage feedback path from EMI noises.

12 Device and Documentation Support

12.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR23625 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
SIMPLE SWITCHER, WEBENCH are registered trademarks of Texas Instruments.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMR23630ADDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	F30A	Samples
LMR23630ADDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	F30A	Samples
LMR23630AFDDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	F30AF	Samples
LMR23630AFDDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	F30AF	Samples
LMR23630APDRRR	ACTIVE	SON	DRR	12	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	3630P	Samples
LMR23630APDRRT	ACTIVE	SON	DRR	12	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	3630P	Samples
LMR23630DRRR	ACTIVE	SON	DRR	12	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	23630	Samples
LMR23630DRRT	ACTIVE	SON	DRR	12	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	23630	Samples
LMR23630FDRRR	ACTIVE	SON	DRR	12	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	3630F	Samples
LMR23630FDRRT	ACTIVE	SON	DRR	12	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	3630F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LMR23630 :

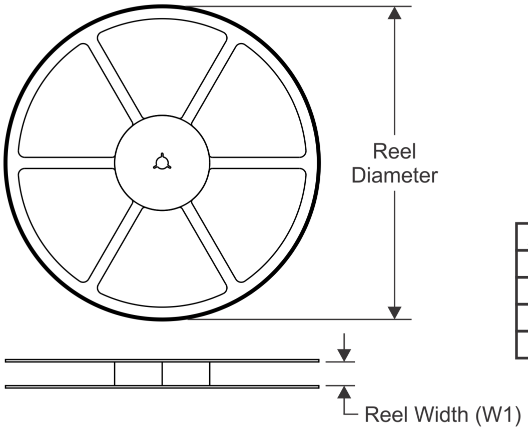
- Automotive: LMR23630-Q1

NOTE: Qualified Version Definitions:

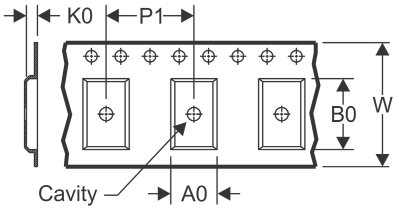
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

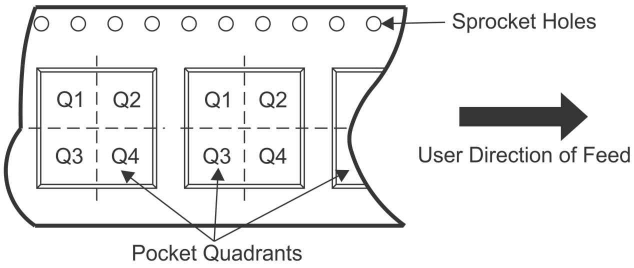


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

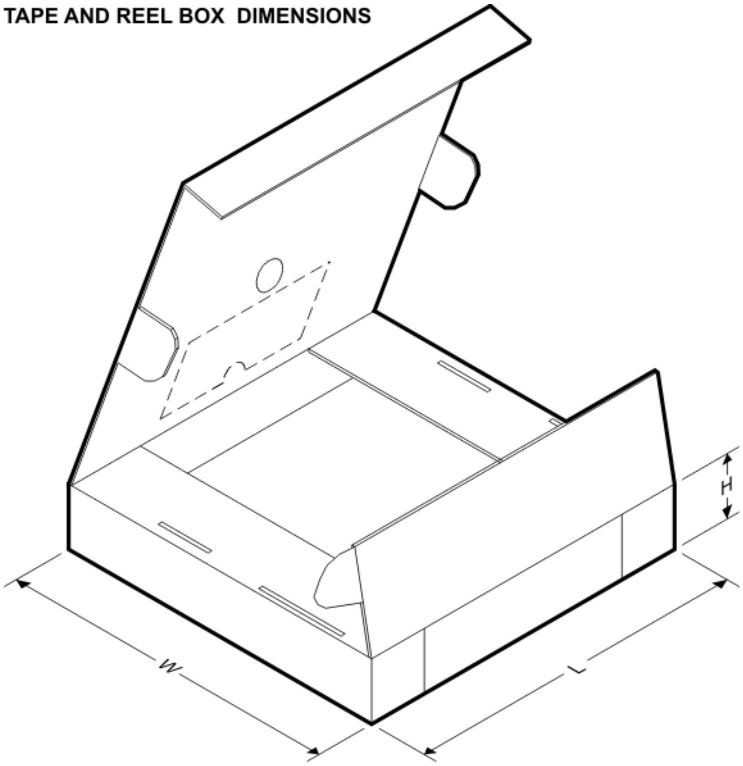
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMR23630ADDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR23630AFDDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1
LMR23630APDRRR	SON	DRR	12	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LMR23630APDRRT	SON	DRR	12	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LMR23630DRRR	SON	DRR	12	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LMR23630DRRT	SON	DRR	12	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LMR23630FDRRR	SON	DRR	12	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2
LMR23630FDRRT	SON	DRR	12	250	180.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

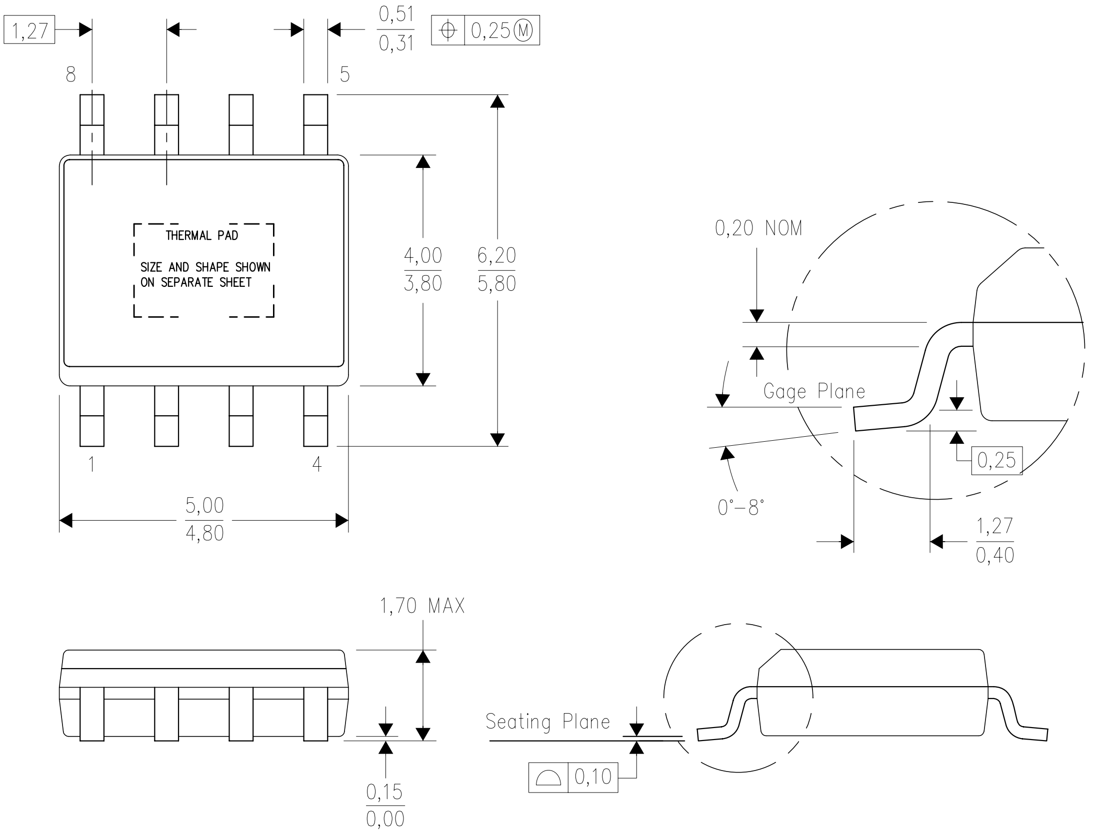
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMR23630ADDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR23630AFDDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0
LMR23630APDRRR	SON	DRR	12	3000	370.0	355.0	55.0
LMR23630APDRRT	SON	DRR	12	250	195.0	200.0	45.0
LMR23630DRRR	SON	DRR	12	3000	370.0	355.0	55.0
LMR23630DRRT	SON	DRR	12	250	195.0	200.0	45.0
LMR23630FDRRR	SON	DRR	12	3000	370.0	355.0	55.0
LMR23630FDRRT	SON	DRR	12	250	195.0	200.0	45.0

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

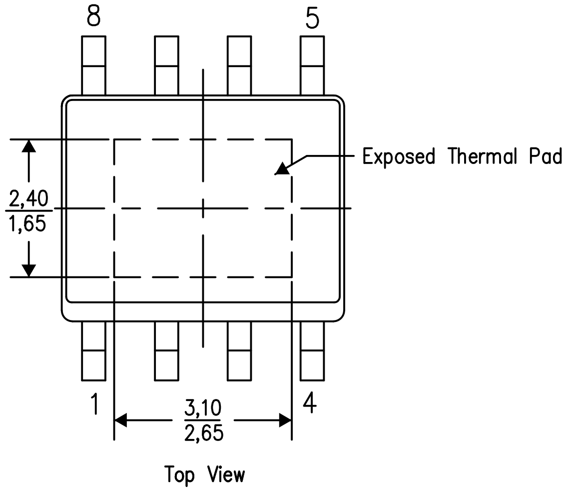
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

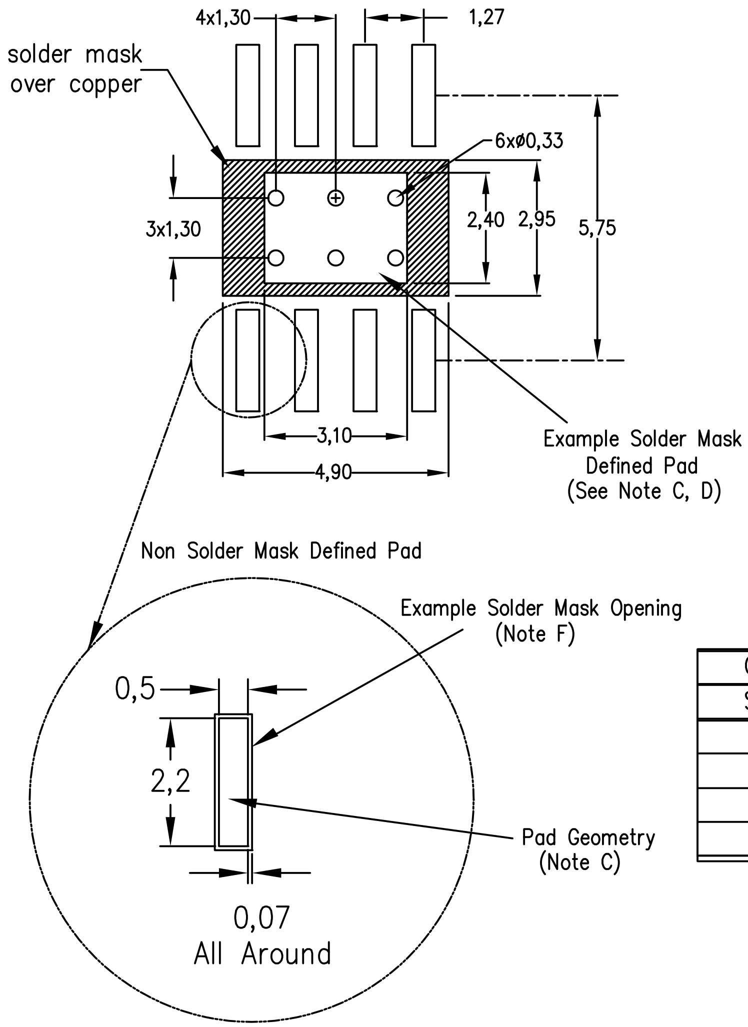
4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

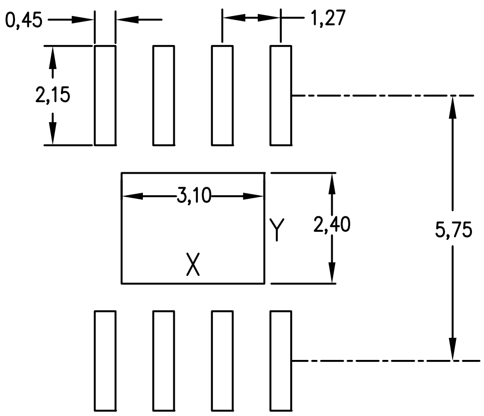
PowerPAD is a trademark of Texas Instruments

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

Example Board Layout
Via pattern and copper pad size
may vary depending on layout constraints



0,127mm Thick Stencil Design Example
Reference table below for other
solder stencil thicknesses
(Note E)



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

4208951-6/D 04/12

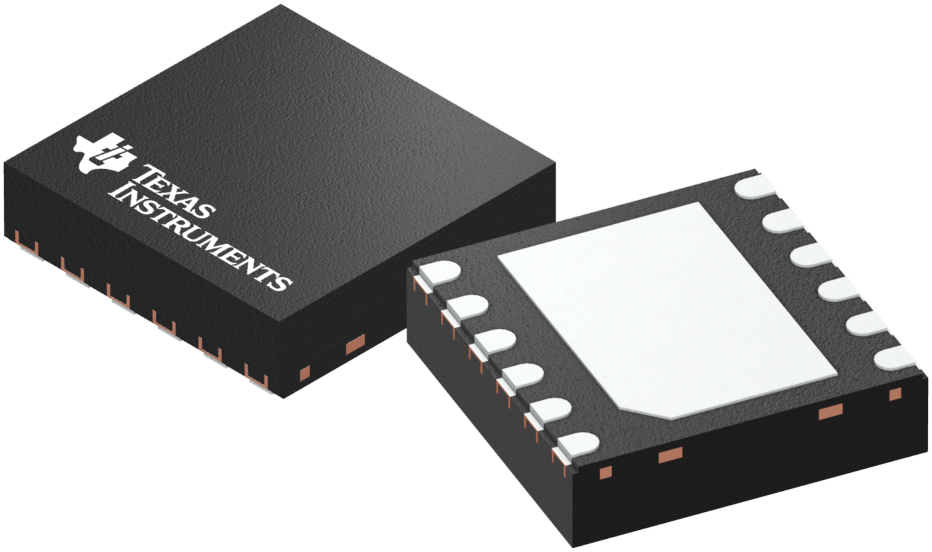
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

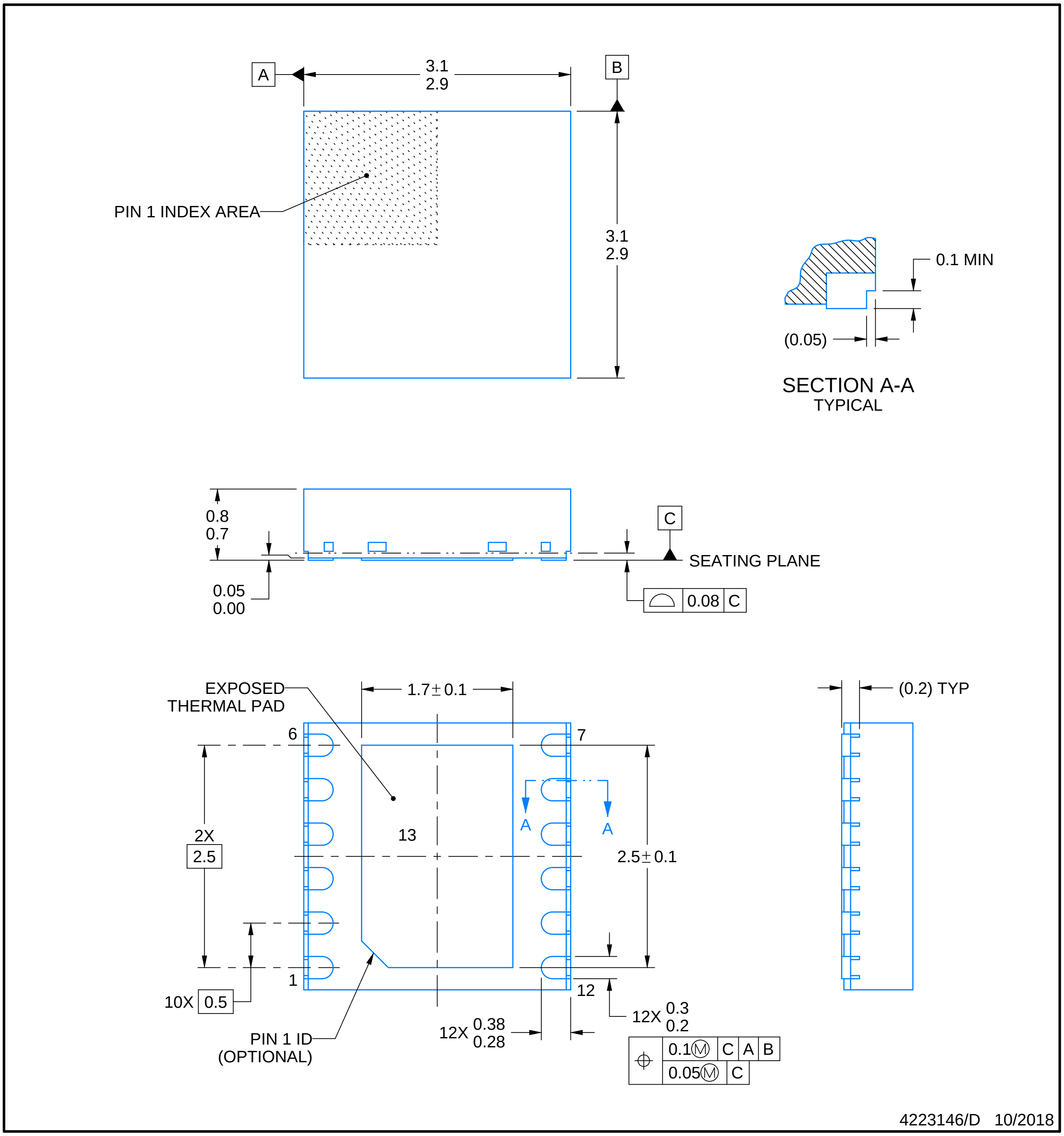
DRR 12

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

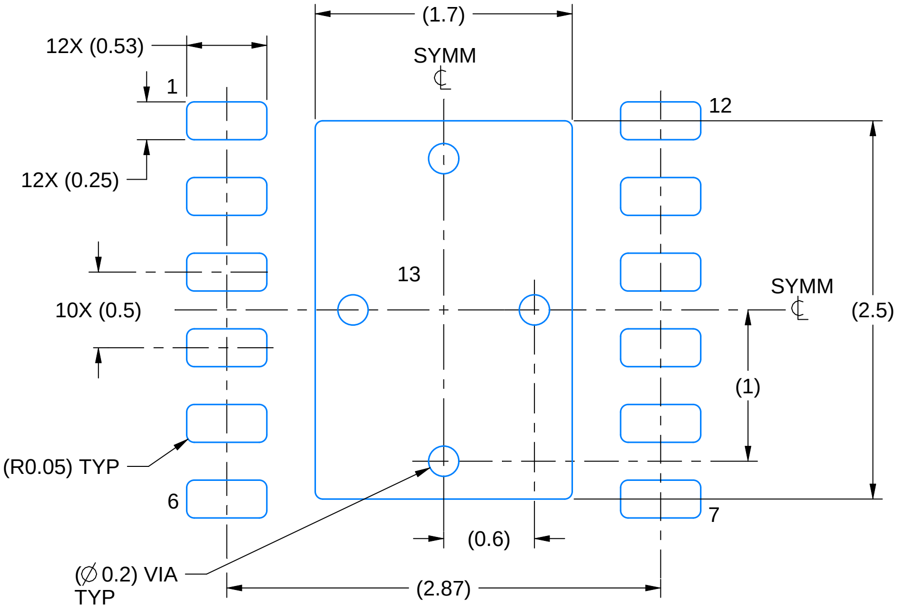


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

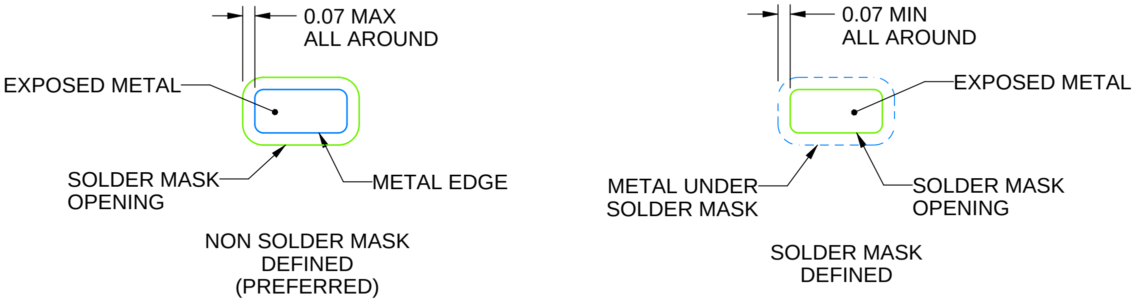


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



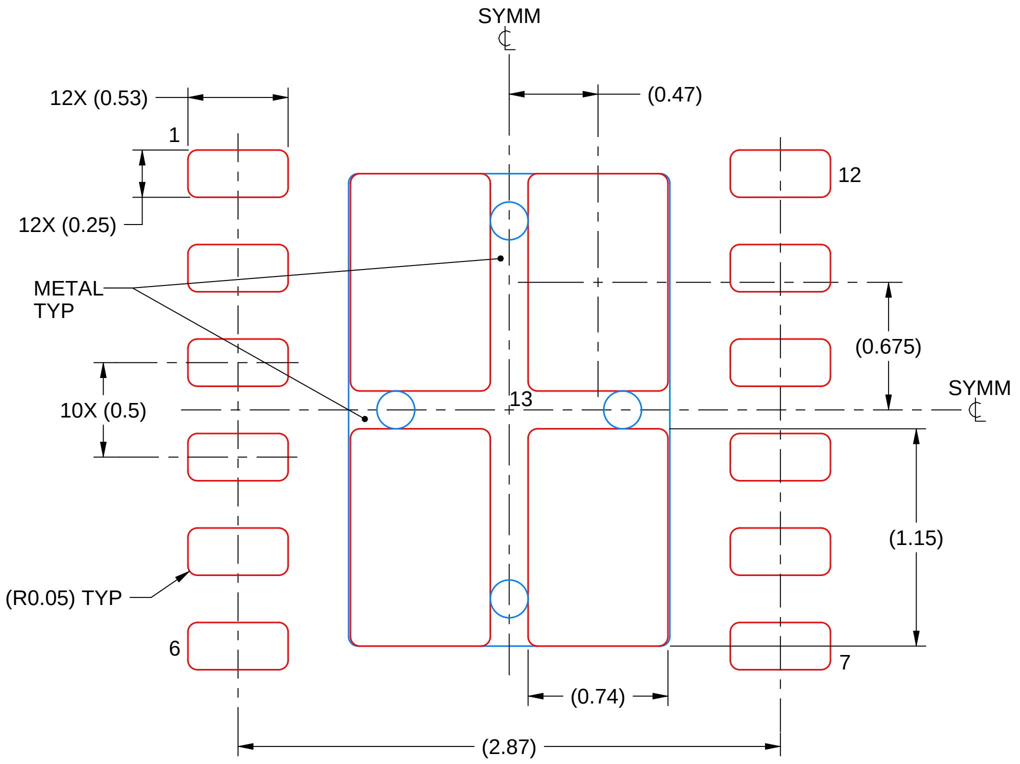
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80.1% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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