PIN CONFIGURATION



CE ATUDES

Multi-Protocol Universal Synchronous Receiver/Transmitter USYNR/T

| FEATURES | 1 | | |
|---|---|--|---|
| <u> </u> | | | |
| ☐ Selectable Protocol—Bit or Byte oriented | | V∞ [1 | 40 MSEL |
| ☐ Direct TTL Compatibility | | RCP ☐ 2 | 39 TCP 38 TSO |
| | | RSI ☐ 3 SFR ☐ 4 | 37 TXENA |
| ☐ Three-state Input/Output BUS | | RXACT 5 | 36 TSA |
| □ Processor Compatible—8 or 16 bit | RDA 6 | 35 TBMT | |
| ☐ High Speed Operation—1.5 M Baud—typical | | RSA 7 | 34 TXACT |
| Thigh Open Operation To the Status and Car | RXENA 8 | 33 MR | |
| ☐ Fully Double Buffered—Data, Status, and Co | ruoi negisteis | GND 9 | 32 □ Vcc 31 □ DBØØ |
| ☐ Full or Half Duplex Operation—independent 7 | DBØ8 [10 | 30 DBØ1 | |
| Receiver Cloc | | DBØ9 [11 DB1Ø [12 | 29 DB#2 |
| —individually se | | DB11 13 | 28 DBØ3 |
| | | DB12 14 | 27 DBØ4 |
| length for Rec | eiver and | DB13 ⊈15 | 26 DBØ5 |
| Transmitter | | DB14 16 | 25 D 08Ø6 |
| ☐ Master Reset—resets all Data, Status, and C | ontrol Registers | DB15 17 | 24 DBØ7 23 DPENA |
| The interpolated built in colf checking | | W R 18 A2 19 | 23 DPENA 22 BYTE OP |
| ☐ Maintenance Select—built-in self checking | | A1 20 | 21 AØ |
| | | | |
| | | PACKAGE: | 40-Pin D.I.P. |
| BIT ORIENTED PROTOCOLS—SDLC, HDLC, ADCCP Automatic bit stuffing and stripping Automatic frame character detection and generation Valid message protection—a valid received message is protected from overrun Residue Handling—for messages which terminate with a partial data byte, the number of valid data bits is available SELECTABLE OPTIONS: Variable Length Data—1 to 8 bit bytes Error Checking—CRC (CRC16, CCITT-0, or CCITT-1)—None Primary or Secondary Station Address Mode All Parties Address—APA Extendable Address Field—to any number of bytes Extendable Control Field—to 2 bytes Idle Mode—idle FLAG characters or MARK the line Point to Point, Multi-drop, or Loop Configuration | BYTE ORIENTED PROT Automatic detection ar SELECTABLE OPTIONS Variable Length Data— Variable SYNC charac Error Checking—CRC —None Strip Sync—deletion o synchroni Idle Mode—idle SYNC | nd generation of S S: -1 to 8 bit bytes cter—5, 6, 7, or 8 b (CRC16, CCITT-((odd/even parity) f leading SYNC characteristy | yNC characters its 0, or CCITT-1) haracters after |
| APPLIC | ATIONS | | |
| ☐ Intelligent Terminals | ☐ Remote Data Con | centractors | |
| ☐ Line Controllers | ☐ Communication 7 | | t |
| | | | • |
| ☐ Network Processors | □ Computer to Com | iputer Liriks | |

☐ Front End Communications

☐ Hard Disk Data Handler

General Description

The COM 5025 is a COPLAMOS® n channel silicon gate MOS/LSI device that meets the majority of synchronous communications requirements, by interfacing parallel digital systems to synchronous serial data communication channels while requiring a minimum of controller overhead.

The COM 5025 is well suited for applications such as computer to modern interfaces, computer to computer serial links and in terminal applications. Since higher level decisions and responses are made or initiated by the controller, some degree of intelligence in each controller of the device is necessary.

Newly emerging protocols such as SDLC, HDLC, and ADCCP will be able to utilize the COM 5025 with a high degree of efficiency as zero insertion for transmission and zero deletion for reception are done automatically. These protocols will be referred to as Bit Oriented Protocols (BOP). Any differences between them will be discussed in their respective sections. Conventional synchronous protocols that are control character oriented such as BISYNC can also utilize this device. Control Character oriented protocols will be referred to as CCP protocols. Other types of protocols that operate on a byte or character count basis can also utilize the COM 5025 with a high degree of efficiency in most cases. These protocols, such as DDCMP will also be referred to as CCP protocols.

The COM 5025 is designed to operate in a synchronous communications system where some external source is expected to provide the necessary received serial data, and all clock signals properly synchronized according to EIA standard RS334. The external controller of the chip will provide the necessary control signals, intelligence in interpreting control signals from the device and data to be transmitted in accord with RS334.

The receiver and transmitter are as symmetrical as possible without loss of efficiency. The controller of the device will be responsible for all higher level decisions and interpretation of some fields within message frames. The degree to which this occurs is dependent on the protocol being implemented. The receiver and transmitter logic operate as two totally independent sections with a minimum of common logic.

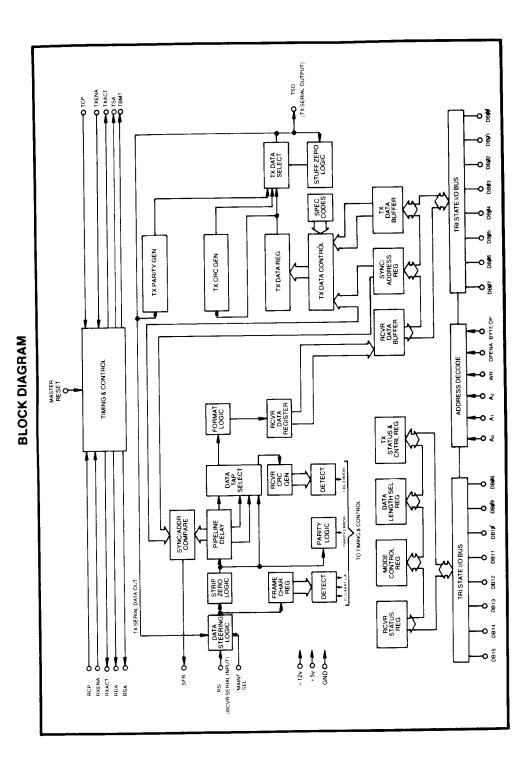
References:

- ANSI—American National Standards Institute X353, XS34/589 202-466-2299
- CCITT—Consultative Committee for International Telephone and Telegraph X.25
 202-632-1007
- 3. EIA—Electronic Industries Association TR30, RS334 202-659-2200
- IBM
 General Information Brochure, GA27-3093

 Loop Interface—OEM Information, GA27-3098
 System Journal—Vol. 15, No. 1, 1976; G321-0044

Terminology

| Term | Definition | Term | Definition |
|-------|--|------|---|
| ВОР | Bit Oriented Protocols: SDLC, HDLC, ADCCP | GA | 01111111 (0 (LSB) followed by 7-1's) |
| CCP | Control Character Protocols: BiSync, DDCMP | LSB | First transmitted bit, First received bit |
| TDB | Transmitter Data Buffer | MSB | Last transmitted bit, Last received bit |
| RDB | Receiver Data Buffer | RDP | Receiver Data Path |
| TDSR | Transmitter Data Shift Register | TDP | Transmitter Data Path |
| FLAG | 01111110 | LM | Loop Mode |
| ABORT | 11111111 (7 or more contiguous 1's) | | |



Description of Pin Functions

| Pin No. | Symbol | Name | 1/0 | Function | | | | |
|---------|---------|---------------------------------|-----|--|--|--|--|--|
| 1 | Voo | Power Supply | PS | + 12 volt Power Supply. | | | | |
| 2 | RCP | Receiver Clock | 1 | The positive-going edge of this clock shifts data into the receiver shift register. | | | | |
| 3 | RSI | Receiver Serial Input | | This input accepts the serial bit input stream. | | | | |
| 4 | SFR | Sync/Flag Received | ó | This output is set high, for 1 clock time of the RCP, each time a sync or flag character is received. | | | | |
| 5 | RXACT | Receiver Active | 0 | This output is asserted when the RDP presents the first data character of the message to the controller. In the BOP mode the first data character is the first non-flag character (address byte). In the CCP mode: 1. if strip-sync is set; the first non-sync character is the first data character 2. if strip-sync is not set; the first data character 2. if strip-sync is not set; the first data character is the character following the second sync. In the BOP mode the trailing (next) FLAG resets RXACT. In the CCP mode RXACT is never reset, it can be cleared via RXENA. | | | | |
| 6 | RDA | Receiver Data Available | 0 | This output is set high when the RDP has assembled an entire character and transferred it into the RDB. This output is reset by reading the RDB. | | | | |
| 7 | RSA | Receiver Status Available | 0 | This output is set high: 1. CCP—in the event of receiver over run (ROR) or parity error (if selected), 2. BOP—in the event of ROR, CRC error (if selected receiving REOM or RAB/GA. This output is reset by reading the receiver status register or dropping of RXENA. | | | | |
| 8 | RXENA | Receiver Enable | I | A high level input allows the processing of RSI data. A low level disables the RDP and resets RDA, RSA and RXACT. | | | | |
| 9 | GND | Ground | GND | Ground | | | | |
| 10 | DBØ8 | Data Bus | 1/0 | Bidirectional Data Bus. | | | | |
| 11 | DBØ9 | Data Bus | 1/0 | Bidirectional Data Bus. | | | | |
| 12 | DB1Ø | Data Bus | I/O | Bidirectional Data Bus. | | | | |
| 13 | DB11 | Data Bus | 1/0 | | | | | |
| | DB12 | Data Bus | | Z TANO OIL THE DEEP SEP. | | | | |
| 14 | | | 1/0 | | | | | |
| 15 | DB13 | Data Bus | 1/0 | Bidirectional Data Bus. | | | | |
| 16 | DB14 | Data Bus | I/O | Bidirectional Data Bus. | | | | |
| 17 | DB15 | Data Bus | I/O | Bidirectional Data Bus. J | | | | |
| 18 | W/R | Write/Read | - 1 | Controls direction of data port. W/R=1, Write. W/R=0, Read. | | | | |
| 19 | A2 | Address 2 | - 1 | Address input—MSB. | | | | |
| 20 | A1 | Address 1 | - 1 | Address input. | | | | |
| 21 | AØ | Address 0 | - 1 | Address input—LSB. | | | | |
| 22 | BYTE OP | Byte Operation | 1 | If asserted, byte operation (data port is 8 bits wide) is selected. If BYTE OP=0, data port is 16 bits wide. | | | | |
| 23 | DPENA | Data Port Enable | I | Strobe for data port. After address, byte op, W/R and data are set-up DPENA may be strobed. If reading the port, DPENA may reset (depending on register selected by address) RDA or RSA. If writing into the port, DPENA may reset (depending on register selected by address) TBMT. | | | | |
| 24 | DBØ7 | Data Bus | I/O | Bidirectional Data Bus—MSB. | | | | |
| 25 | DBØ6 | Data Bus | I/O | Bidirectional Data Bus. | | | | |
| 26 | DBØ5 | Data Bus | 1/0 | Bidirectional Data Bus. | | | | |
| 27 | DBØ4 | Data Bus | 1/0 | Bidirectional Data Bus. | | | | |
| | | | | | | | | |
| 28 | DBØ3 | Data Bus | 1/0 | Bidirectional Data Bus. | | | | |
| 29 | DBØ2 | Data Bus | I/O | Bidirectional Data Bus. | | | | |
| 30 | DBØ1 | Data Bus | 1/0 | Bidirectional Data Bus. | | | | |
| 31 | DBØØ | Data Bus | I/O | Bidirectional Data BusLSB. | | | | |
| 32 | Vcc | Power Supply | PS | +5 volt Power Supply. | | | | |
| 33 | MR | Master Reset | I | This input should be pulsed high after power turn on. This will: clear all flags, and status conditions, set TBMT=1, TSO=1 and place the device in the primary BOP mode with 8 bit TX/RX data length, CRC CCITT initialized to all 1's. | | | | |
| 34 | TXACT | Transmitter Active | 0 | This output indicates the status of the TDP. TXACT will go high after asserting TXENA and TSOM coinsidently with the first TSO bit. This output will reset one half clock after the byte during which TXENA is dropped. | | | | |
| 35 | ТВМТ | Transmitter Buffer Empty | 0 | This output is at a high level when the TDB or the TX Status and Control Register may be loaded with the new data. TBMT=0 on any write access to TDB or TX Status and Control Register. TBMT returns high when the TDSR is loaded. | | | | |
| 36 | TSA | Transmitter Status Available | 0 | TERR bit, indicating transmitter underflow. Reset by MR or assertion of TSOM. | | | | |
| 37 | TXENA | Transmitter Enable | 1 | A high level input allows the processing of transmitter data. | | | | |
| 38 | TSO | Transmitter Serial Output | 0 | This output is the transmitted character. | | | | |
| 39 | TCP | Transmitter Clock | 1 | The positive going edge of this clock shifts data out of the transmitter shift register. | | | | |
| 40 | MSEL | Maintenance Select | I | Internally RSI becomes TSO and RCP becomes TCP. Externally RSI is disabled and TSO=1. | | | | |
| | | | | | | | | |

Definition of Terms Register Bit Assignment Chart 1 and 2

| D889 RSOM Receiver Start of Message—resol only bit. In BOP mode only, opes high when first non-fleig daddress byte) character loaded into the Tion (D81 is cleared with the second byte) is olded into the Tion of the Start of Message—resol only bit. In BOP mode only, set high when first non-fleig daddress byte) Receiver first of Message—resol only bit. In BOP mode only, set high when first non-fleig daddress byte.) Receiver for for I Message—resol only bit. In BOP mode only, set high with only bit. In BOP mode only, mode on | Data Bu | Term | Definition | |
|--|--------------|-----------------|--|-----------|
| character loaded rink PRD. It is cleared when the second bytes is clapid and the rever of table loaded into PRD. It is cleared from the second from the property of the proper | | DCOM | Receiver Start of Message—read only bit. In BOP mode only, goes high when first non-flag (address byte) | |
| when an ABOPT character's received. It is clared on reading on receiver Statist Register to the state and wing an ABOPT Character's Color of the Col | | | character loaded into RDB. It is cleared when the second byte is loaded into the RDB. | |
| RABIGA Received ABORT or GO AHEAD character, read only 5t. In EUP mode arely. If will be seared on reading of ABORT character; If Little - this bit is a PERSA. ABORT character; If Little - this bit is a PERSA. Receiver Over Rum—read only bit. Set high with cross-vocated data transferred into RDB and previous data has not been read, indicating plaint to is serviced by which none character time. Closed on orasiding of Receiver Status. Register or dropping of RVERA. Regis | DB Ø9 | REOM | | ř |
| DB15 ERR CHK CPC mode: 1, set high it party sistered and received in error, a samine when RECM=1, in CPC mode: 1, set high it party sistered and received in error, at CRC selected (setted and end of each byte) ERR CHK = 1 if CRC GOOD. ERR CHK = 0 if CRC NOT GOOD. Controller must determine the lists byte of the massage. Transmiter Start of Message—With bit in Provided TXRH. = 1, StOM, and in CCP+1. IDLE=0, International of Stomphylogical Start (Stort Stort | DB1Ø | RAB/GA | Described ADODT or CO ALEAD character read only hit in HOP mode only. II LM = 0 this bit is set of receiving an | gist |
| DB15 ERR CHK CPC mode: 1, set high it party sistered and received in error, a samine when RECM=1, in CPC mode: 1, set high it party sistered and received in error, at CRC selected (setted and end of each byte) ERR CHK = 1 if CRC GOOD. ERR CHK = 0 if CRC NOT GOOD. Controller must determine the lists byte of the massage. Transmiter Start of Message—With bit in Provided TXRH. = 1, StOM, and in CCP+1. IDLE=0, International of Stomphylogical Start (Stort Stort | | | Describes Chattan Register or dropping of RYENA | , Re |
| DB15 ERR CHK CPC mode: 1, set high it party sistered and received in error, a samine when RECM=1, in CPC mode: 1, set high it party sistered and received in error, at CRC selected (setted and end of each byte) ERR CHK = 1 if CRC GOOD. ERR CHK = 0 if CRC NOT GOOD. Controller must determine the lists byte of the massage. Transmiter Start of Message—With bit in Provided TXRH. = 1, StOM, and in CCP+1. IDLE=0, International of Stomphylogical Start (Stort Stort | DB11 | ROR | a control of the second and the control of the cont | atus |
| DB15 ERR CHK CPC mode: 1, set high it party sistered and received in error, a samine when RECM=1, in CPC mode: 1, set high it party sistered and received in error, at CRC selected (setted and end of each byte) ERR CHK = 1 if CRC GOOD. ERR CHK = 0 if CRC NOT GOOD. Controller must determine the lists byte of the massage. Transmiter Start of Message—With bit in Provided TXRH. = 1, StOM, and in CCP+1. IDLE=0, International of Stomphylogical Start (Stort Stort | | | S 11 dispersion of DVENIA | ŗs |
| DB15 ERR CHK CPC mode: 1, set high it party sistered and received in error, a samine when RECM=1, in CPC mode: 1, set high it party sistered and received in error, at CRC selected (setted and end of each byte) ERR CHK = 1 if CRC GOOD. ERR CHK = 0 if CRC NOT GOOD. Controller must determine the lists byte of the massage. Transmiter Start of Message—With bit in Provided TXRH. = 1, StOM, and in CCP+1. IDLE=0, International of Stomphylogical Start (Stort Stort | DB12-14 | A, B, C | a will a Dia County good only bits. In BOD mode only examine when REOM=1, ABC=0, message terminated | ie Sie |
| DB15 ERR CHK CPOT Chock—read only bit. In BOP set high if LPGC selected and received in error, a samine when RECM=1. In CPC CP mode 1. set high it party selected and received in error, a semine when RECM=1. In CPC CP mode 1. set high it party selected and received in error, a selected (setted at and of each byte) ERR CHK - I I CPC CP mode 1. set high it party selected and received in error, a selected (setted and of each byte) ERR CHK - I I I CPC controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must determine the lists byte of the measure of the controller must be measured byte of the controller must be measured by ELAG. DB16 TXAB Transmit Go Ahead—Wilk Dit. In BCP mode only, TXAB = 1 finish present character then: 1. DLE=0, transmit and the controller must be controller. Transmitter Error—read only bit. Underflow, set high when TDB not loaded in time to maintain controller. Transmitter Error—read only bit. Underflow set high when TDB not loaded in time to maintain controller. Transmitter Error—read only bit. Underflow set high when TDB not loaded in time to maintain controller. Transmitter Error—read only bit. Underflow set high when TDB not loaded in time to maintain controller. Transmitter Error—read only bit. Underflow set high when TDB not loaded in time to maintain controller. Transmitter Error—read | | | to the state of the problem of the p | ěč |
| CCP mode 1. set high flaphy selected and received in error, CPL rev. selected rest of the message. DR 1 FSOM Transmiter Start of Massage—Wilk bit Provided TXENA=1, TSOM initiates start of message in BOP, TSOM=1 from the set byte of the message in BOP received and start of the selection of the | DB15 | ERR CHK | - OLD JUDIE AND SELECTION OF SIGN IS CONTROL OF SIGN O | _ |
| Transmitter Start of Message—W/R bit. Provided TXENA=1, TSOM initiates start of message in RDP, TSOM=1 Transmitter Start of Message—W/R bit. Provided TXENA=1, TSOM initiates start of message in RDP, TSOM=1 September of the Start of Start Start of Message in RDP mode there is also a Special Space Sequence W/R bit. Head for the Start Start Start of Message in RDP mode there is also a Special Space Sequence W/R bit. Used to terminate a message. In RDP mode, TEOM=1 sends CRC, then FLAG; if TXENA=1 and TEOM=1 continue to send SYNCs, if TXENA=0 and TEOM=1 IDLE=0, TEOM=1 send SYNCs, if TXENA=1 and TEOM=1 continue to send SYNCs, if TXENA=0 and TEOM=1 IDLE=0, TEOM=1 send SYNCs, if TXENA=1 and TEOM=1 continue to send SYNCs, if TXENA=0 and TEOM=1 IDLE=0, TEOM=1 send SYNCs, if TXENA=1 and TEOM=1 continue to send SYNCs, if TXENA=0 and TEOM=1 IDLE=0, TEOM=1 send SYNCs, if TXENA=1 and TEOM=1 continue to send SYNCs, if TXENA=0 and TEOM=1 IDLE=0, TEOM=1 send SYNCs, if TXENA=1 and TEOM=1 continue to send SYNCs, if TXENA=0 and TEOM=1 IDLE=0, TEOM=1 send SYNCs, if TXENA=1 and TEOM=1 continue to send SYNCs, if TXENA=0 and TEOM=1 IDLE=0, TEOM=1 send SYNCs, if TXENA=1 and TEOM=1 continue to send SYNCs, if TXENA=0 and TEOM=1 IDLE=0, TEOM=1 send TEOM=1 continue to send TEOM=1 contin | | | and the second of the second o | |
| Section Sect | | | message | |
| SYNC register, continue until TSOM -0, then begin data 2. IULE = 1 transmits of interest by the service and special Space Sequence of 16 of 5 initiated by TSOM = 1 and TEOM = 1 SSO in TEOM = 1 service and SCRC, then Transmit End of Message—WR But. Used to terminate a message INC =0 and TEOM = 1 sends CRC, then FLAG, if TXRM = 1 and TEOM = 1 orbit to terminate a message INC =0 and TEOM = 1 sends CRC, then INC = 1 service and TEOM = 1 orbit to terminate a message INC = 0 and TEOM = 1 sends CRC, then INC = 1 service and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send SVNCs, if TXENA = 0 and TEOM = 1 orbit to the send send svnc in the send send such send send send send send send send send | DB8 | TSOM | The Control Manager W/R bit Provided TYENA = 1 TSOM initiates start of message. In BOP, TSOM = 1 | |
| a Special Space Sequence of 16-0's initiated by 1'SUM-1 and 1EUM-1 SSS is TECHM-1's send's CRC, then FLAG; iTXENA-1 and TEOM-1's continue to send FLAGs, iTXENA-1's and TEOM-1's continue to Send's CRC, it and TEOM-1's continue to send SYNC's, it TXENA-0's and TEOM-1's continue to send SYNC's an | | | EVAIC society, continue until TSOM=0, then begin data, 2, IDLE=1 transmit out of 1 DB, in BOP mode inere is also | |
| DB15 TERR | | | - C Conso Converse of 16.0's initiated by TSOM=1 and LEOM=1, 355 is followed by FLAG. | te. |
| DB15 TERR | DB9 | TEOM | FLAC X TVENA 1 and TEOM 1 continue to condit AGS IT IXENA = U and I EOM = I MANN HID. III OUT 1. | atus |
| DB15 TERR | | | IDLE=0, TEOM=1 send SYNC, if TXENA=1 and TEOM=1 continue to send SYNC's, if TXENA=0 and TEOM=1 | £ 5 |
| DB15 TERR | | | ALLOW DE A TECNA A MARK BAC | ite |
| DB15 TERR | DB1Ø | TXAB | O IDLE 1 transmit ELAG | န်း ၁ |
| TERR | DB11 | TXGA | Transmit Go Ahead—W/R bit. In BOP mode only, modifies character called for by TEOM. GA sent in place of FLAG. | Trai |
| Table | D016 | TEDD | The second service and columbit Linderflow, set high when TDR not loaded in time to maintain continuous | |
| DB1-16 | DB 13 | Liuv | transmission. In BOP automatically transmit: 1. IDLE=0, ABORT 2. IDLE=1, FLAG. In COP automatically transmit. | |
| DB11 IDLE | | | | |
| DB12 IDLE | DB8-1Ø | X,Y,Z | 0 0 X ¹⁶ + X ¹² + X ⁵ + 1 CCITT—Initialize to "1" | |
| DB11 IDLE Note: Description Note: Descrip | | | 0 0 1 X ¹⁶ + X ¹² + X ⁵ + 1 CCITT—Initialize to "0" | |
| DB11 IDLE IDLE mode select—WR bit. Affects transmitter only. In BOP—control the type of character sent when TXAB asserted or in the event of data underflow. In CCP—control the type of character sent when TXAB asserted or in the event of data underflow. In CCP—control the type of character transmission and underflow. "In CCP—controls the method of initial SYNC character transmission and underflow." "I = transmit SYNC from TDB." 0" = transmit SYNC from SYNC/ADDRESS register. DB12 SEC ADD Secondary Address Mode—W/R bit. In BOP mode only—after FLAG looks for address match prior to activating RDP, if no match found, begin FLAG search again. SEC ADD bit should not be set if EXADD= 1 or EXCON=1. DB13 STRIP SYNC/LOOP Stip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping. PROTOCOL—W/R bit. BOP=0, CCP=1 AIP arties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP. Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 1 Five bits per character 1 0 1 Three bits per character 1 1 1 Seven bits per character 1 1 1 Three bits per character 1 1 1 Seven bits per character 1 1 1 Three bits per chara | | | 100 Mg 100 4 00040 | |
| BDB. if no match found, begin FLAG search again. SEC ADD bit should not be set if EADD = 10 EAODN=1. BDB13 STRIP SYNC/LOOP Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping. PROTOCOL—W/R bit. BOP=0, CCP=1 All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP. Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 1 0 Four bits per character 1 1 0 Four bits per character 1 1 0 Two bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 1 To Two bits per character* 1 To Two bits per character the secondary mode so that the secondary address or 8-1's will activate the RDP. DB8-10 RXDL RXDL RXDL RXDL RXDL RECEIVED TABLE BIT IN TABLE RXDL RECEIVED TABLE BIT IN TABLE RXDL RXD | | | 1 0 Odd Parity—CCP Only | ter |
| BDB. if no match found, begin FLAG search again. SEC ADD bit should not be set if EADD = 10 EAODN=1. BDB13 STRIP SYNC/LOOP Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping. PROTOCOL—W/R bit. BOP=0, CCP=1 All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP. Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 1 0 Four bits per character 1 1 0 Four bits per character 1 1 0 Two bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 1 To Two bits per character* 1 To Two bits per character the secondary mode so that the secondary address or 8-1's will activate the RDP. DB8-10 RXDL RXDL RXDL RXDL RXDL RECEIVED TABLE BIT IN TABLE RXDL RECEIVED TABLE BIT IN TABLE RXDL RXD | | | | egis |
| BDB. if no match found, begin FLAG search again. SEC ADD bit should not be set if EADD = 10 EAODN=1. BDB13 STRIP SYNC/LOOP Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping. PROTOCOL—W/R bit. BOP=0, CCP=1 All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP. Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 1 0 Four bits per character 1 1 0 Four bits per character 1 1 0 Two bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 1 To Two bits per character* 1 To Two bits per character the secondary mode so that the secondary address or 8-1's will activate the RDP. DB8-10 RXDL RXDL RXDL RXDL RXDL RECEIVED TABLE BIT IN TABLE RXDL RECEIVED TABLE BIT IN TABLE RXDL RXD | | | 1 1 Inhibit all error detection and transmission | Œ, |
| BDB. if no match found, begin FLAG search again. SEC ADD bit should not be set if EADD = 10 EAODN=1. BDB13 STRIP SYNC/LOOP Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping. PROTOCOL—W/R bit. BOP=0, CCP=1 All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP. Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 1 0 Four bits per character 1 1 0 Four bits per character 1 1 0 Two bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 1 To Two bits per character* 1 To Two bits per character the secondary mode so that the secondary address or 8-1's will activate the RDP. DB8-10 RXDL RXDL RXDL RXDL RXDL RECEIVED TABLE BIT IN TABLE RXDL RECEIVED TABLE BIT IN TABLE RXDL RXD | | IDI E | IDLE made calcat. W/P bit Affacts transmitter only. In ROP—control the type of character sent when I AAD | ţ |
| BDB. if no match found, begin FLAG search again. SEC ADD bit should not be set if EADD = 10 EAODN=1. BDB13 STRIP SYNC/LOOP Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping. PROTOCOL—W/R bit. BOP=0, CCP=1 All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP. Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 1 0 Four bits per character 1 1 0 Four bits per character 1 1 0 Two bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 1 To Two bits per character* 1 To Two bits per character the secondary mode so that the secondary address or 8-1's will activate the RDP. DB8-10 RXDL RXDL RXDL RXDL RXDL RECEIVED TABLE BIT IN TABLE RXDL RECEIVED TABLE BIT IN TABLE RXDL RXD | וושט | IDLE | accorded or in the event of data underflow. In CCP—controls the method of initial SYNC character transmission and | ပိ |
| BDB. if no match found, begin FLAG search again. SEC ADD bit should not be set if EADD = 10 EAODN=1. BDB13 STRIP SYNC/LOOP Strip Sync or Loop Mode—W/R bit. Effects receiver only. In BOP mode—allows recognition of a GA character. In CCP—after second SYNC, strip SYNC; when first data character detected, set RXACT=1, stop stripping. PROTOCOL—W/R bit. BOP=0, CCP=1 All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP. Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 1 0 Four bits per character 1 1 0 Four bits per character 1 1 0 Two bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character* 1 To Two bits per character* 1 To Two bits per character the secondary mode so that the secondary address or 8-1's will activate the RDP. DB8-10 RXDL RXDL RXDL RXDL RXDL RECEIVED TABLE BIT IN TABLE RXDL RECEIVED TABLE BIT IN TABLE RXDL RXD | | | underflow, "1" = transmit SYNC from TDB, "0" = transmit SYNC from SYNC/ADDRESS register. | ode |
| DB13 STRIP SYNC/LOOP DB14 PROTOCOL DB15 'APA DB15 'APA DB13-15 TXDL Transmitter Data Length—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP. Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 0 Six bits per character 1 1 0 Five bits per character 1 1 0 Three bits per character* 0 1 1 Three bits per character* 0 1 0 Three bits per character (CCP mode). DB8-10 RXDL R | DB12 | SEC ADD | DDD if no motor found, begin ELAG search again, SEC ADD bit should not be set it EXADD = 1 of EXCON = 1. | Σ |
| DB14 PROTOCOL APA PROTOCOL—W/R bit. BOP=0, CCP=1 All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address or 8-1's will activate the RDP. TXDL Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 1 Seven bits per character 1 1 0 Five bits per character 1 0 1 Five bits per character 1 0 1 Three bits per character* 0 1 1 Three bits per character* 0 1 0 Two bits per character 1 0 O Six bits per character* 1 0 O Six bits per character 1 0 O Six bits per character 1 1 1 Seven bits per character 1 1 1 Three bits per character | DB13 | STRIP SYNC/LOOP | Ctrin Sync or Loop Mode | |
| All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address of 8-13 will activate the RDP. DB13-15 TXDL Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 LENGTH 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 0 Six bits per character 1 1 0 Five bits per character 1 0 1 Five bits per character 1 0 1 Three bits per character 0 1 1 Three bits per character* 0 1 0 Two bits per character* 1 0 0 1 Two bits per character 1 0 0 1 Two bits per character 1 0 0 1 Cone bit per character (CCP mode). DB8-10 RXDL RXDL RXDL3 RXDL2 RXDL1 LENGTH 0 0 0 Eight bits per character 1 1 1 Seven bits per character 1 1 1 Seven bits per character 1 1 1 Seven bits per character 1 1 1 Three bits per character 1 1 1 Three bits per character 1 1 1 Three bits per character 1 1 Three bits per character 2 Table Betweeded Control Field—W/R bit. In receiver only: if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. | DB14 | PROTOCOL | PROTOCOL W/R bit BOR-0 CCP=1 | |
| Transmitter Data Length—W/R bits. TXDL3 TXDL2 TXDL1 | | | All Parties Address—W/R bit. If selected, modifies secondary mode so that the secondary address of 6-15 will | |
| TXDL3 TXDL2 TXDL1 | | | | |
| 1 | DB13-15 | TXDL | TXDL3 TXDL2 TXDL1 LENGTH | |
| 1 | | | | |
| 1 | | | | |
| 0 | | | 1 0 1 Five bits per character | |
| 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character 0 0 1 One bit per character DB11 EXCON Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. Extended Address Field—W/R bit. In receiver only: LSB of address byte tested for a "1". If NO—continue receiving | | | The state of the s | ter |
| 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character 0 0 1 One bit per character DB11 EXCON Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. Extended Address Field—W/R bit. In receiver only: LSB of address byte tested for a "1". If NO—continue receiving | | | 0 1 0 Two bits per character* | egis |
| 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character 0 0 1 One bit per character DB11 EXCON Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. Extended Address Field—W/R bit. In receiver only: LSB of address byte tested for a "1". If NO—continue receiving | | | 0 0 1 One bit per character* *For data length only, not to be used for SYNC character (CCP mode). | Œ. |
| 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character 0 0 1 One bit per character DB11 EXCON Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. Extended Address Field—W/R bit. In receiver only: LSB of address byte tested for a "1". If NO—continue receiving | DB8-1Ø | RXDL | Receiver Data Length—W/R bits. | ee |
| 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character 0 0 1 One bit per character DB11 EXCON Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. Extended Address Field—W/R bit. In receiver only: LSB of address byte tested for a "1". If NO—continue receiving | | | | E S |
| 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character 0 0 1 One bit per character DB11 EXCON Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. Extended Address Field—W/R bit. In receiver only: LSB of address byte tested for a "1". If NO—continue receiving | | | | ju j |
| 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 One bit per character 0 0 1 One bit per character DB11 EXCON Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. Extended Address Field—W/R bit. In receiver only: LSB of address byte tested for a "1". If NO—continue receiving | | | and the second s | ä |
| 0 1 1 Three bits per character 0 1 0 Two bits per character 0 0 1 0 Two bits per character 0 0 1 One bit per character 0 0 1 One bit per character DB11 EXCON Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. Extended Address Field—W/R bit. In receiver only; LSB of address byte tested for a "1". If NO—continue receiving | | | | Dat |
| 0 0 1 One bit per character DB11 EXCON Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. Extended Address Field—W/R bit. In receiver only: LSB of address byte tested for a "1". If NO—continue receiving | | | 0 1 1 Three bits per character | |
| DB11 EXCON Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should not be set if SEC ADD = 1. Extended Control Field—W/R bit. In receiver only; LSB of address byte tested for a "1". If NO—continue receiving | | | O 1 One bit per character | |
| not be set if SEC ADD ≈1. Extended Address Field—W/R bit In receiver only: LSB of address byte tested for a "1". If NO—continue receiving | DB11 | EXCON | Extended Control Field—W/R bit. In receiver only; if set, will receive control field as two 8-bit bytes. Excon bit should | |
| DB12 EAADD Extended Address it YES on into control field FXADD bit should not be set if SEC ADD = 1. | | | not be set if SEC ADD = 1. Expended Address Field—W/R bit In receiver only: LSB of address byte tested for a "1". If NO—continue receiving | |
| audiess bytes, in the go into control to the artists and the second of t | DB12 | EXAUD | address bytes, if YES go into control field. EXADD bit should not be set if SEC ADD = 1. | |

Register Bit Assignment Chart 1

| REGISTER | DPØ7 | DPØ6 | DPØ5 | DPØ4 | DPØ3 | DPØ2 | DPØ1 | DPgg |
|---|------|------|------|------|------|------|------|------|
| Receiver Data Buffer | RD7 | RD6 | RD5 | RD4 | RD3 | RD2 | RD1 | RDØ |
| (Read Only- Right Justified- Unused Bits=0) | MSB | | | | | | | LSB |
| Transmitter Data Register | TD7 | TD6 | TD5 | TD4 | TD3 | TD2 | TD1 | TDØ |
| (Read/Write- Unused Inputs=X) | MSB | | | | | | | LSB |
| Sync/Secondary | SSA7 | SSA6 | SSA5 | SSA4 | SSA3 | SSA2 | SSA1 | SSAØ |
| Address (Read/Write- Right Justified- Unused Inputs=X) | MSB | | | | | | | LSB |

Register Bit Assignment Chart 2

| REGISTER | DP15 | DP14 | DP13 | DP12 | DP11 | DP1Ø | DPØ9 | DPø8 |
|--|--------------------|----------|------------------------|---------|-------|--------|-------|-------|
| Receiver Status (Read Only) | ERR CHK | С | В | Α | ROR | RAB/GA | REOM | RSOM |
| TX Status and Control (Read/Write) | TERR (Read Only | y) O | 0 | 0 | TXGA | TXAB | TEOM | TSOM |
| Mode Control (Read/Write) | *APA | PROTOCOL | STRIP SYNC/ LOOP | SEC ADD | IDLE | Z | Y | X |
| Data Length Select (Read/Write) | TXDL3 | TXDL2 | TXDL1 | EXADD | EXCON | RXDL3 | RXDL2 | RXDL1 |

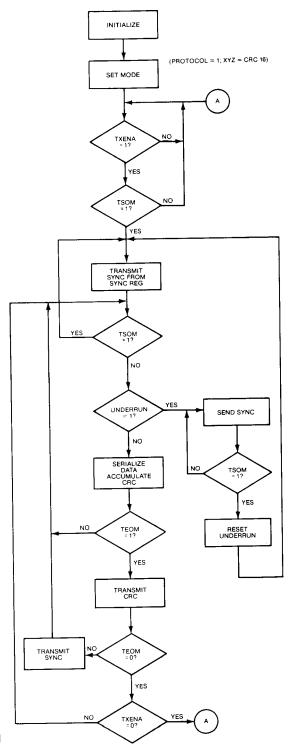
^{*} Note: Product manufactured before 1Q79 may not have this feature.

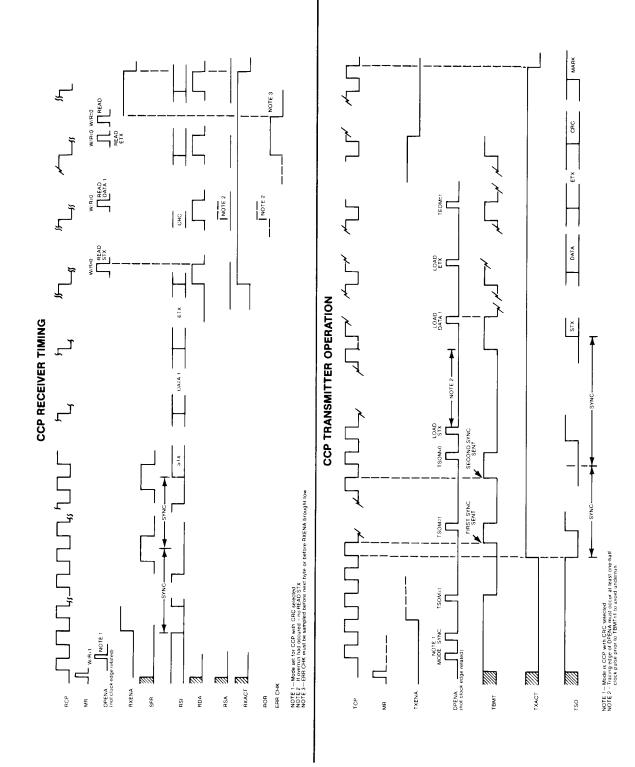
Register Address Selection

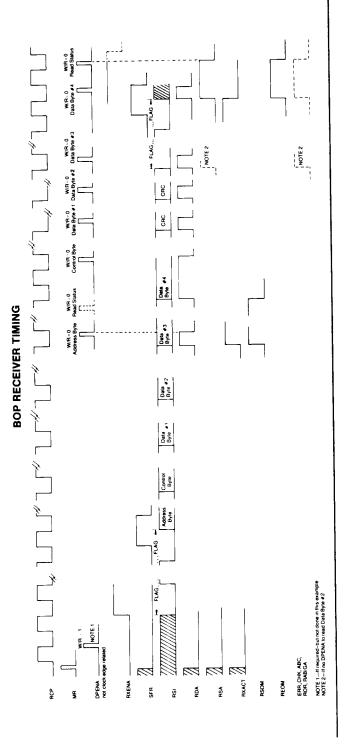
| 1) BYTE OP = | 0, data port 16 | bits wide | |
|----------------|------------------|-----------|---|
| A2 | A1 | AØ | Register |
| 0 | 0 | X | Receiver Status Register and Receiver Data Buffer |
| 0 | 1 | X | Transmitter Status and Control Register and Transmitter Data Buffer |
| 1 | 0 | X | Mode Control Register and SYNC/Address Register |
| 1 | 1 | X | Data Length Select Register |
| X = don't care | | | |
| | | | |
| 2) BYTE OP = | 1, data port 8 l | oits wide | |
| A2 | A1 | AØ | Register |
| 0 | 0 | 0 | Receiver Data Buffer |
| 0 | 0 | 1 | Receiver Status Register |
| 0 | 1 | 0 | Transmitter Data Buffer |
| 0 | 1 | 1 | Transmitter Status and Control Register |
| 1 | 0 | 0 | SYNC/Address Register |
| 1 | 0 | 1 | Mode Control Register |
| 1 | 1 | 0 | |
| 1 | 1 | 1 | Data Length Select Register |

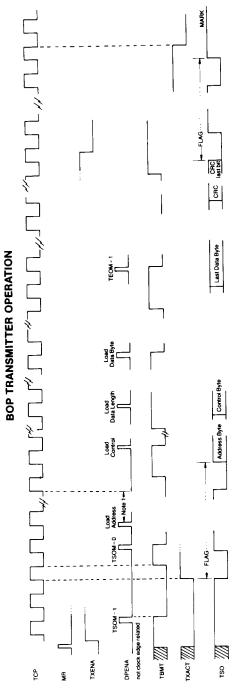
BOP TRANSMITTER OPERATION (PROCESSOR LOAD OR MASTER RESET) INITIALIZE MARK LINE TXENA = 1? YES NO TSOM = 1? Α YES SEND FLAG В YES TSOM = 1? NO SEND ABORT CHARACTER YES NO UNDERRUN = 12 YES NO TRANSMIT ABORT CHARACTER YES TXGA = 1? SEND GO AHEAD NO TSOM = 1? SEND CRC TEOM = 1? YES NO. RESET UNDERRUN SEND 1 BYTE OF DATA FROM TDB STUFF ZERO. ACCUMULATE CRC NO YES TXENA = 1?

CCP TRANSMITTER OPERATION



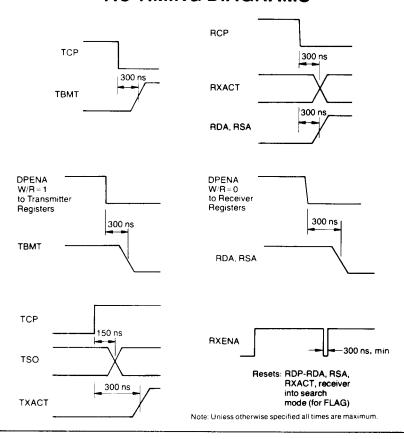




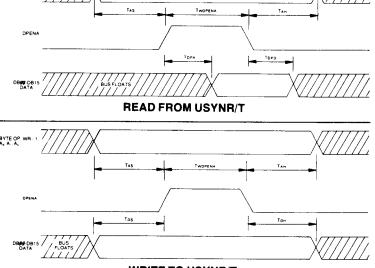


Note 1—Trailing edge of DPENA must occur at least one-half clock pulse pnor to TBMT = 1. To avoid underrun.

AC TIMING DIAGRAMS



Data Port Timing



MAXIMUM GUARANTEED RATINGS*

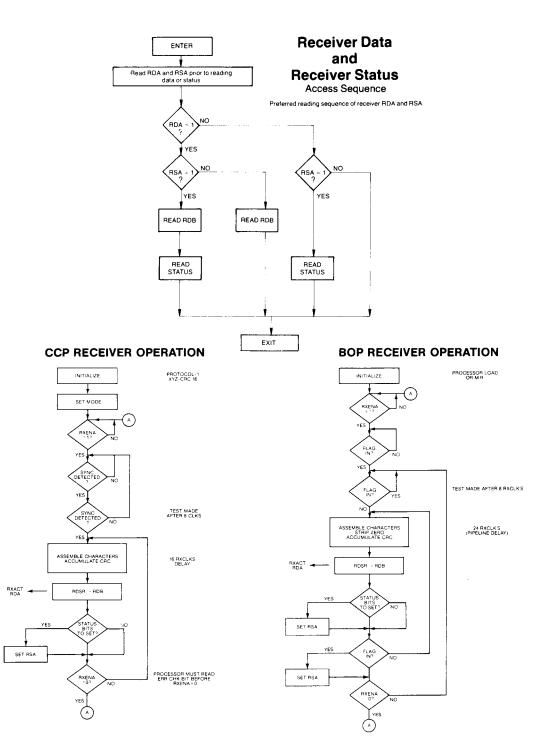
| Armitem der um met eine eine eine eine eine eine eine ei | 0°C to ± 70°C |
|--|-----------------|
| Operating Temperature Range | 55°C to 1150°C |
| Storage Temperature Range | 55 C 10 + 150 C |
| Lead Temperature (soldering, 10 sec.) | +325°C |
| Lead Temperature (soldering, To Sec.) | + 18.0V |
| Positive Voltage on any Pin, with respect to ground | 0.31/ |
| Negative Voltage on any Pin, with respect to ground | |

^{*}Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. For example, the bench power supply programmed to deliver +12 volts may have large voltage transients when the AC power is switched on and off. If this possibility exists it is suggested that a clamp circuit be used.

$\textbf{ELECTRICAL CHARACTERISTICS} \ (T_A=0^{\circ}C \ to \ 70^{\circ}C, \ V_{CC}=+5V\pm5\%, \ V_{DD}=+12V\pm5\%, \ unless \ otherwise \ noted)$

| Parameter | Min. | Тур. | Max. | Unit | Comments |
|--|------|------|-------|---------|--|
| D.C. Characteristics | | | | | |
| INPUT VOLTAGE LEVELS | į | | 1 | | |
| Low Level, Vil | | | 0.8 | V | |
| High Level, V⊪ | 2.0 | | Vcc | V | |
| OŬTPUT VOLTAGE LEVELS | | | | | 1.0 |
| Low Level, Vol | | | 0.4 | V | loL=1.6ma |
| High Level, Vон | 2.4 | | | | Іон=40µа |
| INPUT LEAKAGE | | | | | 0≤V _{IN} ≤5v, DPENA=0 or W/R= |
| Data Bus | | 5.0 | 50.0 | μa | Vin=+5v |
| All others | 1 | | | μa | VIN=+5V |
| INPUT CAPACITANCE | | | | | |
| Data Bus, Cin | | | | pf | |
| Address Bus, Cin | | | | pf | |
| Clock, Cin | | | | pf | |
| All other, Cin | | | | pf | |
| POWER SUPPLY CURRENT | l | | | | |
| Icc | | | 70 | ma | |
| loo | | | 90 | ma | |
| A.C. Characteristics | ĺ | | | | T _A =25°C |
| CLOCK-RCP, TCP | | ļ | 1 | | |
| frequency | DC | İ | 1.5 | MHz | |
| PWн | 325 | | | nş | |
| PWL | 325 | į. | | ns | |
| tr, tr | | 10 | | ns | |
| DPENA. TWOPENA | 250 | | 50 μs | ns | |
| Set-up Time, Tas | 0 | | | ns | |
| Byte Op, W/R | | | | | |
| A ₂ , A ₁ , A ₀ | | | | | |
| Hold Time, Tah | 0 | | | ns | |
| Byte Op, WIR, | | | | | |
| A ₂ , A ₁ , A ₀ | | | | | |
| DATA BUS ACCESS, TDPA | | | 150 | ns | |
| DATA BUS DISABLE DELAY, TOPO | | | 100 | ns | |
| DATA BUS SET-UP TIME, Tobs | 0 | 1 | | ns | |
| DATA BUS HOLD TIME, TOBH | 100 | 1 | ! | ns | |
| MASTER RESET, MR | 350 | 1 | | ns | |





Circuit diagrams utilizing SMC products are included as a means of illustrating typical semiconductor applications, consequently complete information sufficient for construction purposes is not necessarily given. The information has been carefully checked and is believed to be entirely reliable. However, no responsibility is assumed for inaccuracies. Furthermore, such information does not convey to the purchaser of the semiconductor devices described any license under the patent rights of SMC or others. SMC reserves the right to make changes at any time in order to improve design and supply the best product possible.