PLESSEY
Semiconductors

MV1815

T-77-07-05

SINGLE CHIP TELETEXT DECODER FOR 625 LINE OPERATION

The MV1815 is an advanced CMOS single chip Teletext decoder for 625 line World Standard Teletext Systems. The MV1815 has an on board data slicer circuit, dual page acquisition circuits, and direct memory addressing, which allow a low cost Teletext decoder to be built with a minimum number of additional components.

FEATURES

- On-Chip data slicing.
- Up to 254 display pages, using two low cost 200ns DRAMs.
- Low external component count.
- I²C Bus for low cost interfacing .
- Multi-language capability for fourteen European languages .
- Pinout to suit single sided PCB layout.
- Non-display packets stored for linked page operation, video programming, and other advanced uses.
- High resolution characters 16 by 10 dot matrix
- Advanced CMOS technology gives low power dissipation and high reliability.

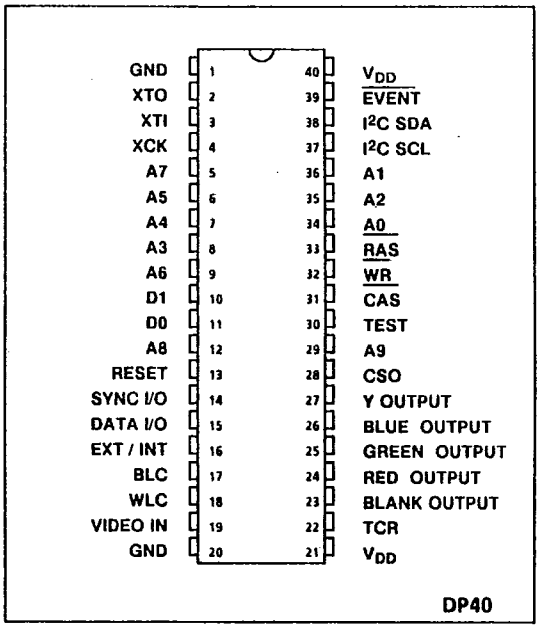

Figure 1. Pin Connections (top view)

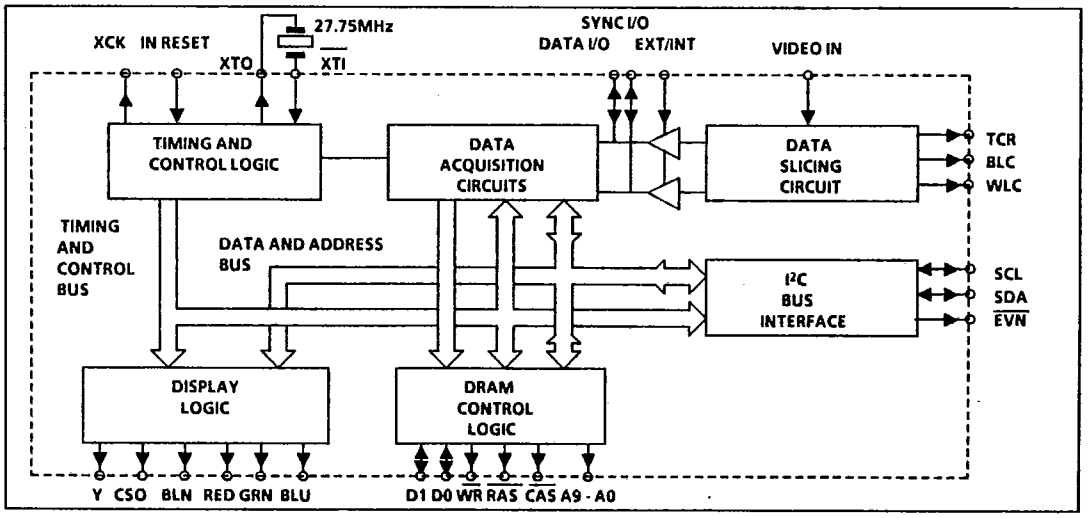

Figure 2. MV1815 Block diagram

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Section	Specification
Data Acquisition Logic	
Teletext data rate	625 Lines 50 Fields / second. 6.9375 Mbits / sec ± 25ppm.
Data line content	360 bits as 45 bytes of 8 bits each.
TV lines used VBI	Lines 6 to 22 and 319 to335.
TV lines used full field	Lines 6 to310 and 319 to 622. (display is interrupted during data acquistion).
Packets accepted	X/0 to X/25, X/26, X/27,X/28, X/29, 8/30 (formats 1 & 2), X/31.
Page numbers	00 to FF
Pages subcodes	0000 to 3F7F
Display Logic	
Characters per row	40, occupying 46.126µs of the 52µs display time
Teletext rows displayed	1 to 24 and 25 and 26 software switchable
TV lines used	Rows Start Finish 24 48 288 26 38 298
Character definition	16 x 10 dot matrix
Character Sets	English, German, Swedish, Italian,Belgian,Spanish, Czechoslovakian, Polish, Rumanian, Hungarian, Serbo Croat, Danish and American
Spacing control characters	Standard Level One Range
Data boxing into picture	Page Number - Row 1 characters 1 to 8 Page Header - Row 1 characters 9 to 32 Clock Time - Row 1 characters 33 to 40 Rows 25 and 26
Displayable page stores	14 to 254 each of 1K bytes, depending on the size of the DRAM being used
Display options	Picture, Text Mix of text foreground and picture background Three part magnify - display rows 1 to 12 rows 7 to 18 rows 13 to 24 Boxing of Newsflash and Subtitles into picture Boxing of picture into text.
Dynamic RAM Control Logic	
Device Type	2 off 1M x 1 or, 2 off 256K x 1 or, 2 of 64K x 1 with page or nibble mode operation.
Maximum access time (t_{RAC})	200ns.
Refresh period for complete memory	2.048ms. Refresh occurs during the line flyback period. Contents of any memory location may be accessed by the microprocessor via the I²C Bus interface.
I²C Bus Interface	Standard implementation of a slave transmitter / receiver. Control of the MV1815 is via 31 on - chip registers.

Table 1 MV1815 System Specification

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Device Description

The MV1815 is a single chip teletext decoder using an on chip data slicing circuit capable of receiving Teletext services broadcast to the WST Level 1+ standard, for display on 625 line TV receivers.

The device is controlled using a low cost I²C interface allowing easy interface to microprocessors. The register structure of the MV1815 allows the microprocessor to quickly read the Event and Page Receive registers, which hold information on the page being currently received. The chip requires only a single 27.75MHz crystal for all system clocks, this clock is internally divided by two to generate an external clock capable of driving the host microprocessor at 13.875MHz.

The MV1815 has dual acquisition circuits to ensure that the viewed page can always be kept live while the second acquisition circuit stores linked or other pages. It is possible for many linked page numbers to be transmitted in extra packet 27's. As the MV1815 has the capacity to store up to 254 different pages, it can store a complete magazine of linked pages.

The display memory uses two very low cost DRAMs. The DRAMs are controlled by the MV1815, including all the necessary refresh cycles. Refresh occurs during the flyback period on all ten address lines. The two DRAMs may be either: 64K x 1, 256K x 1, or 1M x 1 giving 14, 62, or 254 displayable pages in memory, plus two pages of store for non-display packets. These two pages will store two versions of packet 30 and two versions of packet 29 leaving the rest of the two pages to store any mix of packets 26, 27, or 28 up to a total maximum of 23 per acquistion circuit. It will be possible for the MV1815 to use two 4Mbyte DRAMs if the extra address lines are externally controlled.

Rows 25 & 26 can be displayed under software control. The contents of these lines will be optionally written by packets X/24 and X/25 dependent on the status of a register bit. A row zero write inhibit bit in a register will prevent the transmitted data in the header packet writing to memory, so that the microprocessor may process packet 8/30 data and write its own header line at the top of the screen. The displayed page can be enlarged into three overlapping half pages for ease of reading.

The on board character ROM holds 192 different characters with a resolution of 16 x 10 dots . This allows selective interlacing with high resolution characters, and a seven language capability.

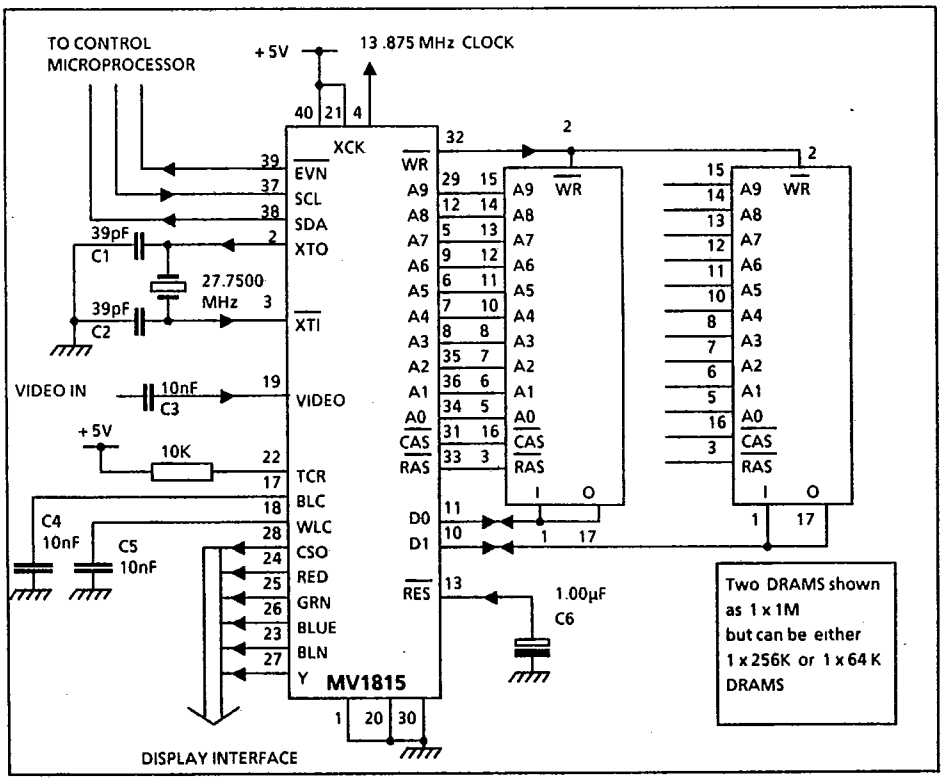

Figure 3. MV1815 applications circuit

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APPLICATION NOTES

The following notes assume that the MV1815 is to operate in a system which conforms to the principles of the teletext transmissions as described in the "World System Teletext Specifications".

The design of the MV1815 enables it to be incorporated in a system, using a minimum of external components, figure 3 shows a typical application circuit. It can be seen from this circuit that to produce a complete multi-page teletext system requires only three ICs and eight discrete components.

The video signal required is typically 1V (peak to peak) coupled by a 10nF capacitor in series.

The pin-out on the MV1815 has been specially designed to allow the circuit to be constructed easily on a single sided PCB when using either 64K x 1 or 256K x 1 DRAMs. It is required that two DRAMS are always included in the circuit rather than a single large DRAM, as the MV1815 expects to access a two deep memory field.

The reset input must be held low for about 250ms from power up to avoid erroneous clocking. A 1µF capacitor is all that is required.

If the on-chip data slicer is not required, by holding EXT/INT high, an external data stream and sync pulses may be input to the MV1815 on pins SYNC and DATA.

Pin Descriptions

Vdd and Vss (pins 21 & 40 and 1 & 20 respectively).

The 5 ± 0.5 volt supply is applied to any convenient pair of these pins. It is however recommended that all four supply pins are used.

Video input (pin 19).

The video input is connected to this pin coupled via a 10nF capacitor. A video signal between 0.5V and 2.5V peak to peak is required.

BLC (pin 17).

Black level capacitor. A 10nF capacitor connected to ground is required.

WLC (pin 18).

White level capacitor. A 10nF capacitor connected to ground is required.

TCR(pin22)

Time constant resistor. A 10K resistor is required to V_{DD}.

DATA I/O and SYNC I/O (pins 15 and 14 respectively).

The two outputs from the internal data slicer are fed via two tri-state buffers to the inputs of the data acquisition logic circuits. These two pins can be used to inject an external data and sync pulse train into the data acquisition circuits or to use the output of the internal data-slicer, depending on the state of EXT/INT.

EXT/$\overline{\text{INT}}$ (pin 16).

When this pin is held low the data acquisition circuits use the data and sync pulse trains from the internal data slicer. When high it permits external data and sync signals to be fed directly into the data acquisition circuits.

$\overline{\text{XTI}}$ & XTO (pins 3 and 4).

This pair of pins are designed to drive a 27.75000 MHz fundamental or third overtone quartz crystal. If a third overtone type is used, two external components are required to ensure operation at the correct frequency. Typical external components are, a 33nF capacitor and a 1µH. inductor in series and in parallel with the crystal. A 1MΩ resistor is included on chip between XTI and XTO to bias the input to its correct operating region. The crystal should be within ± 100 p.p.m. of the nominal frequency over the operating temperature range.

XCK (pin 4).

This pin is a clock output running at 13.875 MHz. It can be used as a stable clock for other components.

A0-A9(pins 34, 36, 35, 8, 7, 6, 9, 5, 12, 29 respectively).

DRAM address lines.

D0 (pin 11).

DRAM data line to bank 0

D1 (pin 10).

DRAM data line to bank 1

$\overline{\text{CAS}}$ (pin31).

DRAM column address strobe

$\overline{\text{RAS}}$ (pin 33).

DRAM row address strobe

$\overline{\text{WR}}$ (pin 32).

DRAM read/not write signal

TEST(pin 30).

This pin is used for internal testing and should be held low for the normal operation of the chip.

$\overline{\text{EVENT}}$ (pin 39).

An active low open drain output intended to interrupt a microprocessor when an important event occurs on either data acquisition circuit. The EVENT/A /B register bits uniquely describe which type of event has occured.

CSO OUT, BLUE, GREEN RED, BLANK (pins 28, 26,25,24,23).

These pins are high power RGB outputs allowing direct connection to display circuits without further buffering.

Y (pin 27).
This pin is a logical OR of the R.G.B. ouputs

SCL & SDA (pins 37 & 38 respectively)
Standard connection to I²C bus. The MV1815 can work at frequencies to a maximum of 1 MHz.

$\overline{\text{RESET}}$ (pin 13).
The active low reset input. This input has a nominal 150 KΩ resistor coupled to V_{DD} and a schmitt input buffer, allowing a simple external circuit consisting of a 1µF capacitor to ground to perform a power - on reset pulse of sufficient duration to allow the crystal oscillator to stabilize. When held low this input resets all registers to default setting and initalises counters.

MV1815 REGISTER ACCESSING VIA I²C

The MV1815 has twelve read registers and nineteen write registers. The I²C - bus slave address is "001001W/R".

When the MV1815 is addressed on the I²C bus as a slave transmitter, i.e. the eighth data bit is high, it will acknowledge the address byte, then transmit the contents of register address #0 to #10 in numerical order, if the master receiver continues to issue clock and acknowledge pulses. After transmitting register 10 contents, the register address will be set to #17, the RAM data register. The contents of RAM will be transmitted from the starting address set in the memory address registers. Each further transmitted byte increments the memory address by one, rather than the register address.

When addressed as a slave receiver, i.e. the eighth data bit is low, the MV1815 will acknowledge the address byte. The first data byte received by the MV1815 sets the register address counter. This defines the address of the register that will be written to by the following byte. Subsequent transmitted bytes will increment the register address by one each time, and the data will thus be written to all numerically higher registers, until the address reaches #17, the RAM data register. All subsequent received bytes will increment the memory address by one and be written to RAM. Whenever a stop condition occurs while the MV1815 is addressed as either a receiver or transmitter, the register address counter will be reset to zero.

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READ REGISTERS

EVENT A/B - Event Registers (register numbers 0 & 1).

These are interrupt registers, designed to quickly notify the controlling microprocessor about the major acquisition events, so that the microprocessor is relieved of the task of polling memory for information regarding the reception of data. The EVENT output is set low when any one of six major events occurs in either of the acquisition circuits. Multiple events will set multiple bits in the registers, which will be cleared when the appropriate registers have been read, as will the EVENT output.

The events that are notified using this register are:- New page received, Valid header received, receipt of non-display packets and control bits C8 and C10, though these bits do not set the EVENT output.

CBITS A/B - Control Bit Registers (register numbers 2 & 6).

These registers display the remaining eight control bits, C5, C6, C7, C9, C11, C12, C13 and C14 received in the last valid header for each acquisition circuit.

PGR 1/2/3 A/B - Page Received Registers. (register numbers 3,4,5,7,8 & 9).

These registers show the exact page number and sub code of the received page.

HAMMC - Hamming Correction Counter. (register number 10).

To aid correct tuning of the receiver, each Hamming protected character received with other than exactly correct Hamming protection, will increment this counter. Thus by regularly reading this count, and monitoring its rate of increase, a good indication is given of the signal quality.

RDATA - RAM Contents Register. (register number 17).

RD7 to RD0 - The video RAM data at the address set by HADD and LADD registers, can be read from this register.

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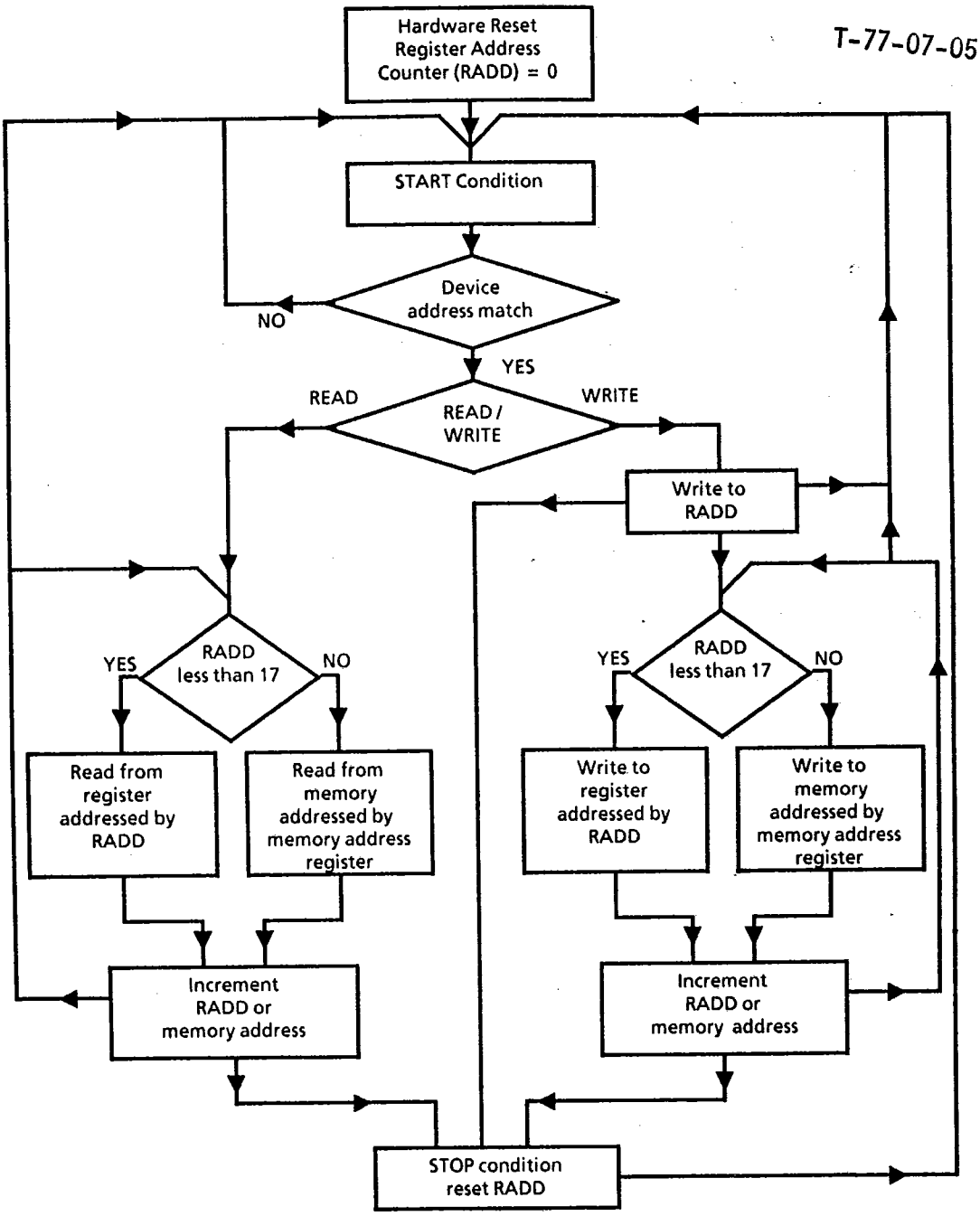

Figure 4. Memory addressing using I²C bus

WRITE REGISTERS

RADD - Register Address Counter.

The first data byte transmitted in any write sequence is the address of the first register to be written to, (see figure 4). Bits 0 to 4 define the register address. An Auto Increment Inhibit bit, disables the auto incrementing of the register or RAM address. The other two bits set the quadrant in which the memory address registers work.

ACON A/B - Acquisition control registers for A and B acquisition circuits (register numbers 1 & 5)

These two registers control the acquisition of data. They control which acquisition circuits are on and which of the magazine, page number or sub-code digits are of "don't care" status during reception of Teletext.

STOR A/B - Acquisition Store Select Registers (register numbers 1 & 6).

The eight bits in each register select which of the 254 page stores will be written to by each acquisition circuit The controlling microprocessor must ensure that the two registers are not written with the same value.

PGS A/B - Page Select Registers (register numbers 2,3,4,7,8 and 9)

These registers define the magazine, page and sub-page that each acquisition circuit will search for, depending on the information set in the ACON registers.

RECON - Receive Control Register (register number 10).

This register controls the data format of the teletext being received including the:-

- Writing of Packet 0 to memory;
- Writing of Packet 24 to memory;
- Writing of Packet 25 to memory;
- Parity check enable;
- Accuracy of the framing code;
- Full field or normal teletext data;
- Rolling headers.

DISCON 1,2,3,4 - Display control registers (register numbers 11,12,13 and 14)

These four registers control the actual display of the teletext and picture. The features controlled include :-

- Which acquisition circuit is displayed;
- Language displayed;
- Control of the display of the header;
- Display of TEXT, PICTURE, or MIX;
- Display of boxes of either text or picture;
- Reveal of text hidden by "conceal" control codes;
- Cursor control;
- Control of separated graphics;
- The display of lines 25 and 26;
- Double height display of,
  - Top half of text,
  - Middle half of text,
  - Bottom half of text.

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Double height of any area will be true double height, i.e. giving quad height characters if double height control characters are present. Double height control characters have no effect when on the bottom row of any displayed region.

HADD - High Address Word Register. (register number 15)

A8 to A15 - The high order address bits selecting one of the 256 sections of 256 bytes to be read through the data register.

LADD - Low Address Byte Register (register number 16)

A0 to A7 - The lower order address bits selecting one of 256 bytes in a given section. This register auto-increments after every read or write operation of the DATA registers if the AII bit is low. Auto incrementing of this register from FF to 00 will increment the HADD register, and overflow of HADD increments A16 & A17 in the RADD register.

WDATA - RAM contents Register. (register 17)

The video RAM data at the address set by HADD and LADD registers can be written via this register.

MEMORY ORGANISATION.

The display memory addresses as seen by the microprocessor via the I²C registers 'HADD' and 'LADD' bear little resemblance to the actual memory addresses that are used to store the data in the DRAMs, in conjunction with RAS and CAS strobes. This is of little consequence though to the system designer, unless he wishes to access the display DRAM data directly, which is inadvisable since the MV1815 needs access to the DRAMs during all TV lines.

The data address in HADD and LADD have been arranged as logically and as simply as possible, to allow a processor system easy access to the display (and non-display) data. Irrespective of the size of memory devices used, the lowest 2K (2048 bytes) of DRAM addresses, referred to as Store 0 and Store 1 contain all the non-display packets associated with the pages being acquired by both acquisition circuits. Space is reserved in Store 0 and Store 1 for up to 23 versions of packets X/26, X/27 or X/28. The only restriction is the total number of the three packets. These packets are stored in the same sequence as they are received. Reception of the same page will overwrite the memory space with new packets X/26, X/27 or X/28.

The first byte of rows 1 to 23 inclusive in both Store 0 and Store 1 can be read by the microprocessor to identify which non-display packet is stored in the particular row. This byte is made up of the 3 least significant bits of the packet number and the designation code value. In addition, packet 29's are stored in both stores and the two versions of packet 8/30 are stored, one in each of the two stores.

The lowest 24 bytes of store 0 (address 0000 to 0017 HEX) are allocated as follows. The first eight (0000 - 0007) are never written to by the MV1815 acquisition circuits. They are however read by the display circuits for display as the first eight characters in the top display row of the teletext page. This is normally where the requested page number is shown. There is no fixed format for this however and the MV1815 puts no constraints on what data is written to this part of the screen. When headers are 'rolling', MV1815 does not write any colour control characters to these locations. It is the responsibility of the control software to do this if it is required. It is therefore perfectly feasible to have red, yellow or cyan rolling headers to signify different states if so desired, or of course white, as the headers are actually transmitted. Allowing access to all eight characters allows a system to write e.g. "123-0001", or "432-XXXX", to show the magazine, page number and sub-code selected by the user, not just the page number as with previous systems. This address in store 1 is not used and may be used by the system for other purposes.

Address 0008 - 000F are written by the MV1815 acquisition circuit that is currently selected for display, with the last eight bytes from every header (packet 0) received by the MV1815 (or every header of the relevant parallel magazine). The only exception are 'out of sequence' headers, or if the 'WI0' bit is set, then no data will be written to these eight bytes. The microprocessor may then write them as required with, for instance, the time derived from packet 8/30. These eight bytes are displayed by the MV1815 as the last eight characters on the top display row, irrespective of which store is selected for display. Addresses 0010 - 0017 are used by the MV1815 to output packet 31 at receiver rate.

The display stores, 2 to 15 (63 or 255 if larger DRAMs are used), start at address 0800, the boundaries being in multiples of 1024 bytes, at 0C00, 1000 etc. (HEX). In each store, the first 24 bytes are nos. 14 to 37 inc. from the header for the requested page The further 1000 bytes per store are used by packets 1 though to 25 (40 bytes per packet), in that order, irrespective of the order of the transmission.

TABLE POSITION	ENGLISH	GERMAN	SWEDISH FINNISH	ITALIAN	FRENCH (BELGIAN)	SPANISH	CZECH
2/3	£	#	#	£	é	ç	#
2/4	$	$	¤	$	ï	$	ů
4/0	@	§	É	é	à	¡	č
5/11	←	Ä	Ä	°	ë	á	ť
5/12	½	Ö	Ö	ç	ê	é	ž
5/13	→	Ü	Å	→	ù	í	ý
5/14	↑	^	Ü	^	î	ó	í
5/15	#	_	_	#	#	ú	ř
6/0	—	°	é	ù	è	¿	é
7/11	¼	ä	ä	à	â	ü	á
7/12	‖	ö	ö	ò	ô	ñ	ě
7/13	¾	ü	å	è	û	è	ú
7/14	÷	ß	ü	ì	ç	à	š

Table 2. International Character set

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ROW	0	1	COLUMN (bits 5,6, 7 & 8) 2	3	4	5	6	7
0	Alpha Black	Graphic Black		0	@	P	—	p
1	Alpha Red	Graphics Red	!	1	A	Q	a	q
2	Alpha Green	Graphics Green	"	2	B	R	b	r
3	Alpha Yellow	Graphics Yellow	£	3	C	S	c	s
4	Alpha Blue	Graphics Blue	$	4	D	T	d	t
5	Alpha Magenta	Graphics Magenta	%	5	E	U	e	u
6	Alpha Cyan	Graphics Cyan	&	6	F	V	f	v
7	Alpha White	Graphics White	'	7	G	W	g	w
8	Flash	Conceal Display	(	8	H	X	h	x
9	Steady	Contiguous Graphics	)	9	I	Y	i	y
10	End Box	Separate Graphics	*	:	J	Z	j	z
11	Start Box	No action	+	;	K	←	k	¼
12	Normal Height	Black Background	,	<	L	½	l	‖
13	Double Height	New Background	-	=	M	→	m	¾
14	No action	Hold Graphics	.	>	N	↑	n	÷
15	No action	Release Graphics	/	?	O	#	o	

Table 3. Control Characters, Primary Character Set G0 and Mosaic Graphics Set G1

TIMING CHARACTERISTICS

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Test conditions (unless otherwise stated)
T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

Characteristic		Value			Units	Conditions
		Min	Typ	Max		
SCL Clock frequency	f_{SCL}	0	100	1000	kHz	
Time the bus must be free before a new transision can start	t_{BUF}	4.7			µs	
Hold time start condition.After this periodthe first clock pulse is generated	$t_{HD;STA}$	4.0			µs	
Low period of clock	t_{LOW}	470			ns	All values refer to V_{IH} and V_{IL} levels
High period of clock	t_{HIGH}	400			ns	
Set up time DATA	$t_{SU;DAT}$	25			ns	
Rise time of SDA and SCL signals	t_R			1	µs	
Fall time of SDA and SCL signals	t_F			300	ns	
Set up time for STOP condition	$t_{SU;STO}$	4			µs	

Table 4 I²C Parameters

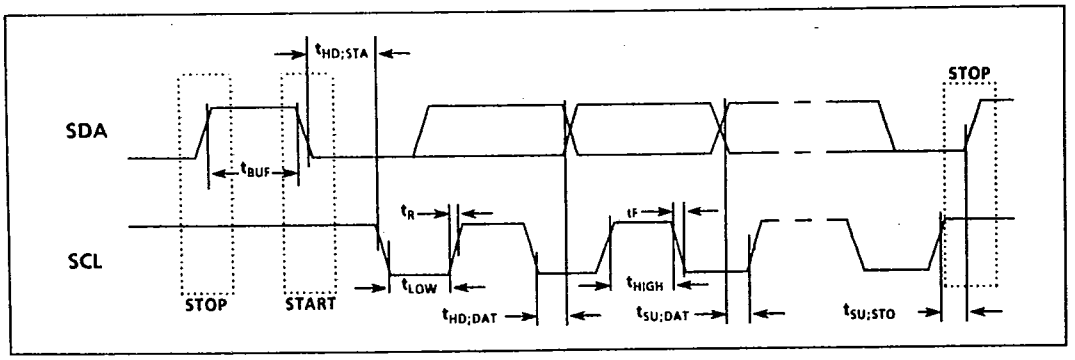

Figure 5 I²C bus timing diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated)
T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

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Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
All Inputs (except XTI and TEST)						All inputs have 150KΩ pull-up resistor to V_{DD} except test
Input low current (source)		-10	-33	-100	µA	
Input high current (sink)				10	µA	
XTI and TEST inputs	3					
Input low current (source)	30			-10	µA	
Input high current (sink)				+10	µA	
SYNC and DATA inputs	14,15					
Input low voltage		-0.3		0.8	V	
Input high voltage		2.0		5.3	V	$V_{IH_{MAX}} = V_{DD} + 0.3V$
RESET, SDA, SCL input (Schmitt input)	13					
Input low voltage	38	-0.3		1.0	V	
Input high voltage	37	2.0		5.3	V	$V_{IH_{MAX}} = V_{DD} + 0.3V$
Threshold voltage (rising)			1.85		V	$V_{DD} = 5V$
(falling)			1.05		V	$V_{DD} = 5V$
All other inputs						
Input low voltage		-0.3		1.5	V	
Input high voltage		3.5		5.3	V	$V_{IH_{MAX}} = V_{dd} + 0.3V$
Outputs (A0 to A9,D0, D1, WE,CAS,RAS,EVENT)						
Output low (sink)		13	26		mA	$V_{OL} = 0.4V$
Output high (source)		21	45		mA	$V_{OH} = 2.4V$
XCK	4					
Output low(sink)		6.9	13		mA	$V_{OL} = 0.4V$
Output high(source)		10	22		mA	$V_{OH} = 2.4V$
Frequency			13.875		MHz	
XTO	2,					
Output low (sink)		6.9	13		mA	$V_{OL} = 0.4V$
(source)		10	22		mA	
Max Input Frequency, $F_{IN_{MAX}}$	3		27.75		MHz	

Table 5

ELECTRICAL CHARACTERISTICS

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Test conditions (unless otherwise stated)
T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

Characteristic	Pin	Value			Units	Conditions
		Min	Typ	Max		
R, G, B & Blanking outputs	23,24					
I_{OL}	25,26	23	43		mA	
I_{OH}	27	36	76		mA	V_{OL} = 0.4V
Composite sync I_{OL}		13	26		mA	V_{OH} = 2.4V
output I_{OH}	28	21	45		mA	
Video Input pin Input voltage	19	0.5		2.5	V	peak to peak
Operating temperature		0		70	°C	
Storage temperature		-65		150	°C	
Relative Humidity				85	%	
Absolute Max DC supply	21	-0.3		7.0	V	
	40					

Table 6

TIMING CHARACTERISTICS of DRAMS

Test conditions (unless otherwise stated)
T_{amb} = 0°C to 70°C, V_{DD} = +5V ±0.5V

Characteristic		Value			Units	Conditions
		Min	Typ	Max		
Access time from RAS	t_{RAC}			232	nS	DRAM timing
Access time from CAS	t_{CAC}			124	nS	characteristics required
RAS Precharge Time	t_{RP}			144	nS	by the MV1815
RAS Pulse Width	t_{RAS}			432	nS	
CAS Pulse Width	t_{CAS}			144	nS	
Row Address Hold Time	t_{RAH}			36	nS	
Column Address Hold Time	t_{CAH}	72			nS	
Data-inSet Time	t_{DS}	36			nS	
Data-in Hold Time	t_{DH}	72			nS	
	t_{CP}	108			nS	
	t_{PC}	252			nS	
Ramdon R/W Cycle Time	t_{RC}	576			nS	

Table 7 DRAM Parameters

For more information about all Zarlink products
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TECHNICAL DOCUMENTATION - NOT FOR RESALE