July 2014

FAN53540
2.4 MHz, 5 A TinyBuck™ Synchronous Buck Regulator

Features

- 2.4 MHz Fixed-Frequency Operation
- Best-in-Class Load Transient Response
- 5 A Output Current Capability
- 2.7 V to 5.5 V Input Voltage Range
- Adjustable Output Voltage: 0.8V to 90% of V_{IN}
- PFM Mode for High Efficiency in Light Load (Forced PWM Available on MODE Pin)
- 50 µA Typical Quiescent Current in PFM Mode
- External Frequency Synchronization
- Low Ripple Light-Load PFM Mode with Forced PWM Control
- Power Good Output
- Internal Soft-Start
- Input Under-Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- No External Compensation Required
- 20-Bump WLCSP

Applications

- Set-Top Box
- Hard Disk Drive
- Communications Cards
- DSP Power

Description

The FAN53540 is a step-down switching voltage regulator that delivers an adjustable output from an input voltage supply of 2.7 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53540 is capable of delivering 5 A at over 90% efficiency, while maintaining a very high efficiency of over 80% at load currents as low as 2 mA. The regulator operates at a nominal fixed frequency of 2.4 MHz, which reduces the value of the external components to 470 nH for the output inductor and 20 µF for the output capacitor. Additional output capacitance can be added to improve regulation during load transients without affecting stability and inductance up to 1.2 µH may be used with additional output capacitance.

At moderate and light loads, pulse frequency modulation (PFM) is used to operate the device in power-save mode with a typical quiescent current of 50 µA. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed-frequency control, operating at 2.4 MHz. In shutdown mode, the supply current drops below 1 µA, reducing power consumption. PFM mode can be disabled if constant frequency is desired. The FAN53540 is available in a 20-bump 1.96 mm x 1.56 mm Wafer-Level Chip-Scale Package (WLCSP).

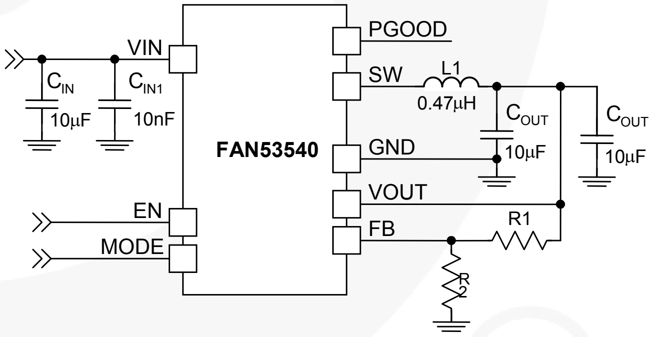


Figure 1. Typical Application

Ordering Information

Part Number	Temperature Range	Package	Packing Method
FAN53540UCX	-40 to 85°C	20-Ball Wafer-Level, Chip-Scale Package (WLCSP), 4x5 Array, 0.4 mm Pitch, 250µm Ball	Tape and Reel

Recommended External Components

Table 1. Recommended External Components for 5 A Maximum Load Current

Component	Description	Vendor	Parameter	Typical	Unit
L1	470 nH Nominal	*See Table 2*	L	0.47	µH
C_{OUT}	10 µF, 6.3 V, X5R, 0805, 2 Pieces	GRM21BR60J106M (Murata) C2012X5R0J106M (TDK)	C	10	µF
C_{IN}	10 µF, 6.3 V, X5R, 0805				
C_{IN1}	10 nF, 25 V, X7R, 0402	Any	C	10	nF

Table 2. Recommended Inductors

						Component Dimensions	
Manufacturer	**Part#**	**L (nH)**	**DCR (mΩ)**	**I_{MAXDC}(1)**	**L**	**W**	**H**
Bourns	SRP5012-R47M	470	19	6.0	5.1	4.5	1.2
Bourns	SRP4012-R47M	470	20	5.5	4.6	4.0	1.2
Coilcraft	XPL4020-471ML	470	19	7.2	4.2	4.2	2.0
Inter-Technical(2)	SC2511-R47M	470	2.6	16.0	6.5	6.5	3.0
TDK	VLC5020T-R47M	470	15	5.4	5.0	5.0	2.0
Vishay	IHLP1616ABERR47M01	470	20	5.0	4.5	4.1	1.2

Notes:
1. I_{MAXDC} is the lesser current to produce 40°C temperature rise or 30% inductance roll-off.
2. Inductor used for efficiency and temperature rise measurements.

Pin Configuration

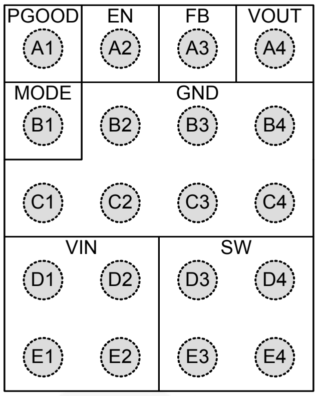


Figure 2. Top View

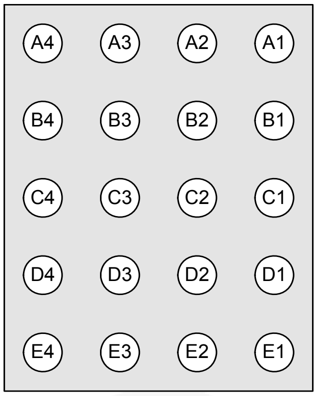


Figure 3. Top View Bottom View

Pin Definitions

Bump #	Name	Description
A1	PGOOD	**Power Good**. This open-drain pin pulls LOW if the output falls out of regulation or is in soft-start.
A2	EN	**Enable**. The device is in Shutdown Mode when this pin is LOW. Do not leave this pin floating. When tying HIGH, use at least a 1 kΩ series resistor if V_{IN} is expected to exceed 4.5 V.
A3	FB	**FB**. Connect to resistor divider. The IC regulates this pin to 0.8 V.
A4	VOUT	**VOUT**. Sense pin for V_{OUT}. Connect directly to C_{OUT}.
B1	MODE	**MODE / SYNC**. A logic 0 allows the IC to automatically switch to PFM during light loads. When held HIGH, the IC to stays in PWM Mode. The regulator also synchronizes its switching frequency to four times (4X) the frequency provided on this pin (f_{MODE}). Do not leave this pin floating. When tying HIGH, use at least a 1 kΩ series resistor if V_{IN} is expected to exceed 4.5 V.
B2, B3, C1 – C4	GND	**Ground**. Low-side MOSFET is referenced to this pin. C_{IN} and C_{OUT} should be returned with a minimal path to these pins.
B4	AGND	**Analog Ground**. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin.
D1, D2, E1, E2	VIN	**Power Input Voltage**. Connect to input power source. Connect to C_{IN} with minimal path.
D3, D4, E3, E4	SW	**Switching Node**. Connect to inductor.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	SW, VIN Pins		-0.3	7.0(3)	V
	Other Pins	Tied without Series Impedance	-0.3	4.5	
		Tied through Series Resistance ≥ 100 Ω	-0.3	V_{IN}	
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2250		V
		Charged Device Model per JESD22-C101	1500		
T_J	Junction Temperature		–40	+150	°C
T_{STG}	Storage Temperature		–65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds			+260	°C

Note:

3. V_{IN} slew rate is limited to 1 V/µs.
4. Lesser of 7 V or V_{IN}+0.3 V.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IN}	Supply Voltage Range	2.7		5.5	V
V_{OUT}	Output Voltage Range	0.8		90% Duty Cycle	V
I_{OUT}	Output Current	0		5	A
L	Inductor		0.47	1.20	µH
C_{IN}	Input Capacitor		10		µF
C_{OUT}	Output Capacitor		20		µF
T_A	Operating Ambient Temperature	-40		+85	°C
T_J	Operating Junction Temperature	-40		+125	°C

Thermal Properties

Symbol	Parameter	Typical	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	38(5)	°C/W

Note:

5. *See Thermal Considerations in the Applications section*.

Electrical Characteristics

Minimum and maximum values are at V_{IN}=2.7 V to 5.5 V, and T_A=-40°C to +85°C, unless otherwise noted. Typical values are at T_A=25°C, V_{IN}=5 V, and V_{OUT}=1.2 V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Power Supplies						
I_Q	Quiescent Current	I_{LOAD}=0, MODE=0 (AUTO PFM/PWM)		50		µA
		I_{LOAD}=0, MODE=1 (Forced PWM)		30		mA
I_{SD}	Shutdown Supply Current	EN=GND		0.1	10.0	µA
V_{UVLO}	Under-Voltage Lockout Threshold	V_{IN} Rising		2.67	2.80	V
		V_{IN} Falling	2.1	2.3		V
V_{UVHYST}	Under-Voltage Lockout Hysteresis			365		mV
Logic Pins						
V_{IH}	High-Level Input Voltage		1.05			V
V_{IL}	Low-Level Input Voltage				0.4	V
V_{LHYST}	Logic Input Hysteresis Voltage			140		mV
I_{IN}	Input Bias Current	Input Tied to GND or 1 kΩ Resistor to VIN		0.01	1.00	µA
I_{OUTL}	PGOOD Pull-Down Current	V_{PGOOD}=0.4 V	1			mA
I_{OUTH}	PGOOD HIGH Leakage Current	V_{PGOOD}=V_{IN}		0.01	1.00	µA
V_{OUT} Regulation						
V_{REF}	Output Reference DC Accuracy, Measured at FB Pin	T_A=25°C, Forced PWM	0.792	0.800	0.808	V
		T_A=-40°C to 85°C, Forced PWM	0.787	0.800	0.813	V
		AUTO PFM/PWM	0.784	0.800	0.824	V
$\frac{\Delta V_{OUT}}{\Delta I_{LOAD}}$	Load Regulation	MODE=V_{IN} (Forced PWM)		–0.02		%/A
$\frac{\Delta V_{OUT}}{\Delta V_{IN}}$	Line Regulation	2.7 V ≤ V_{IN} ≤ 5.5 V, $I_{OUT(DC)}$=1.5 A		-0.16		%/V
I_{REF}	FB Pin Leakage Current	FB=0.8 V		1		nA
ΔV_{OUT}	Transient Response	I_{LOAD} Step 0.1 A to 1.5 A, t_R=100 ns		-30		mV
Power Switch and Protection						
$R_{DS(ON)P}$	P-Channel MOSFET On Resistance			33		mΩ
$R_{DS(ON)N}$	N-Channel MOSFET On Resistance			28		mΩ
I_{LIMPK}	P-MOS Peak Current Limit	Open Loop	5.8	7.5	8.8	A
		Closed Loop		8		A
T_{LIMIT}	Thermal Shutdown			155		°C
T_{HYST}	Thermal Shutdown Hysteresis			20		°C
V_{SDWN}	Input OVP Shutdown	Rising Threshold		6.1		V
		Falling Threshold	5.5	5.8		V
Frequency Control						
f_{SW}	Oscillator Frequency		2.1	2.4	3.0	MHz
f_{MODE}	MODE Pin Synchronization Range	External Square-Wave, 30% to 70% Duty Cycle	525	600	700	kHz
Soft-Start and Output Discharge						
t_{SS}	Regulator Enable to Regulated V_{OUT} (Rising PGOOD)			1.2		ms
R_{DIS}	Output Discharge Resistance	EN=0 V		175		Ω

Typical Characteristics

Unless otherwise specified; V_{IN}=5 V, V_{OUT}=1.2 V, V_{MODE}=0 V, T_A=25°C, circuit in Figure 1, and components per Table 1.

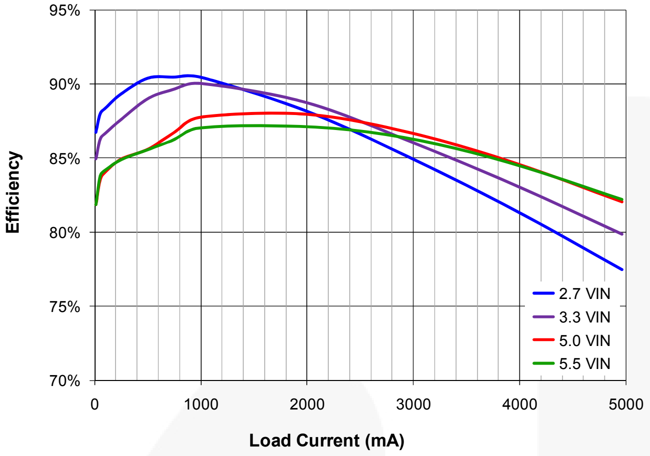


Figure 4. Efficiency vs. I_{LOAD}, 1.2 V_{OUT}

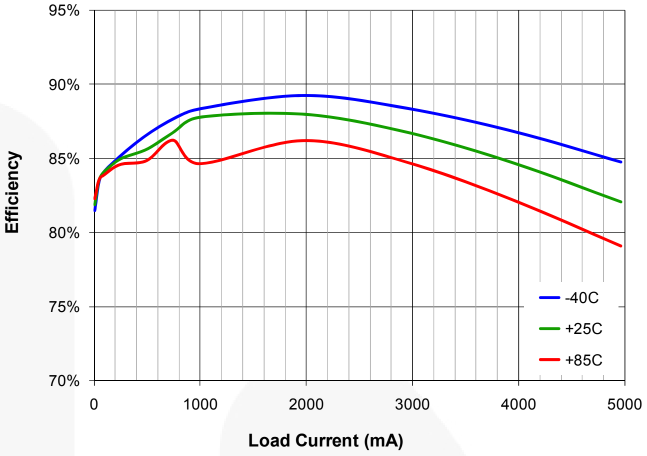


Figure 5. Efficiency vs. I_{LOAD}, 1.2 V_{OUT}

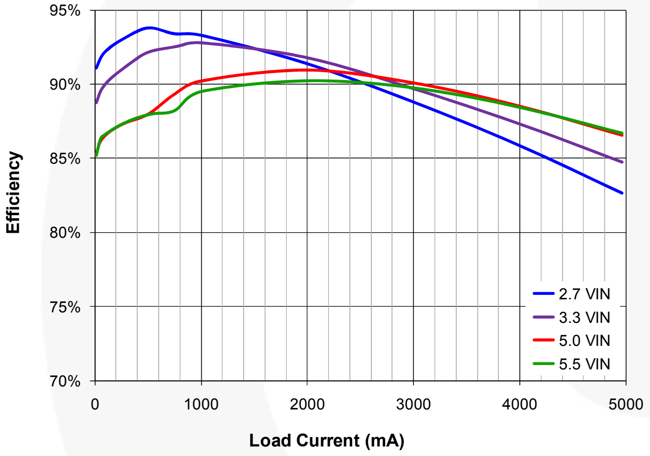


Figure 6. Efficiency vs. I_{LOAD}, 1.8 V_{OUT}

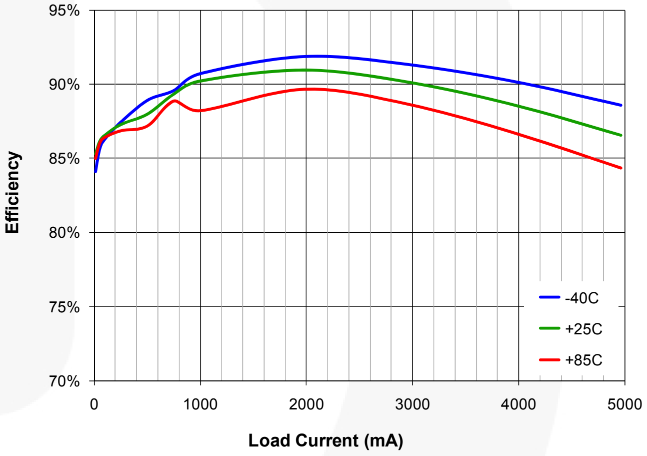


Figure 7. Efficiency vs. I_{LOAD}, 1.8 V_{OUT}

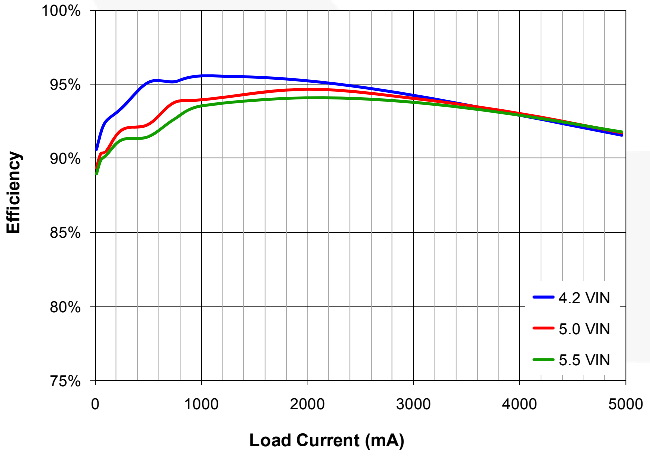


Figure 8. Efficiency vs. I_{LOAD}, 3.3 V_{OUT}

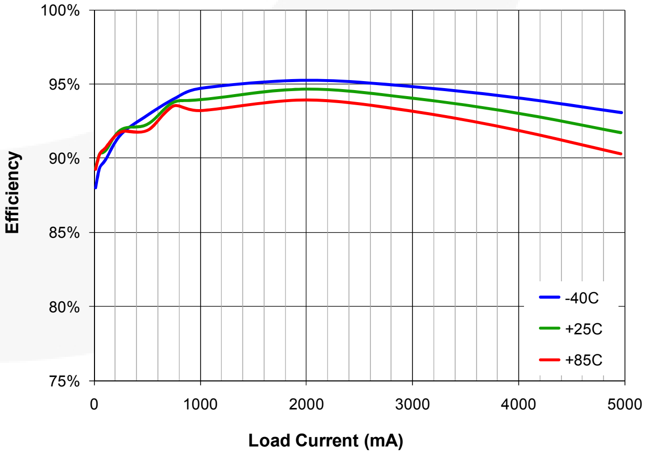


Figure 9. Efficiency vs. I_{LOAD}, 3.3 V_{OUT}

Typical Characteristics

Unless otherwise specified; V_{IN}=5 V, V_{OUT}=1.2 V, V_{MODE}=0 V, T_A=25°C, circuit in Figure 1, and components per Table 1.

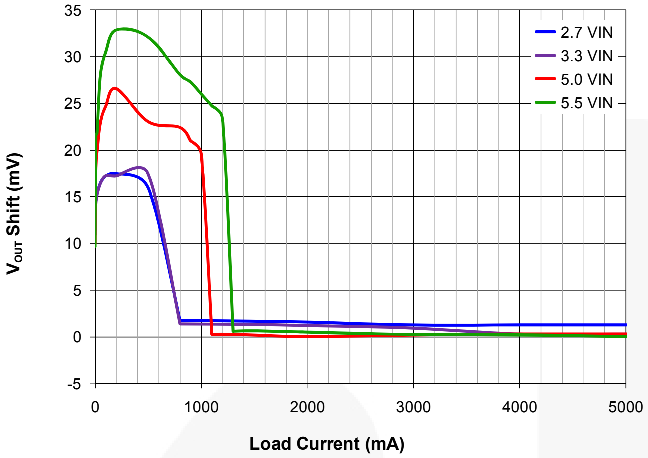


Figure 10. Regulation, 1.2 V_{OUT}

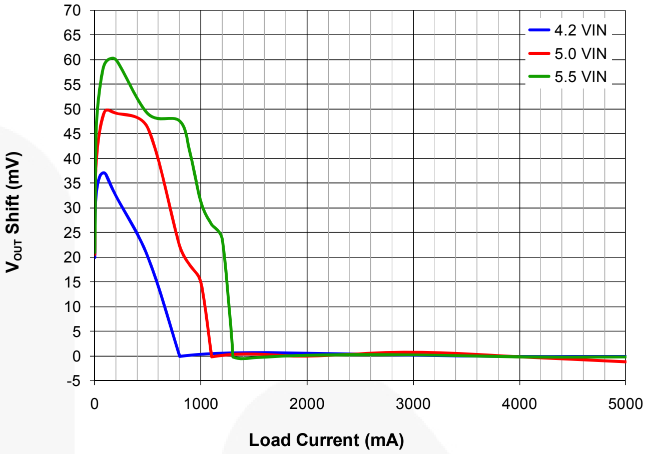


Figure 11. Regulation, 3.3 V_{OUT}

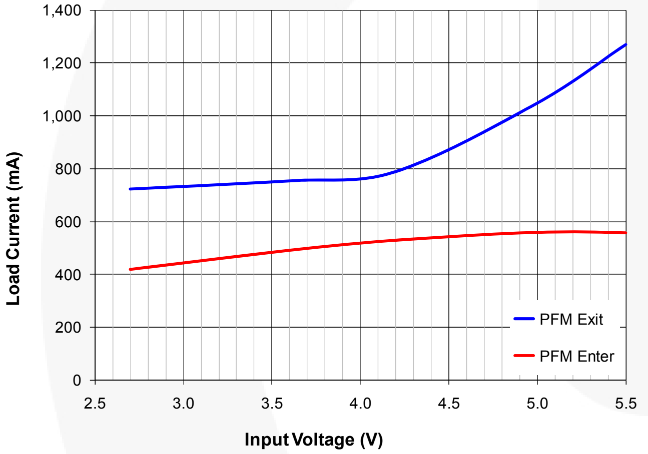


Figure 12. PFM / PWM Boundaries, 1.2 V_{OUT}

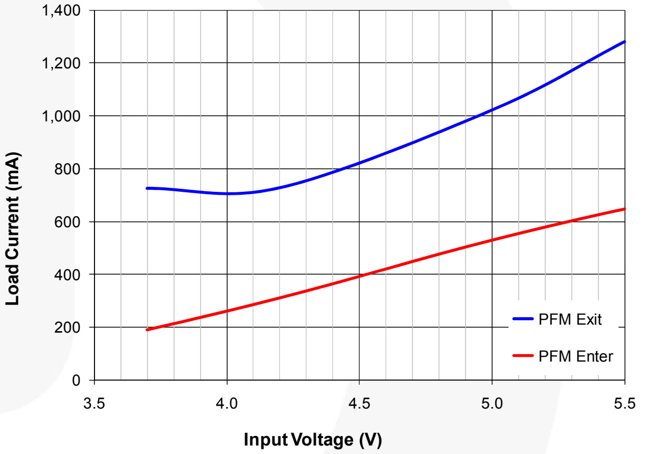


Figure 13. PFM / PWM Boundaries, 3.3 V_{OUT}

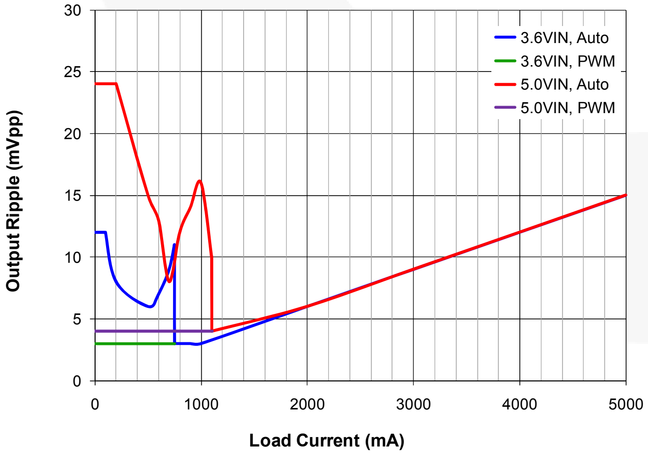


Figure 14. Output Voltage Ripple

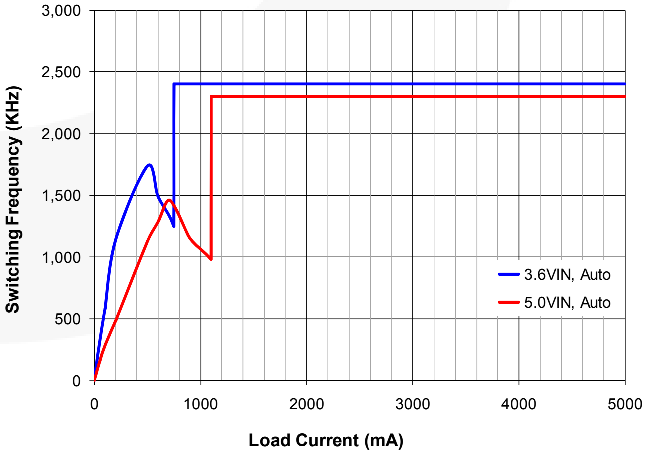


Figure 15. Switching Frequency

Typical Characteristics

Unless otherwise specified; V_{IN}=5 V, V_{OUT}=1.2 V, V_{MODE}=0 V, T_A=25°C, circuit in Figure 1, and components per Table 1.

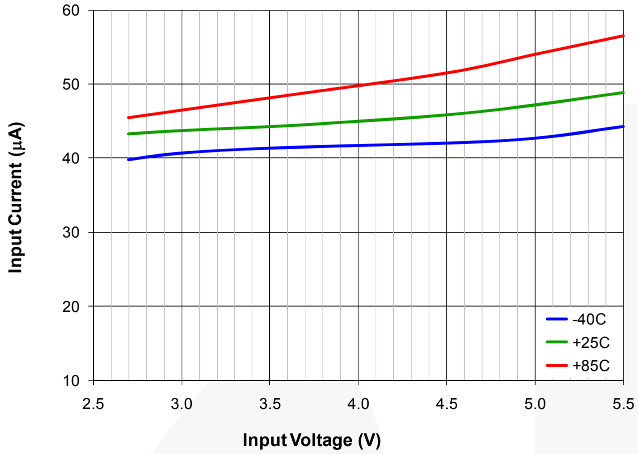


Figure 16. Quiescent Current, Auto Mode, EN=V_{IN}

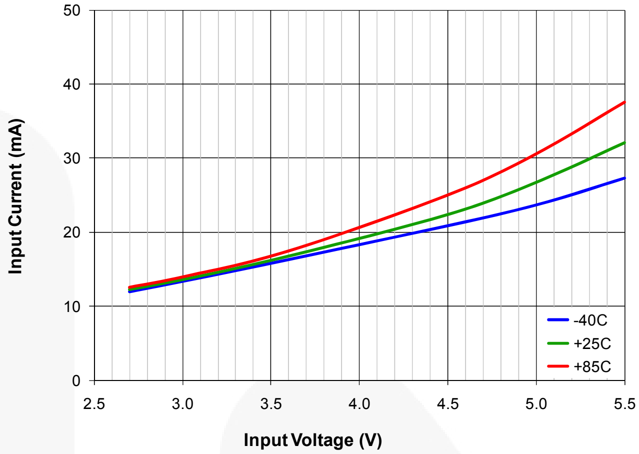


Figure 17. Quiescent Current, PMW Mode, EN=V_{IN}

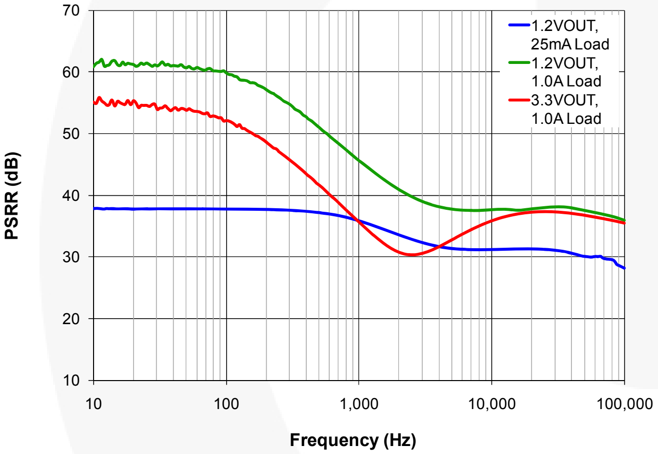


Figure 18. Power Supply Rejection (PSRR)

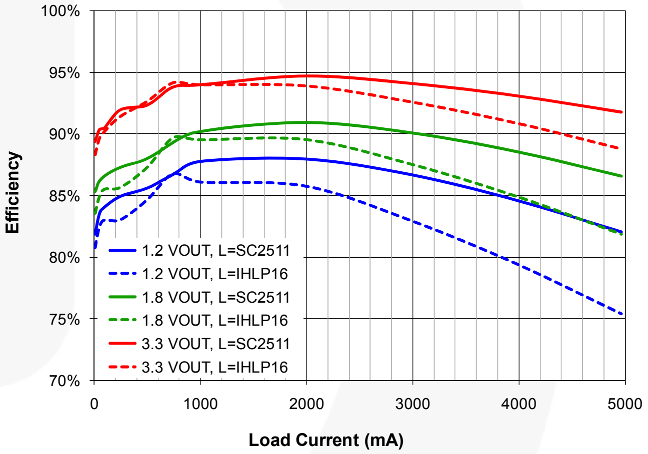


Figure 19. Inductor Efficiency Comparison, 5.0 V_{IN}

Figure 20. Line Transient, 50 Ω Load, t_R=t_F=10 µs

Figure 21. Line Transient, I_{LOAD}=1.0 A, t_R=t_F=10 µs

Typical Characteristics

Unless otherwise specified; V_{IN}=5 V, V_{OUT}=1.2 V, V_{MODE}=0 V, T_A=25°C, circuit in Figure 1, and components per Table 1.

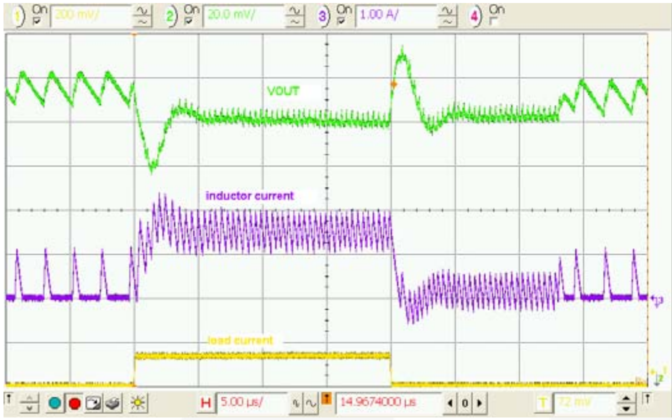


Figure 22. Load Transient, 0.1-1.5 A Load, t_R=t_F=100 ns

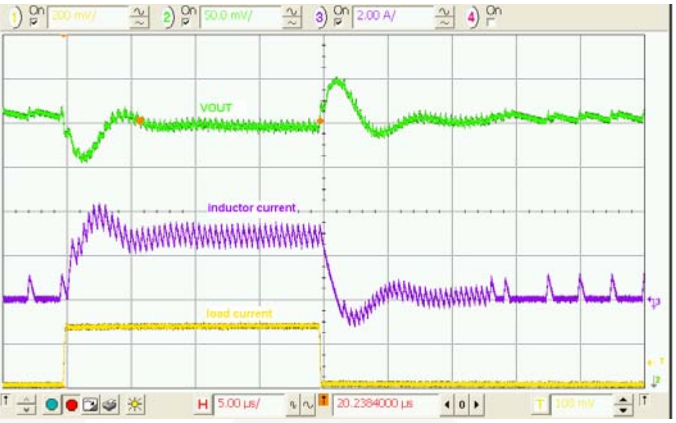


Figure 23. Load Transient, 0.1-3.0 A Load, t_R=t_F=100 ns, C_{OUT}=2x22 µF

Figure 24. Startup / Shutdown, No Load

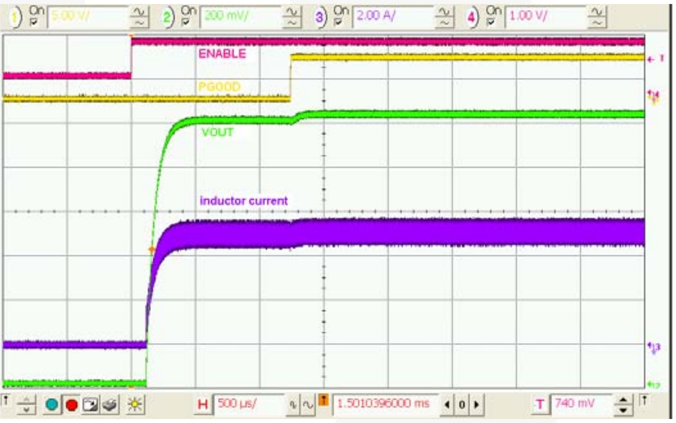


Figure 25. Startup / Shutdown, 240 mΩ Load, C_{OUT}=2x22 µF

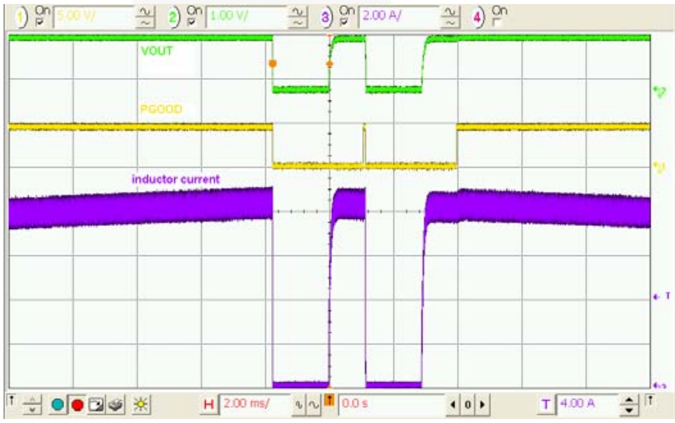


Figure 26. Overload Protection and Recovery

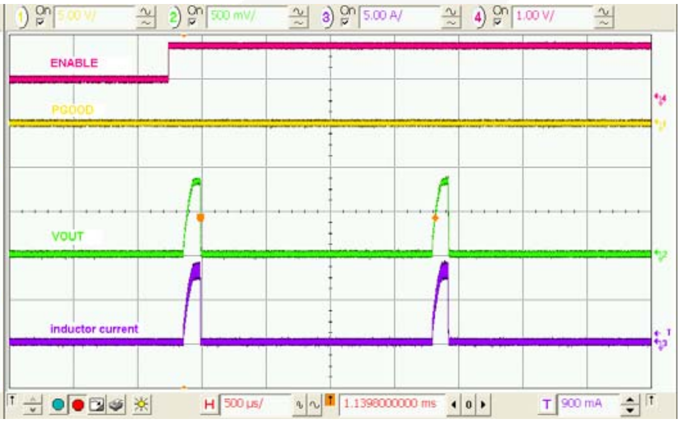


Figure 27. Startup into Overload

Operation Description

The FAN53540 is a step-down switching voltage regulator that delivers an adjustable output from an input voltage supply of 2.7 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53540 is capable of delivering up to 5 A at over 90% efficiency. The regulator operates at a nominal frequency of 2.4 MHz at full load, which reduces the value of the external components to 470 nH for the output inductor and 20 µF for the output capacitor. High efficiency is maintained at light load with single-pulse PFM Mode.

Control Scheme

The FAN53540 uses a proprietary non-linear, fixed-frequency PWM modulator to deliver very fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions.

Regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN53540 operates in Discontinuous Current (DCM) single-pulse PFM Mode, which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is seamless, with a glitch of less than 3% of V_{OUT} during the transition between DCM and CCM Modes.

PFM Mode is disabled by holding the MODE pin HIGH. The IC synchronizes to the MODE pin frequency. When synchronizing to the MODE pin, PFM Mode is disabled.

Setting Output Voltage

The output voltage is set by the R1, R2, and V_{REF} (0.8 V):

$$\frac{R1}{R2} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \tag{1}$$

R1 must be set at or below 100 kΩ; therefore:

$$R2 = \frac{R1 \bullet 0.8}{(V_{OUT} - 0.8)} \tag{2}$$

For example, for V_{OUT}=1.2 V, R1=100 kΩ, R2=200 kΩ.

Enable and Soft-Start

When the EN pin is LOW, the IC is shut down, all internal circuits are off, and the part draws very little current. Raising EN above its threshold voltage activates the part and starts the soft-start cycle. During soft-start, the modulator's internal reference is ramped slowly to minimize surge currents on the input and prevents overshoot of the output voltage.

If large values of output capacitance are used, the regulator may fail to start. If V_{OUT} fails to achieve regulation within 1.2 ms from the beginning of soft-start, the regulator shuts down and waits 1.6 ms before attempting a restart. If the regulator is in current limit for 16 consecutive PWM cycles, the regulator shuts down before restarting 1.6 ms later. This limits the C_{OUT} capacitance when a heavy load ($I_{LOAD(SS)}$) is applied during the startup.

The maximum C_{OUT} capacitance for successful starting with a heavy constant-current load is approximately:

$$C_{OUT\,MAX} \approx (5.8 - I_{LOAD}) \bullet \frac{800}{V_{OUT}} \tag{3}$$

where C_{OUTMAX} is expressed in µF and I_{LOAD} is the load current during soft-start, expressed in A.

Diode Emulation Mode is employed during soft-start, allowing the IC to start into a pre-charged output. Diode emulation prohibits reverse inductor current from flowing through the synchronous rectifier.

When EN is LOW, a 150 Ω resistor discharges V_{OUT}.

Under-Voltage Lockout (UVLO)

When EN is HIGH, the under-voltage lockout keeps the part from operating until the input supply voltage rises high enough to operate properly. This ensures no misbehavior of the regulator during startup or shutdown.

Input Over-Voltage Protection (OVP)

When V_{IN} exceeds V_{SDWN} (about 6.1 V), the IC stops switching to protect the circuitry from excessive internal voltage spikes. An internal filter prevents the circuit from shutting down due to V_{IN} noise spikes.

Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high-side switch. Upon reaching this point, the high-side switch turns off, preventing high currents from causing damage. 16 consecutive PWM cycles in current limit cause the regulator to shut down and stay off for about 1.6 ms before attempting a restart.

In the event of a short circuit, the soft-start circuit attempts to restart and produces an over-current fault after 16 consecutive cycles in current limit, which results in a duty cycle of less than 5%, providing current into a short circuit.

External Frequency Synchronization

Logic 1 on the MODE pin forces the IC to stay in PWM Mode. Logic 0 allows the IC to automatically switch to PFM during light loads. If the MODE pin is toggled, the converter synchronizes its switching frequency to four times the frequency on the mode pin (f_{MODE}).

The MODE pin is internally buffered with a Schmitt trigger, which allows the MODE pin to be driven with slow rise and fall times. An asymmetric duty cycle for frequency synchronization is permitted, provided it is consistent with parametric table limits.

PGOOD Pin

The PGOOD pin is an open-drain that indicates that the IC is in regulation when its state is open. PGOOD pulls LOW under the following conditions:

- The IC has operated in cycle-by-cycle current limit for eight consecutive PWM cycles;
- The circuit is disabled, either after a fault occurs or when EN is LOW; or
- The IC is performing a soft-start.

Thermal Shutdown

When the die temperature increases, due to a high load condition and/or a high ambient temperature, the output switching is disabled until the temperature on the die has fallen sufficiently. The junction temperature at which the thermal shutdown activates is nominally 155°C with a 20°C hysteresis.

Minimum Off-Time Effect on Switching Frequency

$t_{OFF(MIN)}$ is 45 ns, which constrains the maximum V_{OUT}/V_{IN} that the FAN53540 can provide, while still maintaining a fixed switching frequency in PWM Mode. Regulation is maintained even though the regulator is unable to provide sufficient duty-cycle and operate at 2.4 MHz.

Switching frequency is the lower of 2.4 MHz or:

$$f_{SW}(\text{MHz}) = 22.2 \bullet \left(1 - \frac{V_{OUT} + I_{OUT} \bullet R_{OFF}}{V_{IN} + I_{OUT} \bullet (R_{OFF} - R_{ON})}\right) \qquad (4)$$

where:

I_{OUT} = load current, in A;

$R_{ON} = R_{DS(ON)\_P} + DCR_L$, in Ohms; and

$R_{OFF} = R_{DS(ON)\_N} + DCR_L$, in Ohms.

A result of ≤ 0 MHz indicates 100% duty cycle operation.

Application Information

Selecting the Inductor

The output inductor must meet both the required inductance and the energy handling capability of the application. The inductor value affects the average current limit, output voltage ripple, transient response, and efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \bullet \left(\frac{V_{IN} - V_{OUT}}{L \bullet f_{SW}}\right) \qquad (5)$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current as:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \qquad (6)$$

The FAN53540 is optimized for operation with L=470 nH, but is stable with inductances up to 1.2 µH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so lowers the amount of DC current the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do core and skin-effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}{}^2 + \frac{\Delta I^2}{12}} \qquad (7)$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs as well as the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

Table 3 shows the effects on regulator performance of higher inductance than the recommended 470 nH.

Table 3. Inductor Value and Regulator Performance

$I_{MAX(LOAD)}$	ΔV_{OUT} (EQ. 8)	Transient Response
Increase	Decrease	Degraded

Inductor Current Rating

The FAN53540's current-limit circuit can allow a peak current of about 8.8 A to flow through L1 under worst-case conditions. If it is possible for the load to draw that much continuous current, the inductor should be capable of sustaining that current or failing in a safe manner.

For space-constrained applications, a lower current rating for L1 can be used. The FAN53540 may still protect these inductors in the event of a short circuit, but may not be able to protect the inductor from failure if the load is able to draw higher currents than the DC rating of the inductor.

Output Capacitor and V_{OUT} Ripple

Table 1 suggests 0805 capacitors, but 0603 capacitors may be used if space is at a premium. Due to voltage effects, the 0603 capacitors have a lower in-circuit capacitance, which can degrade transient response and output ripple.

Increasing C_{OUT} has a negligible effect on loop stability and can be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, ΔV_{OUT}, is:

$$\Delta V_{OUT} = \Delta I \bullet \left(\frac{1}{8 \bullet C_{OUT} \bullet f_{SW}} + ESR \right) \tag{8}$$

where C_{OUT} is the effective output capacitance. The capacitance of C_{OUT} decreases at higher output voltages, which results in higher ΔV_{OUT}. If large values are used for C_{OUT}, the regulator may fail to start under load. If an inductor value greater than 1.0 μH is used, at least 30 μF of C_{OUT} should be used to ensure transient response performance.

The lowest ΔV_{OUT} is obtained when the IC is in PWM Mode and, therefore, operating at 2.4 MHz. In PFM Mode, f_{SW} is reduced, causing ΔV_{OUT} to increase.

ESL Effects

The Equivalent Series Inductance (ESL) of the output capacitor network should be kept low to minimize the square-wave component of output ripple that results from the division ratio C_{OUT} ESL and the output inductor (L_{OUT}). The square-wave component due to the ESL can be estimated as:

$$\Delta V_{OUT(SQ)} \approx V_{IN} \bullet \frac{ESL_{COUT}}{L1} \tag{9}$$

A good practice to minimize this ripple is to use multiple output capacitors to achieve the desired C_{OUT} value. For example, to obtain C_{OUT}=20 μF, a single 22 μF 0805 would produce twice the square wave ripple of two 10 μF 0805.

To minimize ESL, try to use capacitors with the lowest ratio of length to width. 0805s have lower ESL than 1206 s. If very low output ripple is necessary, research vendors that produce 0508 or 0612 capacitors with ultra-low ESL. Placing additional small value capacitors near the load also reduces the high-frequency ripple components.

Input Capacitor

The 10 μF ceramic input capacitor should be placed as close as possible between the VIN pin and PGND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional "bulk" capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce under-damped ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective C_{IN} capacitance value decreases as V_{IN} increases due to DC bias effects. This has no significant impact on regulator performance.

To reduce ringing and overshoot on VIN and SW, an additional bypass capacitor C_{IN1} is recommended. Because this lower value capacitor has a higher resonant frequency than C_{IN}; C_{IN1} should be placed closer to the VIN and GND pins of the IC than C_{IN}.

Layout Recommendations

The layout example below illustrates the recommended component placement and top copper (green) routing. The inductor in this example is the TDK VLC5020T-R47N.

To minimize VIN and SW spikes and thereby reduce voltage stress on the IC's power switches, it is critical to minimize the loop length for the VIN bypass capacitors.

Switching current paths through C_{IN} and C_{OUT} should be returned directly to the GND bumps of the IC on the top layer of the printed circuit board (PCB). VOUT and GND connections to the system power and ground planes can be made through multiple vias placed as close as possible to the C_{OUT} capacitors. The regulator should be placed as close to its load as possible to minimize trace inductance and capacitance.

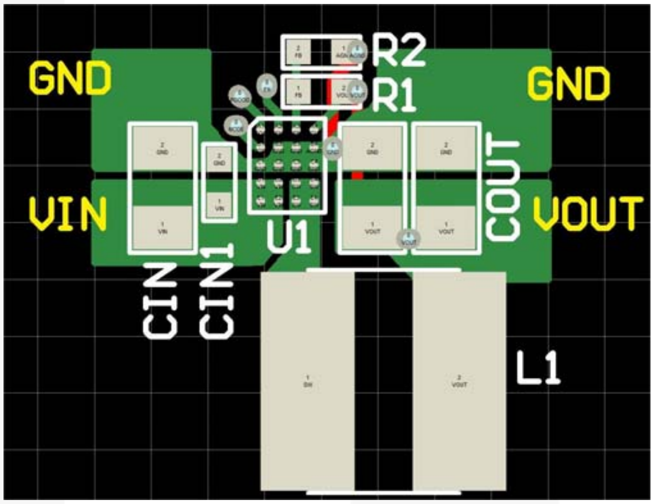


Figure 28. Recommended Layout

Connect the VOUT pin and R1 directly to C_{OUT} using a low impedance path (shown in red in Figure 28. Recommended Layout). A $\geq$0.4 mm wide trace is recommended. Avoid routing this trace directly beneath SW unless separated by an internal GND plane.

If the MODE function is not required, extend the ground plane through the MODE pin to reduce the loop inductance for the VIN bypass.

Thermal Considerations

Heat is removed from the IC through the solder bumps to the PCB copper. The junction-to-ambient thermal resistance (θ_{JA}) is largely a function of the PCB layout (size, copper weight, and trace width) and the temperature rise from junction to ambient (ΔT).

For the FAN53540UC, θ_{JA} is 38°C/W when mounted on its four-layer evaluation board in still air, with 2 oz. outer layer copper weight and 1 oz. inner layers. Halving the copper thickness results in an increased θ_{JA} of 48°C/W.

For long term reliable operation, the IC's junction temperature (T_J) should be maintained below 125°C.

Maximum IC power loss is 2.88 W. Figure 29 shows required power dissipation and derating for a FAN53540UC mounted on the Fairchild evaluation board in still air (38°C/W).

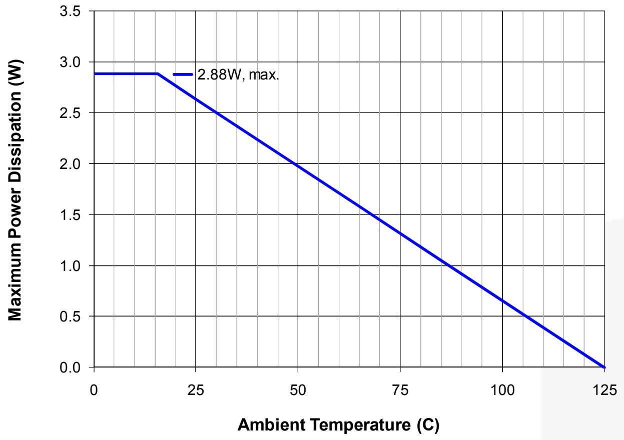


Figure 29. Power Derating

To calculate maximum operating temperature ($\leq$125°C) for a specific application:

1. Use efficiency graphs to determine efficiency for the desired V_{IN}, V_{OUT}, and load condition
2. Calculate IC power dissipation using:

$$P_{IC} = V_{OUT} \bullet I_{LOAD} \bullet \left(\frac{1}{\eta} - 1 \right) \quad (10)$$

   where η is efficiency from Figure 4 through Figure 9.

3. Compute inductor copper losses using:

$$P_L = I_{LOAD}^2 \bullet DCR_L \quad (11)$$

4. Combine IC (step 2) and inductor losses (step 3) to determine total dissipation:

$$P_D = P_{IC} + P_L \quad (12)$$

5. Determine device operating temperature:

$$\Delta T = P_D \bullet R_{\theta JA} \text{ and } T_{IC} = T_{AMB} + \Delta T \quad (13)$$

Device temperature (T_{IC}) should not exceed 125°C.

A different approach, shown here as an example, uses the same equations to determine maximum inductor DCR for a specific application:

If a design requires a 5.0V_{IN}, 1.2 V_{OUT}, 4 A_{RMS}, at 75°C:

A. From Figure 4, η is ~82%.
B. From Eq. 10, P_{IC}=1,054 mW.
C. From Eq. 13, maximum P_D=1,316 mW for 50°C rise.
D. From Eq. 12, P_L=262 mW.
E. From Eq. 11, DCR<16.4 mΩ.

Due to the +0.4%/°C temperature coefficient of copper, inductor DCR must be further reduced to accommodate the ~50°C temperature rise.

To meet the design requirements, an inductor with a room temperature DCR of <13.6 mΩ is necessary.

Figure 30 shows the maximum ambient temperature where FAN53540UC can be used for a continuous load, at 5.0 V_{IN}:

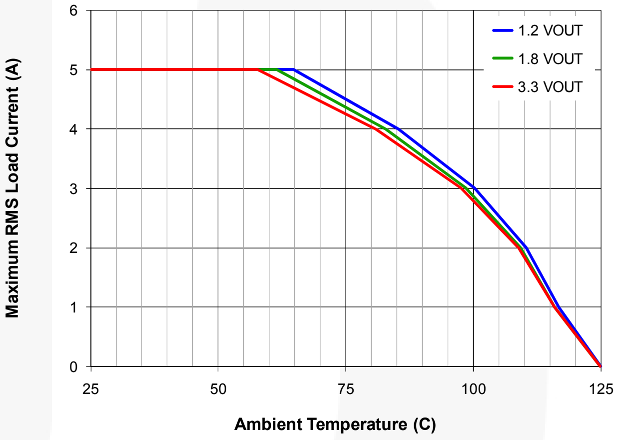
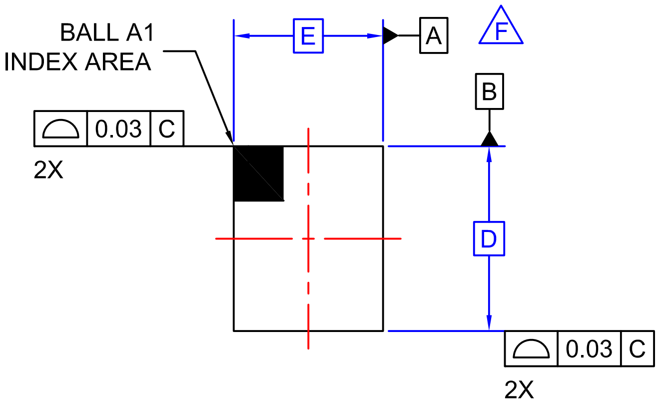


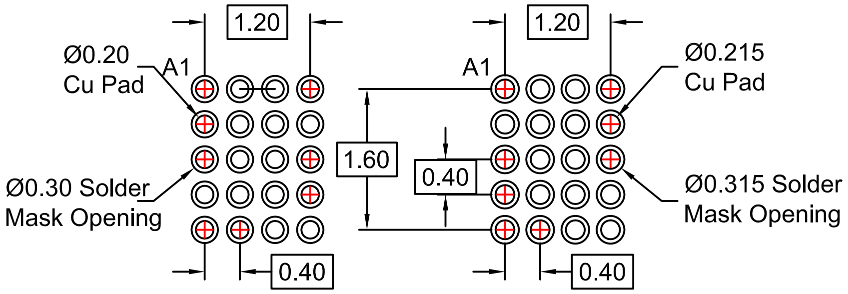
Figure 30. Load Current Derating[6]

Note:

6. The graph was empirically determined using an ultra-low DCR (2.6 mΩ) inductor. For physically smaller devices with higher DCR, further derating may be necessary.



TOP VIEW

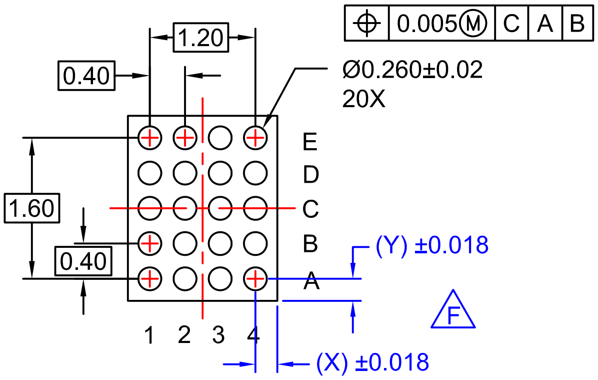


option 1

option 2

RECOMMENDED LAND PATTERN
(NSMD TYPE)

SIDE VIEWS



BOTTOM VIEW

NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE
PER ASMEY14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILNAME: MKT-UC020AArev3.

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