



Integrated Device Technology, Inc.

3.3V CMOS 16-BIT REGISTER (3-STATE)

IDT54/74FCT163374/A/C
IDT54/74FCT163H374/A/C

FEATURES:

- 0.5 MICRON CMOS Technology
- **Typical tsk(o) (Output Skew) < 250ps**
- ESD > 2000V per MIL-STD-883, Method 3015;
> 200V using machine model (C = 200pF, R = 0)
- 25 mil Center SSOP and Cerpack Packages and
19.6 mil pitch TSSOP Package
- Extended commercial range of -40°C to +85°C
- Vcc = 3.3V ±0.3V, Normal Range or
Vcc = 2.7 to 3.6V, Extended Range
- CMOS power levels (10µW typ. static)
- Rail-to-Rail output swing for increased noise margin
- Military product compliant to MIL-STD-883, Class B
- Low Ground Bounce (0.3V typ.)
- Inputs (except I/O) can be driven by 3.3V or 5V
components

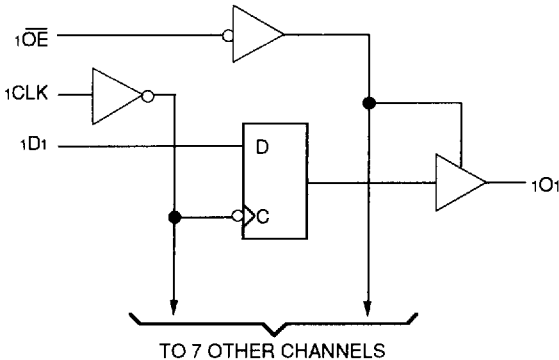
DESCRIPTION:

The IDT54/74FCT163374/A/C 16-bit edge-triggered D-type registers are built using advanced dual metal CMOS technology. These high-speed, low-power registers are ideal for use as buffer registers for data synchronization and storage. The Output Enable (xOE) and clock (xCLK) controls are organized to operate each device as two 8-bit registers or one 16-bit register with common clock. Flow-through organization of signal pins facilitates ease of layout. All inputs are designed with hysteresis for improved noise margin.

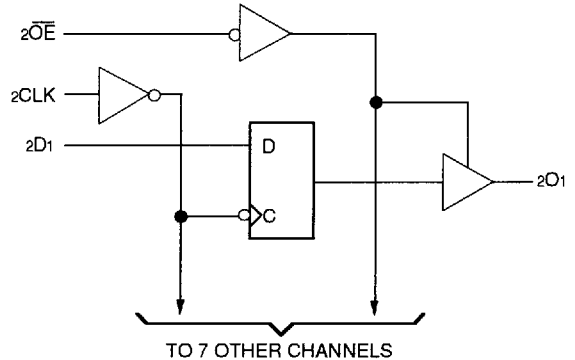
The inputs of IDT54/74FCT163374/A/C can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V supply system.

The IDT54/74FCT163H374/A/C have "Bus Hold" which retains the input's last state whenever the input goes to high impedance. This prevents "floating" inputs and eliminates the need for pull-up/down resistors.

FUNCTIONAL BLOCK DIAGRAM



2775 drw 01



2775 drw 02

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

APRIL 1994

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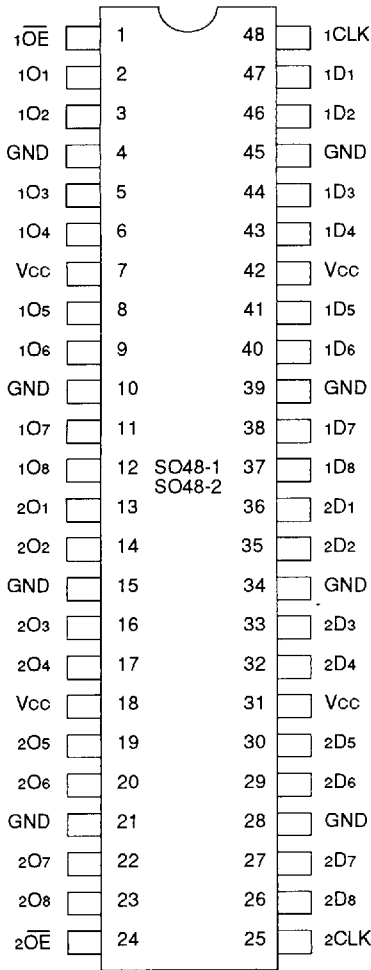
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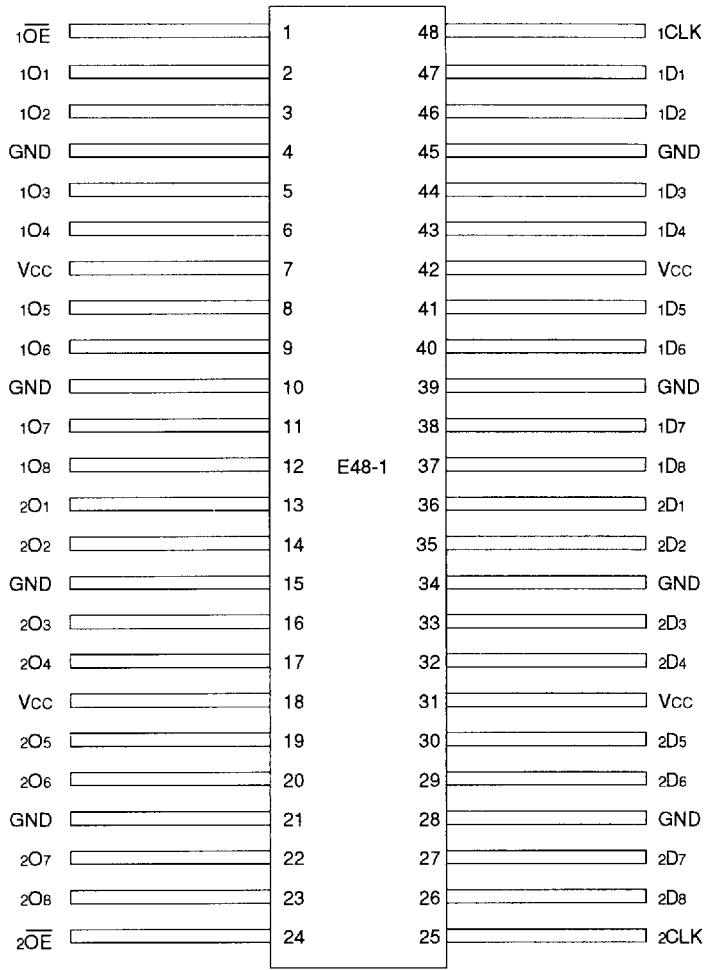
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PIN CONFIGURATIONS



SSOP
TSSOP
TOP VIEW

2775 drw 03



CERPACK
TOP VIEW

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PIN DESCRIPTION

Pin Names	Description
xDx	Data Inputs ⁽¹⁾
xCLK	Clock Inputs
xOx	3-State Outputs.
xOE	3-State Output Enable Input (Active LOW)

2775 tbl 01

NOTE:

- On FCT163H374 these pins have "Bus Hold". All other pins are standard inputs, outputs or I/Os.

FUNCTION TABLE⁽¹⁾

Function	Inputs			Outputs
	xDx	xCLK	xOE	xOx
Hi-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

NOTE:

2775 tbl 02

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance
↑ = LOW-to-HIGH transition

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +4.6	-0.5 to +4.6	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
VTERM ⁽⁴⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc + 0.5	-0.5 to Vcc + 0.5	V
TA	Operating Temperature	-40 to +85	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +150	°C
PT	Power Dissipation	1.0	1.0	W
IOUT	DC Output Current	-60 to +60	-60 to +60	mA

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NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Vcc terminals.
- Input terminals.
- Output and I/O terminals.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	3.5	6.0	pF
COU	Output Capacitance	VOUT = 0V	3.5	8.0	pF

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NOTE:

- This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (STANDARD PARTS)

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, Vcc = 2.7V to 3.6V; Military: TA = -55°C to +125°C, Vcc = 2.7V to 3.6V

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
VIH	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)			2.0	—	Vcc+0.5	
VIL	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
IIH	Input HIGH Current (Input pins) ⁽⁶⁾	Vcc = Max.	VI = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins) ⁽⁶⁾		VI = Vcc	—	—	±1	
IIL	Input LOW Current (Input pins) ⁽⁶⁾		VI = GND	—	—	±1	
	Input LOW Current (I/O pins) ⁽⁶⁾		VI = GND	—	—	±1	
IOZH	High Impedance Output Current (3-State Output pins) ⁽⁶⁾	Vcc = Max.	VO = Vcc	—	—	±1	µA
IOZL			VO = GND	—	—	±1	
VIK	Clamp Diode Voltage	Vcc = Min., IIN = -18mA		—	-0.7	-1.2	V
IODH	Output HIGH Current	Vcc = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		-36	-60	-110	mA
IODL	Output LOW Current	Vcc = 3.3V, VIN = VIH or VIL, VO = 1.5V ⁽³⁾		50	90	200	mA
VOH	Output HIGH Voltage	Vcc = Min. VIN = VIH or VIL	IOH = -0.1mA	Vcc-0.2	—	—	V
			IOH = -3mA	2.4	3.0	—	
		Vcc = 3.0V VIN = VIH or VIL	IOH = -6mA MIL. IOH = -8mA COM'L.	2.4 ⁽⁵⁾	3.0	—	
VOL	Output LOW Voltage	Vcc = Min. VIN = VIH or VIL	IOL = 0.1mA	—	—	0.2	V
			IOL = 16mA	—	0.2	0.4	
			IOL = 24mA	—	0.3	0.5	
Ios	Short Circuit Current ⁽⁴⁾	Vcc = Max., VO = GND ⁽³⁾		-60	-135	-240	mA
VH	Input Hysteresis	—		—	150	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current	Vcc = Max., VIN = GND or Vcc	COM'L.	—	0.1	10	µA
			MIL.	—	0.1	100	

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NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 3.3V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. VOH = Vcc - 0.6V at rated current.
6. The test limit for this parameter is ±5µA at TA = -55°C.



DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (BUS HOLD)

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = -40°C to +85°C, Vcc = 2.7V to 3.6V; Military: TA = -55°C to +125°C, Vcc = 2.7V to 3.6V

Symbol	Parameter		Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
VIH	Input HIGH Level (Input pins)		Guaranteed Logic HIGH Level		2.0	—	5.5	V
	Input HIGH Level (I/O pins)				2.0	—	Vcc+0.5	
VIL	Input LOW Level (Input and I/O pins)		Guaranteed Logic LOW Level		-0.5	—	0.8	V
IIH	Input HIGH Current ⁽⁷⁾	Standard Input ⁽⁶⁾	Vcc = Max.	Vi = Vcc	—	—	±1	µA
		Standard I/O ⁽⁶⁾			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
IIL	Input LOW Current ⁽⁷⁾	Standard Input ⁽⁶⁾	Vcc = Max.	Vi = GND	—	—	±1	µA
		Standard I/O ⁽⁶⁾			—	—	±1	
		Bus Hold Input			—	—	±100	
		Bus Hold I/O			—	—	±100	
IBHH IBHL	Bus Hold Sustain Current ⁽⁷⁾	Bus Hold Input	Vcc = Min.	Vi = 2.0V	-50	—	—	µA
				Vi = 0.8V	+50	—	—	
IBHHO IBHLO	Bus Hold Overdrive Current ⁽⁷⁾	Bus Hold Input	Vcc = Max.	Vi = 1.5V	—	—	TBD	mA
				—	—	—	TBD	
IOZH	High Impedance Output Current		Vcc = Max.	Vo = Vcc	—	—	±1	µA
IOZL	(3-State Output pins) ⁽⁶⁾			Vo = GND	—	—	±1	
VIK	Clamp Diode Voltage		Vcc = Min., IIN = -18mA		—	-0.7	-1.2	V
IDH	Output HIGH Current		Vcc = 3.3V, VIN = VIH or VIL, Vo = 1.5V ⁽³⁾		-36	-60	-110	mA
IODL	Output LOW Current		Vcc = 3.3V, VIN = VIH or VIL, Vo = 1.5V ⁽³⁾		50	90	200	mA
VOH	Output HIGH Voltage		Vcc = Min. VIN = VIH or VIL	IOH = -0.1mA	Vcc-0.2	—	—	V
				IOH = -3mA	2.4	3.0	—	
				IOH = -6mA MIL. IOH = -8mA COM'L.	2.4 ⁽⁵⁾	3.0	—	
VOL	Output LOW Voltage		Vcc = Min. VIN = VIH or VIL	IOl = 0.1mA	—	—	0.2	V
				IOl = 16mA	—	0.2	0.4	
				IOH = 24mA	—	0.3	0.5	
IOS	Short Circuit Current ⁽⁴⁾		Vcc = Max., Vo = GND ⁽³⁾		-60	-135	-240	mA
VH	Input Hysteresis		—		—	150	—	mV
ICCL ICCH IC CZ	Quiescent Power Supply Current		Vcc = Max., VIN = GND or Vcc	COM'L.	—	0.1	10	µA
				MIL.	—	0.1	100	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at Vcc = 3.3V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- This parameter is guaranteed but not tested.
- VOH = Vcc - 0.6V at rated current.
- The test limit for this parameter is ±5µA at TA = -55°C.
- Pins with Bus Hold are identified in the pin description.

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POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$	$V_{IN} = V_{CC} - 0.6V^{(3)}$	—	2.0	30	μA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $x\overline{OE} = \text{GND}$ 50% Duty Cycle One Input Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	50	75	$\mu A / \text{MHz}$
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $x\overline{OE} = \text{GND}$ $f_i = 5\text{MHz}$ 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.5	0.8	mA
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	0.5	0.8	
		$V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $x\overline{OE} = \text{GND}$ $f_i = 2.5\text{MHz}$ 50% Duty Cycle Sixteen Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	2.5	3.8 ⁽⁵⁾	
			$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	—	2.5	4.0 ⁽⁵⁾	

NOTES: 2775 tbl 07

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 3.3V$, $+25^\circ C$ ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND .
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP} N_{CP} / 2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current (} I_{CCL}, I_{CCH} \text{ and } I_{CCZ} \text{)}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input}$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $N_{CP} = \text{Number of Clock Inputs at } f_{CP}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$

SWITCHING CHARACTERISTICS OVER OPERATING RANGE⁽⁴⁾

Symbol	Parameter	Condition ⁽¹⁾	FCT163374 FCT163H374				FCT163374A FCT163H374A				FCT163374C FCT163H374C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH	Propagation Delay xCLK to xOx	CL = 50pF RL = 500Ω	2.0	10.0	2.0	11.0	2.0	6.5	2.0	7.2	2.0	5.2	—	—	ns
tPZH	Output Enable Time		1.5	12.5	1.5	14.0	1.5	6.5	1.5	7.5	1.5	5.5	—	—	ns
tPZL	Output Disable Time		1.5	8.0	1.5	8.0	1.5	5.5	1.5	6.5	1.5	5.0	—	—	ns
tsu	Set-up Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	—	—	ns
th	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	—	—	ns
tw	xCLK Pulse Width HIGH or LOW		7.0	—	7.0	—	5.0	—	6.0	—	5.0	—	—	—	ns
tsk(o)	Output Skew ⁽³⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	—	—	ns

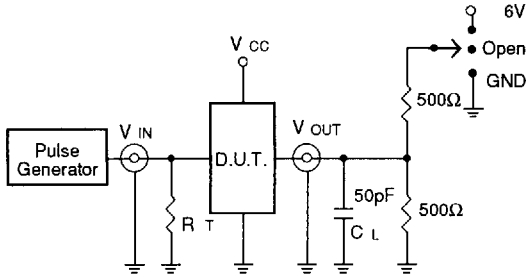
2775 tbl 08

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.
4. Propagation Delay and Enable/Disable times are with V_{CC} = 3.3V ± 0.3V, Normal Range. For V_{CC} = 2.7V to 3.6V, Extended Range, all Propagation Delays and Enable/Disable times should be degraded by 20%.

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2775 drw 05

SWITCH POSITION

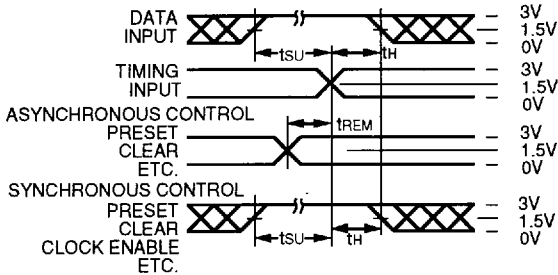
Test	Switch
Open Drain Disable Low Enable Low	6V
Disable High Enable High	GND
All Other tests	Open

DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
 R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

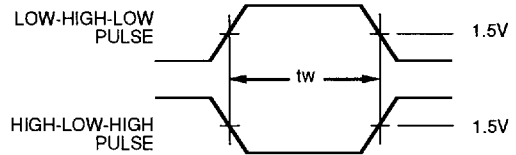
2775 Ink 09

SET-UP, HOLD AND RELEASE TIMES



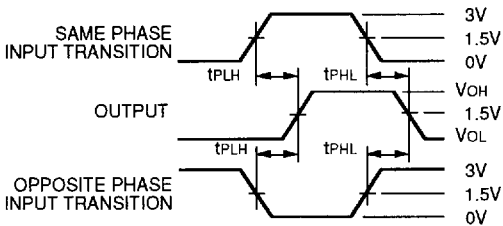
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PULSE WIDTH



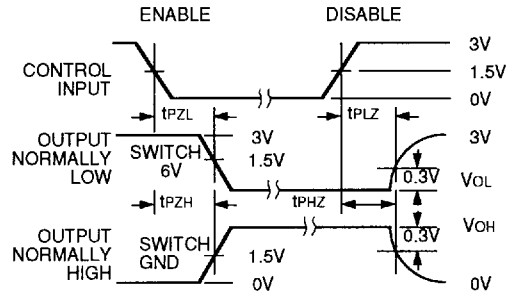
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PROPAGATION DELAY



2775 drw 08

ENABLE AND DISABLE TIMES

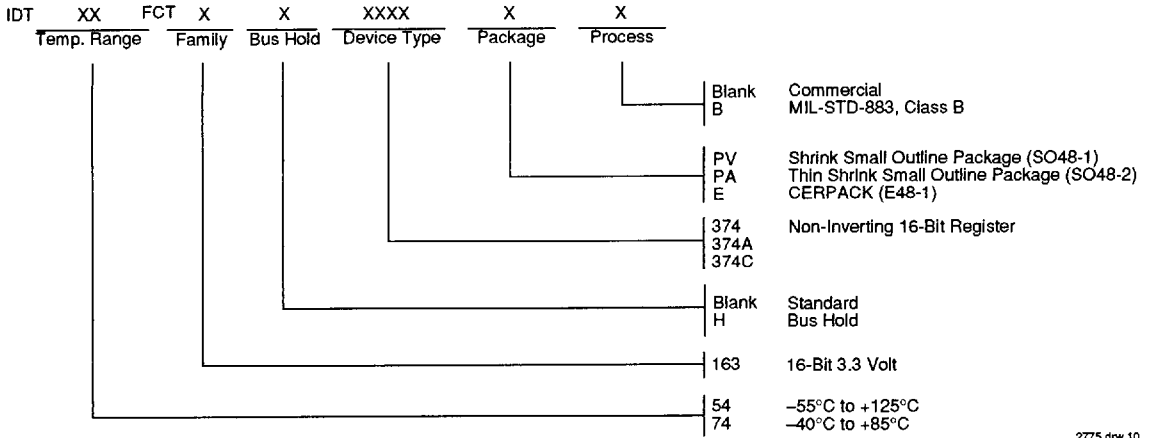


2775 drw 09

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$.
- If V_{CC} is below 3V, input voltage swings should be adjusted not to exceed V_{CC} .

ORDERING INFORMATION



2775 drw 10