# 2.5V or 3.3V, 200 MHz, 1:18 Clock Distribution Buffer

## Features

■ 200 MHz Clock Support

■ 2.5V or 3.3V Operation

■ LVCMOS/LVTTL Clock Input

■ LVCMOS-/LVTTL-Compatible Inputs

■ 18 Clock Outputs: Drive up to 36 Clock Lines

■ 110 ps Typical Output-to-output Skew

■ Output Enable Control

■ Pin Compatible with MPC942C

■ Available in Industrial and Commercial

■ 32-pin LQFP package

## Description

The CY29942 is a low voltage 200 MHz clock distribution buffer with an LVCMOS or LVTTL compatible input clock. All other control inputs are LVCMOS/LVTTL compatible. The eighteen outputs are 2.5V or 3.3V LVCMOS or LVTTL compatible and can drive 50Ω series or parallel terminated transmission lines. For series terminated transmission lines, each output can drive one or two traces giving the devices an effective fanout of 1:36. Low output-to-output skews make the CY29942 an ideal clock distribution buffer for nested clock trees in the most demanding of synchronous systems.

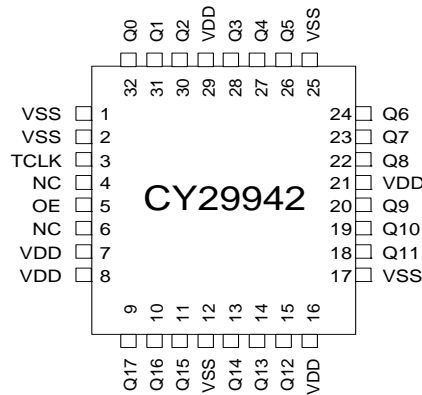## Logic Block Diagram
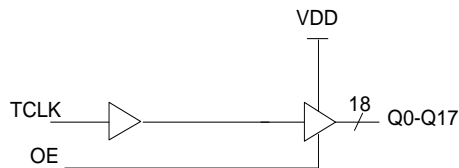
## Pinouts

**Figure 1.  Pin Configuration**



## Table 1.  Pin Description[1]

| Pin | Name | I/O | Description |
|---|---|---|---|
| 3 | TCLK | Input, PD | **External Reference/Test Clock Input** |
| 5 | OE | Input, PU | **Output Enable**. When HIGH, all outputs are enabled. When set LOW, the outputs are at high impedance. |
| 9, 10, 11, 13, 14, 15, 18, 19, 20, 22, 23, 24, 26, 27, 28, 30, 31, 32 | Q(17:0) | Output | Clock Outputs |
| 7, 8, 16, 21, 29 | VDD | | **3.3V or 2.5V Power Supply** |
| 1, 2, 12, 17, 25 | VSS | | **Common Ground** |
| 4, 6 | NC | | **No Connection** |

**Note**
1.  PD = Internal Pull-Down, PU = Internal Pull-up.

## Maximum Ratings[2]

Maximum Input Voltage Relative to $V_{SS}$:............. $V_{SS}$ − 0.3V

Maximum Input Voltage Relative to $V_{DD}$:............. $V_{DD}$ + 0.3V

Storage Temperature:....................................−65° to 150°C

Operating Temperature:..................................−40° to 85°C

Maximum ESD protection............................................... 2 kV

Maximum Power Supply:................................................ 5.5V

Maximum Input Current:............................................±20 mA

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range:

$V_{SS} < (V_{in}$ or $V_{out}) < V_{DD}$

Unused inputs must always be tied to an appropriate logic voltage level (either $V_{SS}$ or $V_{DD}$).

## DC Parameters

$V_{DD}$ = 3.3V ±5% or 2.5V ±5%, $V_{DDC}$ = 3.3V ±5% or 2.5V ±5%, Over the specified temperature range.

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | | $V_{SS}$ | | 0.8 | V |
| $V_{IH}$ | Input High Voltage | | 2.0 | | $V_{DD}$ | V |
| $I_{IL}$ | Input Low Current[3] | | | | −200 | μA |
| $I_{IH}$ | Input High Current[3] | | | | 200 | μA |
| $V_{OL}$ | Output Low Voltage[4] | $I_{OL}$ = 20 mA | | | 0.5 | V |
| $V_{OH}$ | Output High Voltage[4] | $I_{OH}$ = −20 mA, $V_{DDC}$ = 3.3V | 2.4 | | | V |
| | | $I_{OH}$ = −16 mA, $V_{DDC}$ = 2.5V | 2.0 | | | |
| $I_{DDQ}$ | Quiescent Supply Current | | | 5 | 7 | mA |
| $I_{DD}$ | Dynamic Supply Current | $V_{DD}$ = 3.3V, Outputs at 150 MHz, CL = 15 pF | | 285 | | mA |
| | | $V_{DD}$ = 3.3V, Outputs at 200 MHz, CL = 15 pF | | 335 | | |
| | | $V_{DD}$ = 2.5V, Outputs at 150 MHz, CL = 15 pF | | 200 | | |
| | | $V_{DD}$ = 2.5V, Outputs at 200 MHz, CL = 15 pF | | 240 | | |
| $Z_{out}$ | Output Impedance | $V_{DD}$ = 3.3V | 8 | 12 | 16 | Ω |
| | | $V_{DD}$ = 2.5V | 10 | 15 | 20 | |
| $C_{in}$ | Input Capacitance | | | 4 | | pF |

**Notes**
2. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
3. Inputs have pull-up/pull-down resistors that effect input current.
4. Driving series or parallel terminated 50Ω (or 50Ω to $V_{DD}/2$) transmission lines.

[+] Feedback

## AC Parameters

$V_{DD}$ = 3.3V ±5% or 2.5V ±5%, $V_{DDC}$ = 3.3V ±5% or 2.5V ±5%, Over the specified temperature range[5]

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Fmax | Input Frequency | | | | 200 | MHz |
| Tpd | TTL_CLK to Q Delay[6, 7] | $V_{DD}$ = 3.3V | 1.8 | 3.3 | 3.8 | ns |
| | | $V_{DD}$ = 2.5V | 2.3 | 3.8 | 4.4 | |
| FoutDC | Output Duty Cycle[6, 7, 8] | Measured at $V_{DD}$/2 | 45 | | 55 | % |
| Tskew | Output-to-Output Skew[6, 7] | | | 110 | 200 | ps |
| Tskew(pp) | Part-to-Part Skew[9] | $V_{DD}$ = 3.3V | | | 1.0 | ns |
| | | $V_{DD}$ = 2.5V | | | 1.3 | |
| Tskew(pp) | Part-to-Part Skew[10] | | | | 600 | ps |
| Tr/Tf | Output Clocks Rise/Fall Time[6, 7] | 0.8V to 2.0V, $V_{DD}$ = 3.3V | 0.2 | | 1.1 | ns |
| | | 0.5V to 1.8V, $V_{DD}$ = 2.5V | | | | |

**Notes**
5. Parameters are guaranteed by design and characterization. Not 100% tested in production. All parameters specified with loaded outputs.
6. Outputs driving 50Ω transmission lines.
7. See Figure 2.
8. 50% input duty cycle.
9. Across temperature and voltage ranges, includes output skew.
10. For a specific temperature and voltage, includes output skew.

**Figure 2.  LVCMOS_CLK CY29942 Test Reference for VCC = 3.3V and VCC = 2.5V**
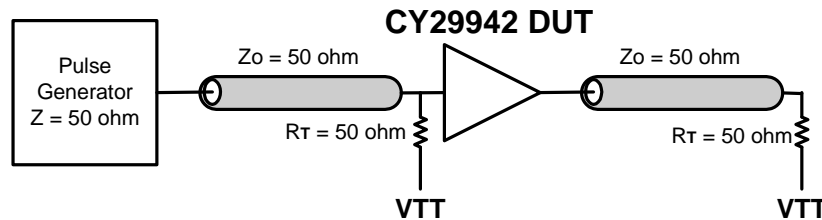


**Figure 3.  LVCMOS Propagation Delay (TPD) Test Reference**
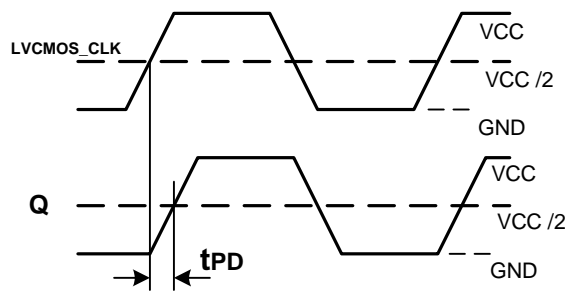
**Figure 4. Output Duty Cycle (FoutDC)**



$$DC = tP / T0 \times 100\%$$
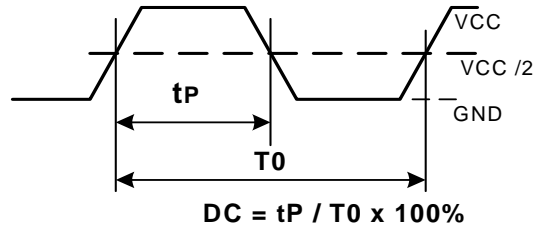
**Figure 5.**

**Figure 6. Output-to-Output Skew tsk(0)**
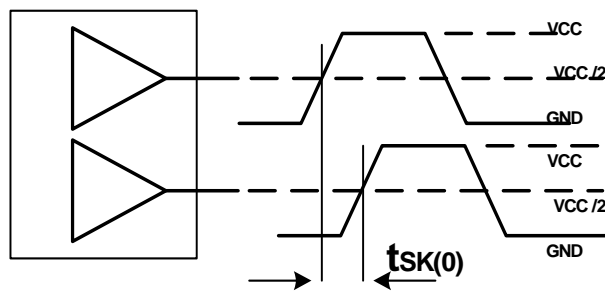


**Figure 7.**

## Ordering Information

| Part Number | Package Type | Production Flow |
|---|---|---|
| CY29942AI | 32-Pin LQFP | Industrial,–40° to 85°C |
| CY29942AIT | 32-Pin LQFP – Tape and Reel | Industrial, –40° to 85°C |
| CY29942AC | 32-Pin LQFP | Commercial, 0° to 70°C |
| Pb-free | | |
| CY29942AXI | 32-Pin LQFP | Industrial, –40° to 85°C |
| CY29942AXIT | 32-Pin LQFP – Tape and Reel | Industrial, –40° to 85°C |
| CY29942AXC | 32-Pin LQFP | Commercial, 0° to 70°C |
| CY29942AXCT | 32-Pin LQFP – Tape and Reel | Commercial, 0° to 70°C |

[+] Feedback

## Package Drawing and Dimensions

### 32-Pin Thin Plastic Quad Flatpack 7 x 7 x 1.4 mm A32.14



51-85088-*B
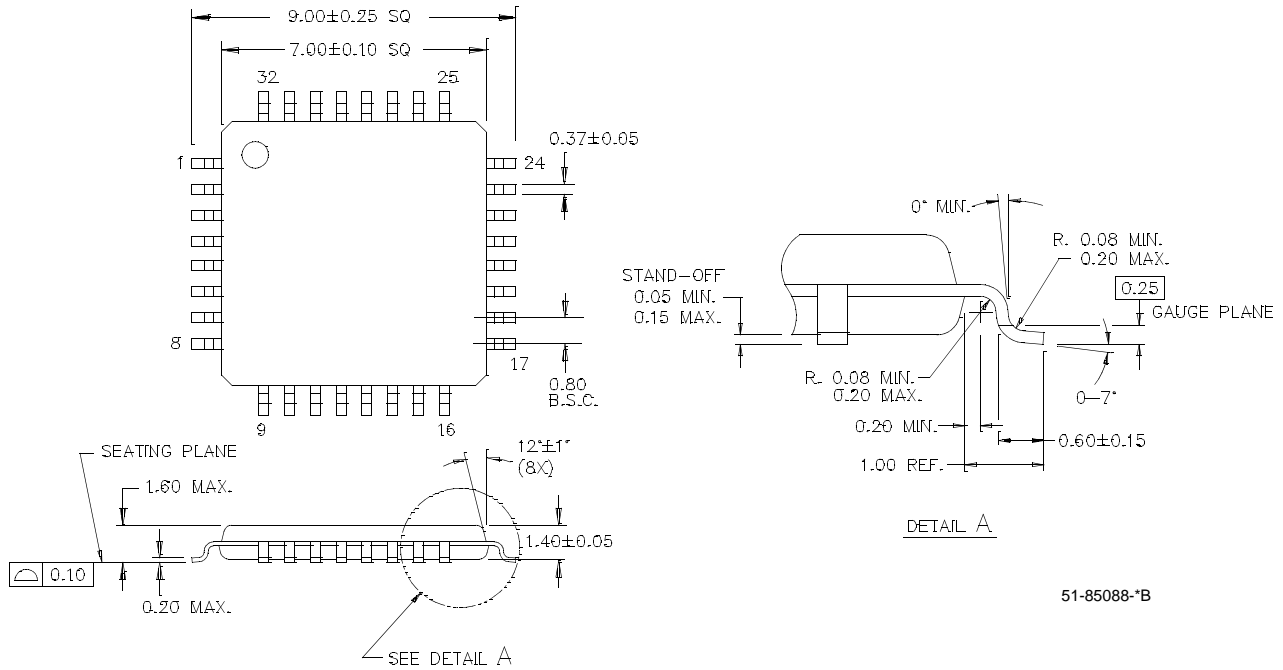
## Document History Page

| Document Title: CY29942 2.5V or 3.3V, 200 MHz, 1:18 Clock Distribution Buffer Document Number: 38-07284 | | | | |
|---|---|---|---|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 111095 | BRK | 02/07/02 | New datasheet |
| *A | 116777 | HWT | 08/14/02 | Added a Commercial Temp. Range in the Ordering Information |
| *B | 122876 | RBI | 12/21/02 | Add power up requirements to maximum rating information. |
| *C | 334117 | RGL | See ECN | Added Lead-free devices Added typical value for output-output skew |
| *D | 2761988 | KVM | 09/10/09 | Ordering Information table: fixed typo and removed obsolete CY29942ACT. Changed Lead-free to Pb-free. |

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