

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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EOL announced Product

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SWITCHING

N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK2515 is N-Channel MOS Field Effect Transistors designed for high current switching applications.

FEATURES

- Super Low on-state resistance
 $R_{DS(on)1} = 9.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 25 \text{ A)}$
 $R_{DS(on)2} = 14 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4 \text{ V, } I_D = 25 \text{ A)}$
- Low input capacitance
 $C_{iss} = 3\,400 \text{ pF TYP.}$
- Built-in G-S Protection Diode

ABSOLUTE MAXIMUM RATINGS ($T_A = 25 \text{ }^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_D \text{ (DC)}$	± 50	A
Drain Current (pulse)*	$I_D \text{ (pulse)}$	± 200	A
Total Power Dissipation ($T_c = 25 \text{ }^\circ\text{C}$)	P_{T1}	150	W
Total Power Dissipation ($T_A = 25 \text{ }^\circ\text{C}$)	P_{T2}	3.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current**	I_{AS}	50	A
Single Avalanche Energy**	E_{AS}	250	mJ

* $PW \leq 10 \text{ } \mu\text{s}$, Duty Cycle $\leq 1 \%$

** Starting $T_{ch} = 25 \text{ }^\circ\text{C}$, $R_G = 25 \text{ } \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0$

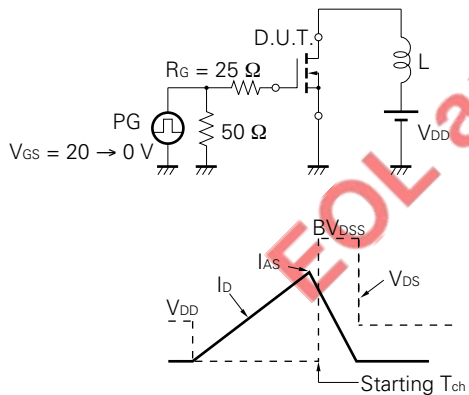
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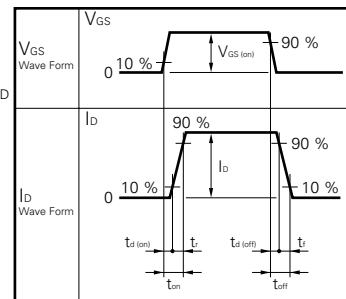
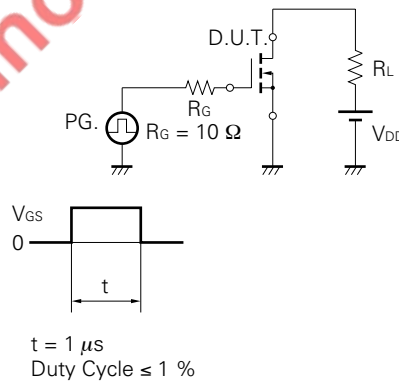
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-Resistance	R _{DS(on)1}		7.3	9.0	mΩ	V _{GS} = 10 V, I _D = 25 A
Drain to Source On-Resistance	R _{DS(on)2}		11	14	mΩ	V _{GS} = 4 V, I _D = 25 A
Gate to Source Cutoff Voltage	V _{GS(off)}	1.0	1.5	2.0	V	V _{DS} = 10 V, I _D = 1 mA
Forward Transfer Admittance	y _{fs}	20	58		S	V _{DS} = 10 V, I _D = 25 A
Drain Leakage Current	I _{DSS}			10	μA	V _{DS} = V _{DSS} , V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±20 V, V _{DS} = 0
Input Capacitance	C _{iss}		3 400		pF	V _{DS} = 10 V
Output Capacitance	C _{oss}		1 600		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		770		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		55		ns	I _D = 25 A
Rise Time	t _r		360		ns	V _{GS(on)} = 10 V
Turn-Off Delay Time	t _{d(off)}		480		ns	V _{DD} = 30 V
Fall Time	t _f		360		ns	R _G = 10 Ω
Total Gate Charge	Q _G		152		nC	I _D = 50 A
Gate to Source Charge	Q _{GS}		11		nC	V _{DD} = 48 V
Gate to Drain Charge	Q _{GD}		60		nC	V _{GS} = 10 V
Body Diode Forward Voltage	V _{F(S-D)}		0.92		V	I _F = 50 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		105		ns	I _F = 50 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		265		nC	di/dt = 100 A/μs

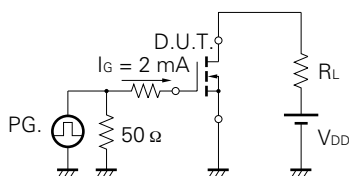
Test Circuit 1 Avalanche Capability



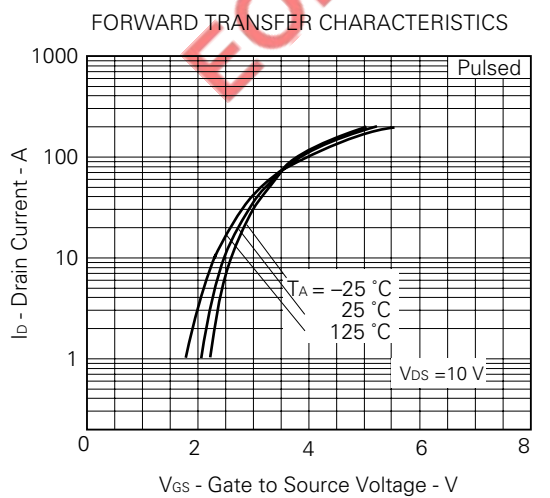
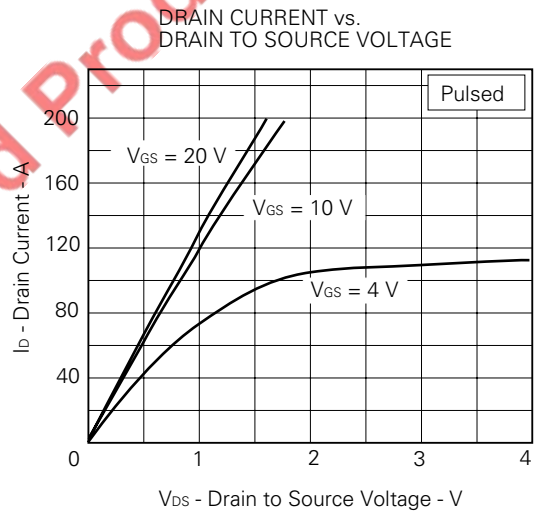
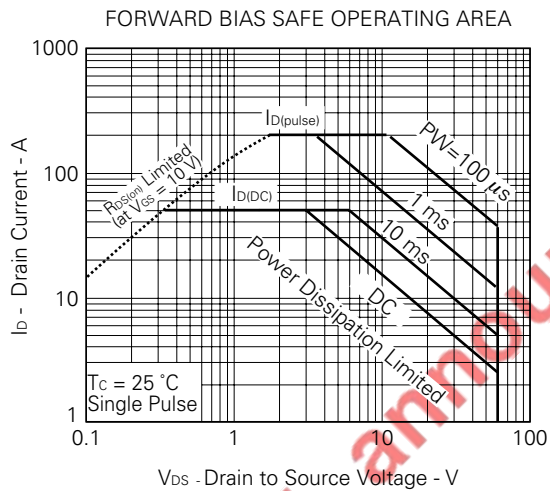
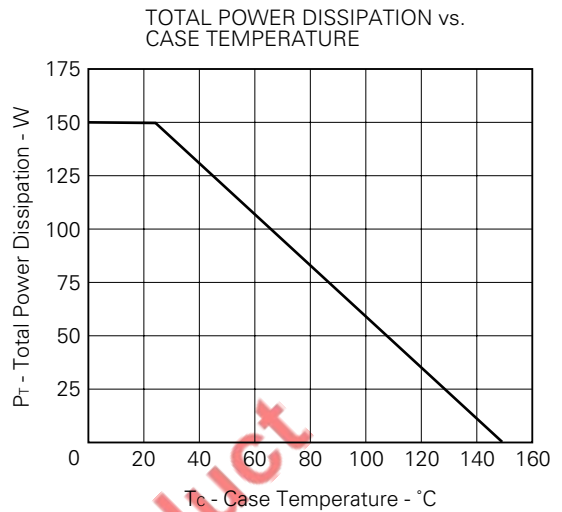
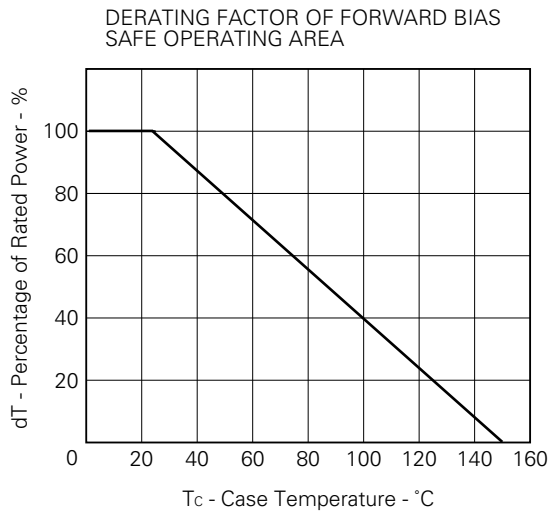
Test Circuit 2 Switching Time



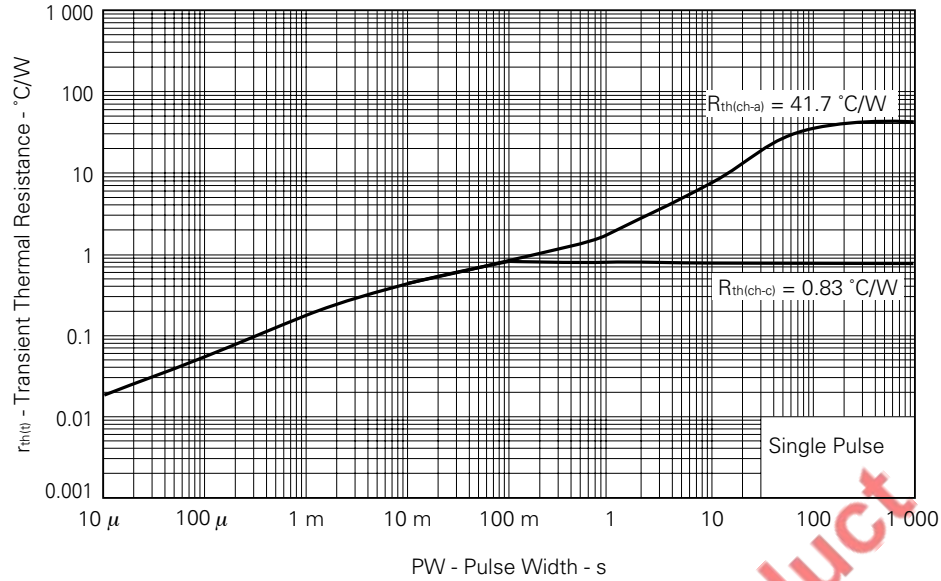
Test Circuit 3 Gate Charge



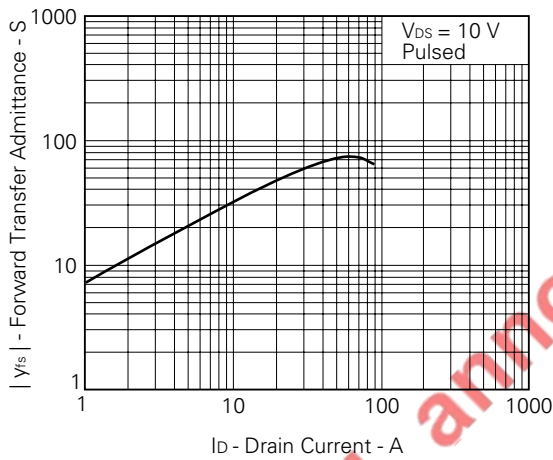
TYPICAL CHARACTERISTICS (T_A = 25 °C)



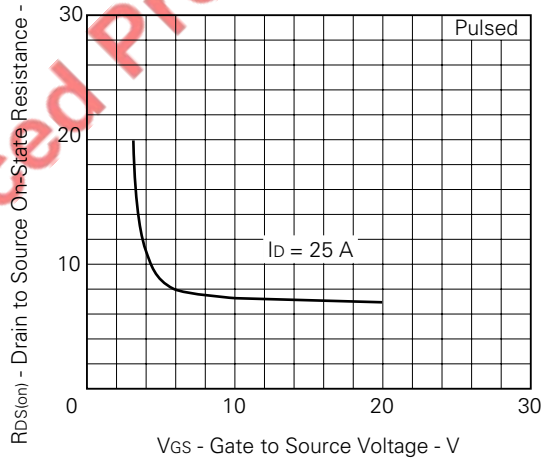
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



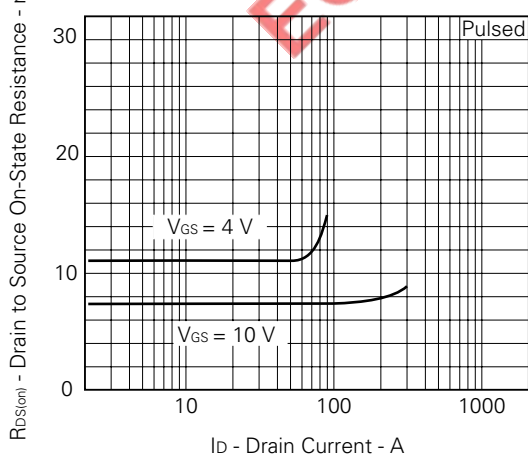
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



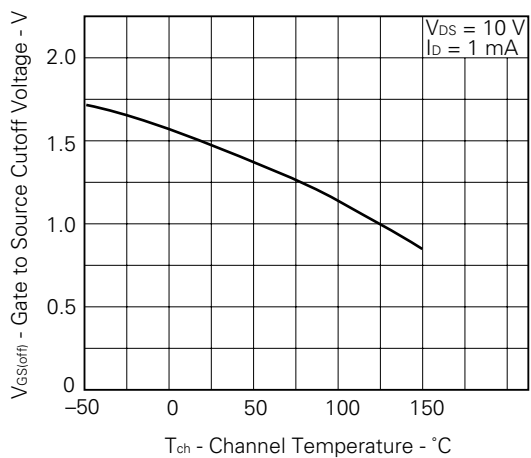
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



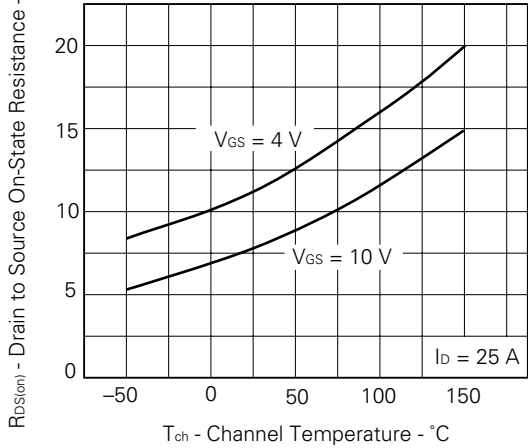
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



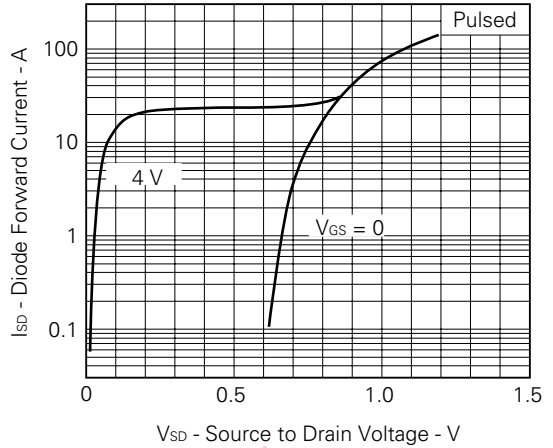
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



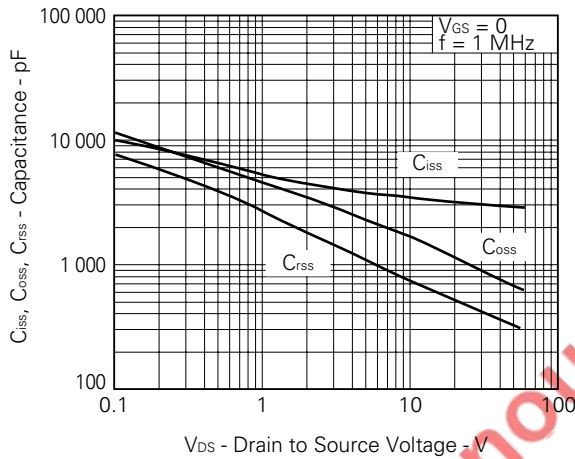
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



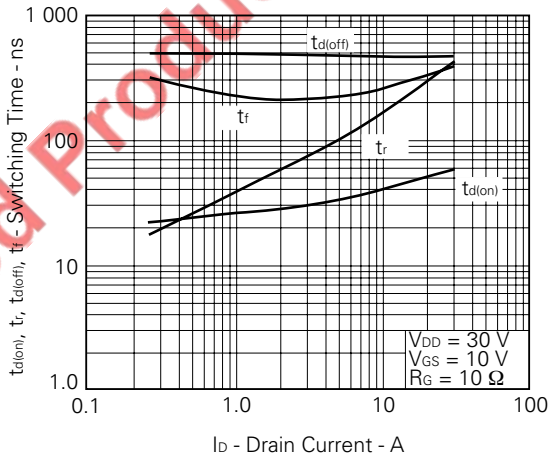
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



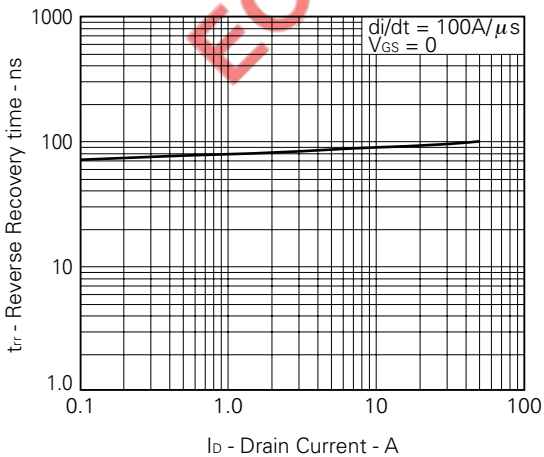
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



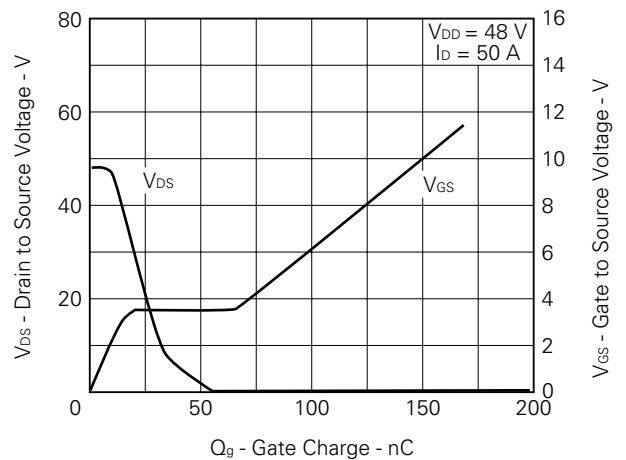
SWITCHING CHARACTERISTICS



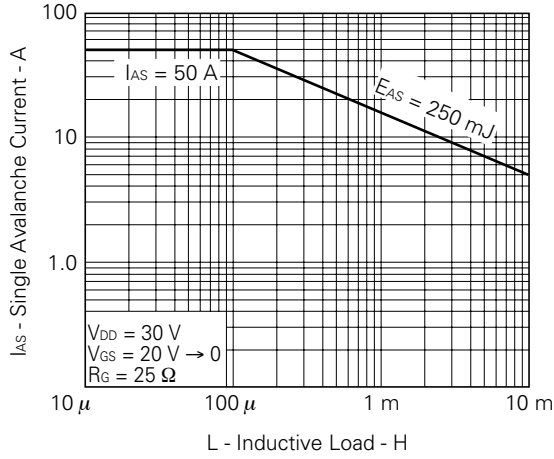
REVERSE RECOVERY TIME vs. DRAIN CURRENT



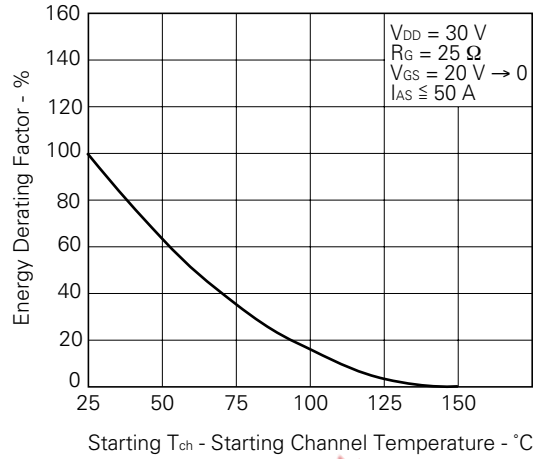
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



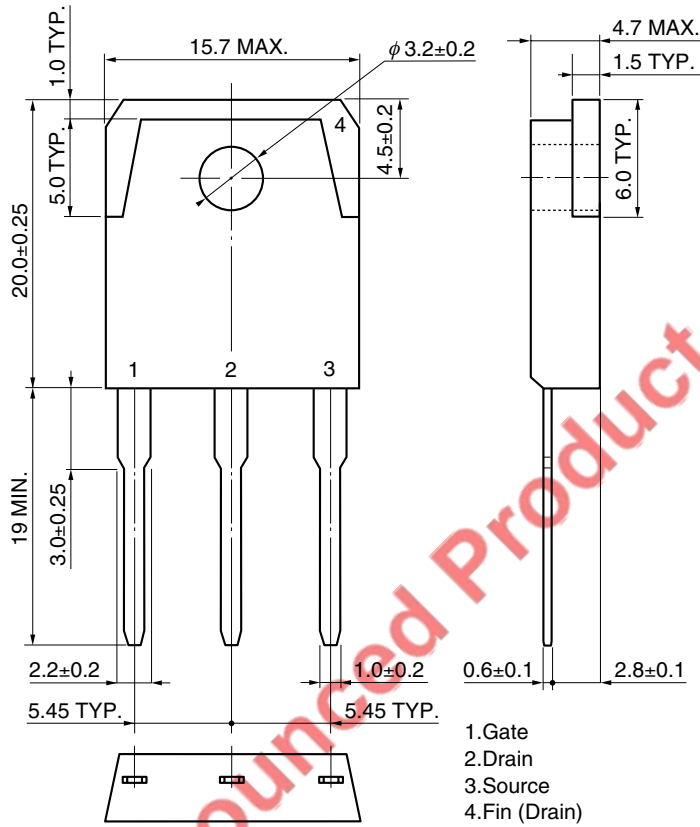
SINGLE AVALANCHE ENERGY DERATING FACTOR



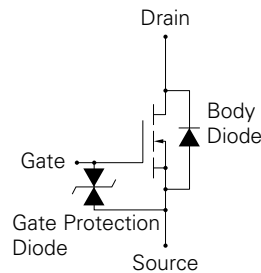
EOL announced Product

PACKAGE DRAWING (Unit: mm)

<R> TO-3P (MP-88)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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