AFE1105

HDSL/MDSL ANALOG FRONT END

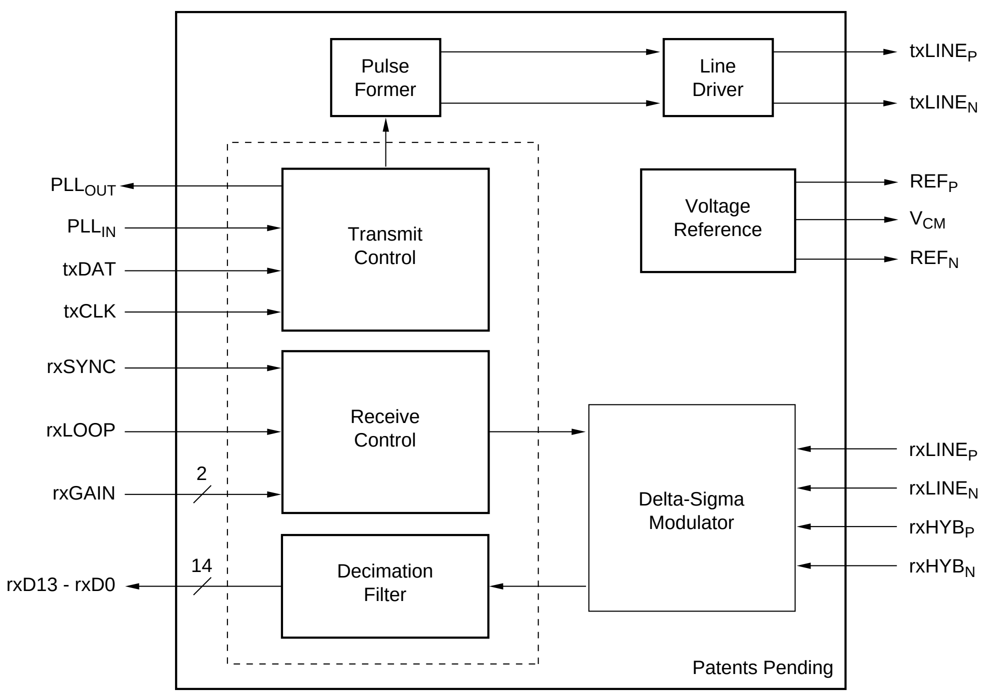
FEATURES

- COMPLETE ANALOG INTERFACE
- T1, E1, AND MDSL OPERATION
- CLOCK SCALEABLE SPEED
- SINGLE CHIP SOLUTION
- +5V ONLY (5V OR 3.3V DIGITAL)
- 250mW POWER DISSIPATION
- 48-PIN SSOP
- –40°C TO +85°C OPERATION

DESCRIPTION

Burr-Brown's Analog Front End greatly reduces the size and cost of an HDSL or MDSL system by providing all of the active analog circuitry needed to connect the Metalink MtH1210B HDSL digital signal processor to an external compromise hybrid and a 1:2.3 HDSL line transformer. All internal filter responses as well as the pulse former output scale with clock frequency—allowing the AFE1105 to operate over a range of bit rates from 196kbps to 1.168Mbps.

Functionally, this unit is separated into a transmit and a receive section. The transmit section generates, filters, and buffers outgoing 2B1Q data. The receive section filters and digitizes the symbol data received on the telephone line and passes it to the MtH1210B. The HDSL Analog Interface is a monolithic device fabricated on 0.6µCMOS. It operates on a single +5V supply. It is housed in a 48-pin SSOP package.



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SPECIFICATIONS

Typical at 25°C, AV_{DD} = +5V, DV_{DD} = +3.3V, f_{tx} = 584kHz (E1 rate), unless otherwise specified.

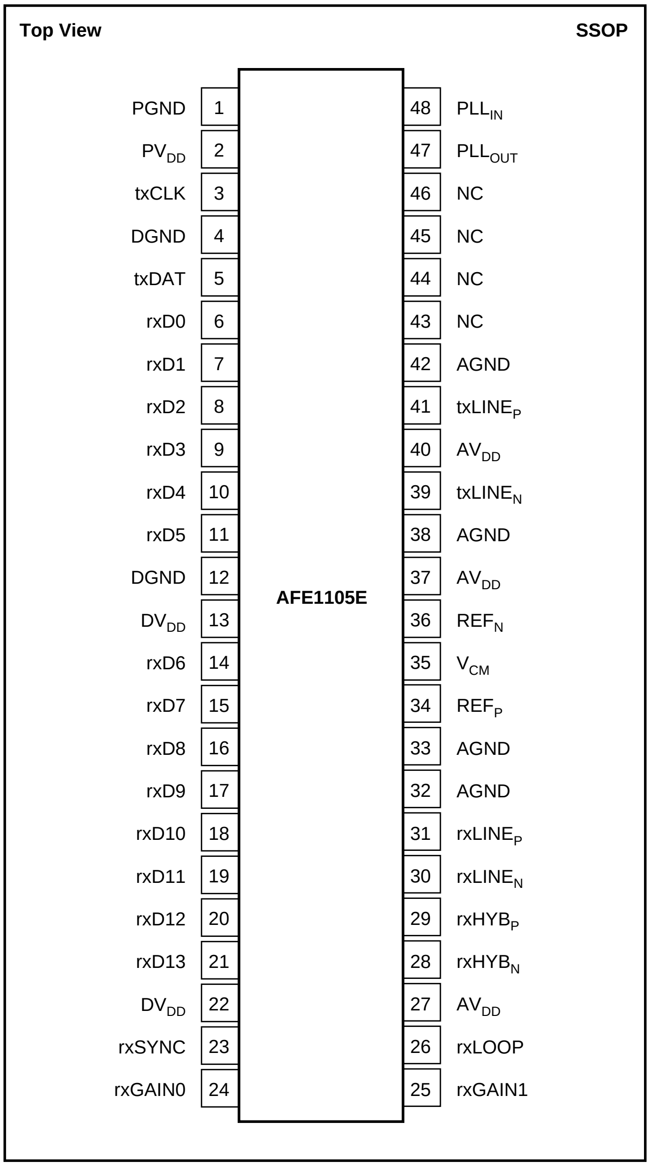
		AFE1105E			
PARAMETER	COMMENTS	MIN	TYP	MAX	UNITS
RECEIVE CHANNEL					
Number of Inputs	Differential	2			
Input Voltage Range	Balanced Differential[1]		±3.0		V
Common-Mode Voltage	1.5V CMV Recommended		+1.5		V
Input Impedance	All Inputs		See Typical Performance Curves		
Input Capacitance			10		pF
Input Gain Matching	Line Input vs Hybrid Input		±2		%
Resolution		14			Bits
Programmable Gain	Four Gains: 0dB, 3.25dB, 6dB, and 9dB	0		9	dB
Settling Time for Gain Change			6		Symbol Periods
Gain + Offset Error	Tested at Each Gain Range		5		%FSR[2]
Output Data Coding			Two's Complement		
Output Data Rate, rxSYNC[3]		98		584[4]	kHz
TRANSMIT CHANNEL					
Transmit Symbol Rate, f_{tx}		98		584[4]	kHz
T1 Transmit –3dB Point	Bellcore TA-NWT-3017 Compliant		196		kHz
T1 Rate Power Spectral Density[5]			See Typical Performance Curves		
E1 Transmit –3dB Point	ETSI RTR/TM-03036 Compliant		292		kHz
E1 Rate Power Spectral Density[5]			See Typical Performance Curves		
Transmit Power[5]		13		14	dBm
Pulse Output			See Typical Performance Curves		
Common-Mode Voltage, V_{CM}			AV_{DD}/2		V
Output Resistance[6]	DC to 1MHz		1		Ω
TRANSCEIVER PERFORMANCE					
Uncancelled Echo[7]	rxGAIN = 0dB, Loopback Enabled			–67	dB
	rxGAIN = 0dB, Loopback Disabled			–67	dB
	rxGAIN = 3.25dB, Loopback Disabled			–69	dB
	rxGAIN = 6dB, Loopback Disabled			–71	dB
	rxGAIN = 9dB, Loopback Disabled			–73	dB
DIGITAL INTERFACE[6]					
Logic Levels					
V_{IH}	$\|I_{IH}\|$ < 10µA	DV_{DD} –1		DV_{DD} +0.3	V
V_{IL}	$\|I_{IL}\|$ < 10µA	–0.3		+0.8	V
V_{OH}	I_{OH} = –20µA	DV_{DD} –0.5			V
V_{OL}	I_{OL} = 20µA			+0.4	V
Transmit/Receive Channel Interface					
t_{tx1}	txCLK Period	1.7		10.2	µs
t_{tx2}	txCLK Pulse Width	t_{tx1}/16		$15t_{tx1}$/16	ns
POWER					
Analog Power Supply Voltage	Specification		5		V
Analog Power Supply Voltage	Operating Range	4.75		5.25	V
Digital Power Supply Voltage	Specification		3.3		V
Digital Power Supply Voltage	Operating Range	3.15		5.25	V
Power Dissipation[4, 8]	DV_{DD} = 3.3V, 1:2 Line Transformer		250		mW
Power Dissipation[4, 8]	DV_{DD} = 5V, 1:2 Line Transformer		300		mW
PSRR		60			dB
TEMPERATURE RANGE					
Operating[6]		–40		+85	°C

NOTES: (1) With a balanced differential signal, the positive input is 180° out of phase with the negative input, therefore the actual voltage swing about the common mode voltage on each pin is ±1.5V to achieve a differential input range of ±3.0V or 6Vp-p. (2) FSR is Full-Scale Range. (3) The output data is available at twice the symbol rate with interpolated values. (4) This specification does not apply to the AFE1105EA. (5) With a pseudo-random equiprobable sequence of HDSL pulses; 13.5dBm applied to the transformer (27dBm output from $txLINE_P$ and $txLINE_N$). (6) Guaranteed by design and characterization. (7) Uncancelled Echo is a measure of the total analog errors in the transmitter and receiver sections including the effect of non-linearity and noise. See the Discussion of Specifications section of this data sheet for more information. (8) Power dissipation includes only the power dissipated within the component and does not include power dissipated in the external loads. The AFE1105 is tested with a 1:2 line transformer, but will typically be used with a 1:2.3 line transformer, this will slightly increase power dissipation.

PIN DESCRIPTIONS

PIN #	TYPE	NAME	DESCRIPTION
1	Ground	PGND	Analog Ground for PLL
2	Power	PV_{DD}	Analog Supply (+5V) for PLL
3	Input	txCLK	Symbol Clock (XMTLE from MtH1210B) (392kHz for T1, 584kHz for E1)
4	Ground	DGND	Digital Ground
5	Input	txDAT	XMTDA from MtH1210B
6	Output	rxD0	ADC Output Bit-0
7	Output	rxD1	ADC Output Bit-1
8	Output	rxD2	ADC Output Bit-2 (RCVD0 from MtH1210B)
9	Output	rxD3	ADC Output Bit-3 (RCVD1 from MtH1210B)
10	Output	rxD4	ADC Output Bit-4 (RCVD2 from MtH1210B)
11	Output	rxD5	ADC Output Bit-5 (RCVD3 from MtH1210B)
12	Ground	DGND	Digital Ground
13	Power	DV_{DD}	Digital Supply (+3.3V to +5V)
14	Output	rxD6	ADC Output Bit-6 (RCVD4 from MtH1210B)
15	Output	rxD7	ADC Output Bit-7 (RCVD5 from MtH1210B)
16	Output	rxD8	ADC Output Bit-8 (RCVD6 from MtH1210B)
17	Output	rxD9	ADC Output Bit-9 (RCVD7 from MtH1210B)
18	Output	rxD10	ADC Output Bit-10 (RCVD8 from MtH1210B)
19	Output	rxD11	ADC Output Bit-11 (RCVD9 from MtH1210B)
20	Output	rxD12	ADC Output Bit-12 (RCVD10 from MtH1210B)
21	Output	rxD13	ADC Output Bit-13 (RCVD11 from MtH1210B)
22	Power	DV_{DD}	Digital Supply (+3.3V to +5V)
23	Input	rxSYNC	ADC Sync Signal (RCVCK from MtH1210B) (392kHz for T1, 584kHz for E1)
24	Input	rxGAIN0	Receive Gain Control Bit-0
25	Input	rxGAIN1	Receive Gain Control Bit-1 (RCVG0 from MtH1210B)
26	Input	rxLOOP	Loopback Control Signal (loopback is enabled by positive signal)
27	Power	AV_{DD}	Analog Supply (+5V)
28	Input	$rxHYB_N$	Negative Input from Hybrid Network
29	Input	$rxHYB_P$	Positive Input from Hybrid Network
30	Input	$rxLINE_N$	Negative Line Input
31	Input	$rxLINE_P$	Positive Line Input
32	Ground	AGND	Analog Ground
33	Ground	AGND	Analog Ground
34	Output	REF_P	Positive Reference Output, Nominally 3.5V
35	Output	V_{CM}	Common-Mode Voltage (buffered), Nominally 2.5V
36	Output	REF_N	Negative Reference Output, Nominally 1.5V
37	Power	AV_{DD}	Analog Supply (+5V)
38	Ground	AGND	Analog Ground
39	Output	$txLINE_N$	Transmit Line Output Negative
40	Power	AV_{DD}	Analog Supply (+5V)
41	Output	$txLINE_P$	Transmit Line Output Positive
42	Ground	AGND	Analog Ground
43	NC	NC	Connection to Ground Recommended
44	NC	NC	Connection to Ground Recommended
45	NC	NC	Connection to Ground Recommended
46	NC	NC	Connection to Ground Recommended
47	Output	PLL_{OUT}	PLL Filter Output
48	Input	PLL_{IN}	PLL Filter Input

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Analog Inputs: Current	±100mA, Momentary
	±10mA, Continuous
Voltage	AGND –0.3V to AV_{DD} +0.3V
Analog Outputs Short Circuit to Ground (+25°C)	Continuous
AV_{DD} to AGND	–0.3V to 6V
PV_{DD} to PGND	–0.3V to 6V
DV_{DD} to DGND	–0.3V to 6V
PLL_{IN} or PLL_{OUT} to PGND	–0.3V to PV_{DD} +0.3V
Digital Input Voltage to DGND	–0.3V to DV_{DD} +0.3V
Digital Output Voltage to DGND	–0.3V to DV_{DD} +0.3V
AGND, DGND, PGND Differential Voltage	0.3V
Junction Temperature (T_J)	+150°C
Storage Temperature Range	–40°C to +125°C
Lead Temperature (soldering, 3s)	+260°C
Power Dissipation	700mW

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

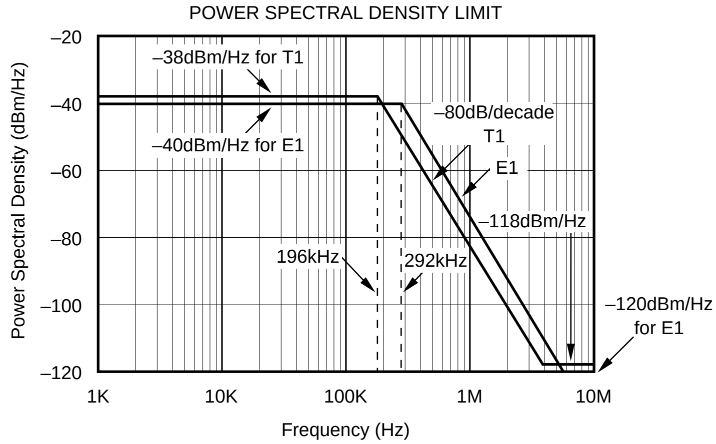
PRODUCT	MAXIMUM BIT RATE	PACKAGE	PACKAGE DRAWING NUMBER(1)	TEMPERATURE RANGE
AFE1105E	1.168Mbps	48-Pin Plastic SSOP	333	–40°C to +85°C
AFE1105EA	512kbps	48-Pin Plastic SSOP	333	–40°C to +85°C

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

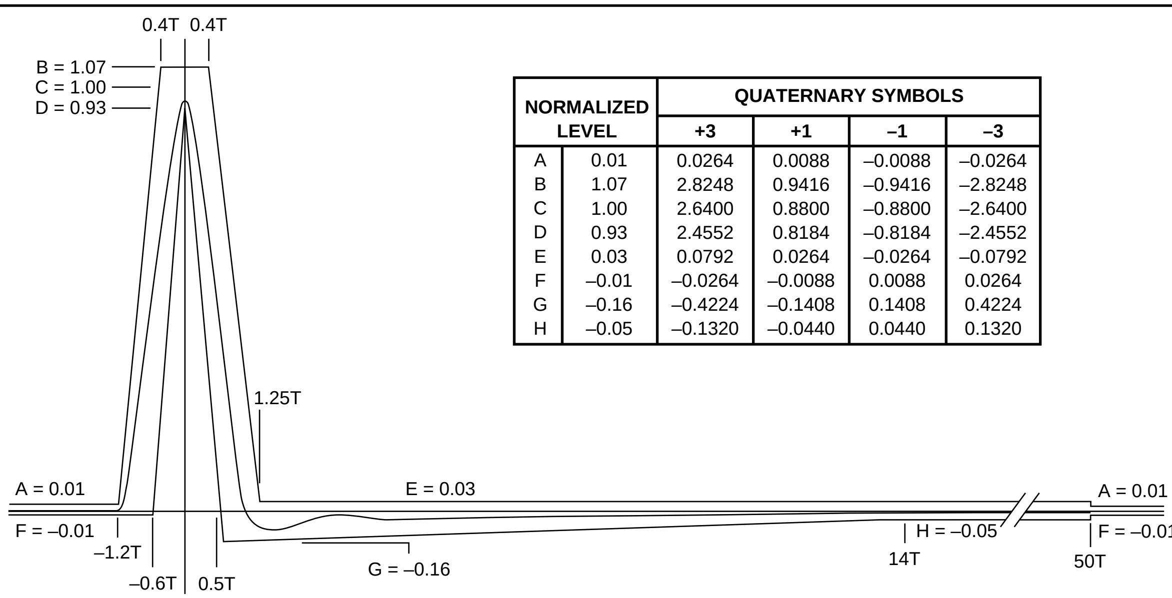
TYPICAL PERFORMANCE CURVES

At Output of Pulse Transformer

Typical at 25°C, AV_{DD} = +5V, DV_{DD} = +3.3V, unless otherwise specified.

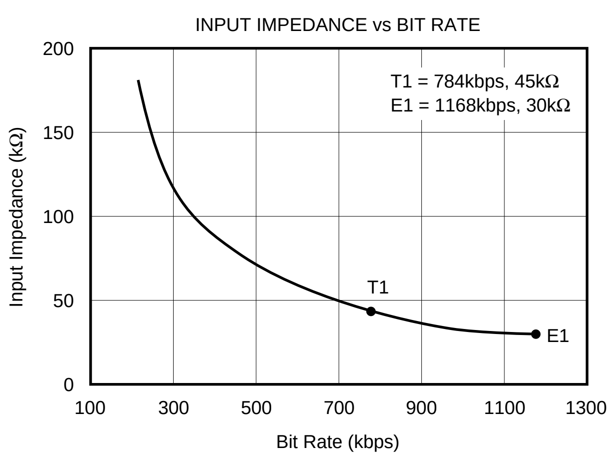


CURVE 1. Upper Bound of Power Spectral Density Measured at the Transformer Output.



NORMALIZED LEVEL		QUATERNARY SYMBOLS			
		+3	+1	–1	–3
A	0.01	0.0264	0.0088	–0.0088	–0.0264
B	1.07	2.8248	0.9416	–0.9416	–2.8248
C	1.00	2.6400	0.8800	–0.8800	–2.6400
D	0.93	2.4552	0.8184	–0.8184	–2.4552
E	0.03	0.0792	0.0264	–0.0264	–0.0792
F	–0.01	–0.0264	–0.0088	0.0088	0.0264
G	–0.16	–0.4224	–0.1408	0.1408	0.4224
H	–0.05	–0.1320	–0.0440	0.0440	0.1320

CURVE 2. Transmitted Pulse Template and Actual Performance as Measured at the Transformer Output.



CURVE 3. Input Impedance of rxLINE and rxHYB.

THEORY OF OPERATION

The transmit channel consists of a switched-capacitor pulse forming network followed by a differential line driver. The pulse forming network receives symbol data from the XMTDA output of the MtH1210B and generates a 2B1Q output waveform. The output meets the pulse mask and power spectral density requirements defined in European Telecommunications Standards Institute document RTR/TM-03036 for E1 mode and in sections 6.2.1 and 6.2.2.1 of Bellcore technical advisory TA-NWT-001210 for T1 mode. The differential line driver uses a composite output stage combining class B operation (for high efficiency driving large signals) with class AB operation (to minimize cross-over distortion).

The receive channel is designed around a fourth-order delta sigma A/D converter. It includes a difference amplifier designed to be used with an external compromise hybrid for first order analog crosstalk reduction. A programmable gain amplifier with gains of 0dB to +9dB is also included. The delta sigma modulator operating at a 24X oversampling ratio produces 14 bits of resolution at output rates up to 584kHz. The basic functionality of the AFE1105 is illustrated in Figure 1 shown below.

The receive channel operates by summing the two differential inputs, one from the line (rxLINE) and the other from the compromise hybrid (rxHYB). The connection of these two inputs so that the hybrid signal is subtracted from the line signal is described in the paragraph titled “Echo Cancellation in the AFE”. The equivalent gain for each input in the difference amp is 1. The resulting signal then passes to a programmable gain amplifier which can be set for gains of 0dB through 9dB. The ADC converts the signal to a 14-bit digital word, rxD13-rxD0.

rxLOOP INPUT

rxLOOP is the loopback control signal. When enabled, the $rxLINE_P$ and $rxLINE_N$ inputs are disconnected from the AFE. The $rxHYB_P$ and $rxHYB_N$ inputs remain connected. Loopback is enabled by applying a positive signal (Logic 1) to rxLOOP.

ECHO CANCELLATION IN THE AFE

The rxHYB input is designed to be subtracted from the rxLINE input for first order echo cancellation. To accomplish this, note that the rxLINE input is connected to the same polarity signal at the transformer (positive to positive and negative to negative) while the rxHYB input is connected to opposite polarity through the compromise hybrid (negative to positive and positive to negative) as shown in Figure 2.

RECEIVE DATA CODING

The data from the receive channel A/D converter is coded in two’s complement code.

ANALOG INPUT	OUTPUT CODE (rxD13 - rxD0)
Positive Full Scale	01111111111111
Mid Scale	00000000000000
Negative Full Scale	10000000000000

RECEIVE CHANNEL PROGRAMMABLE GAIN AMPLIFIER

The gain of the amplifier at the input of the Receive Channel is set by two gain control pins, rxGAIN1 and rxGAIN0. The resulting gain between 0dB and +9dB is shown below.

rxGAIN1	rxGAIN0	GAIN
0	0	0dB
0	1	3.25dB
1	0	6dB
1	1	9dB

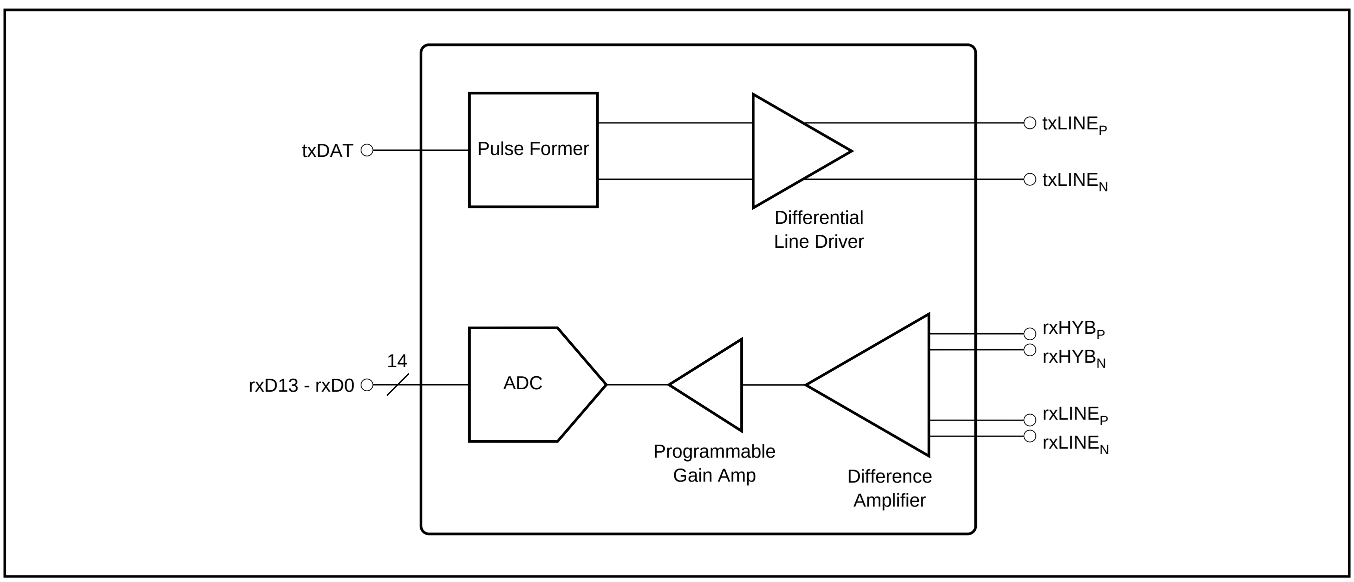


FIGURE 1. Functional Block Diagram of AFE1105.

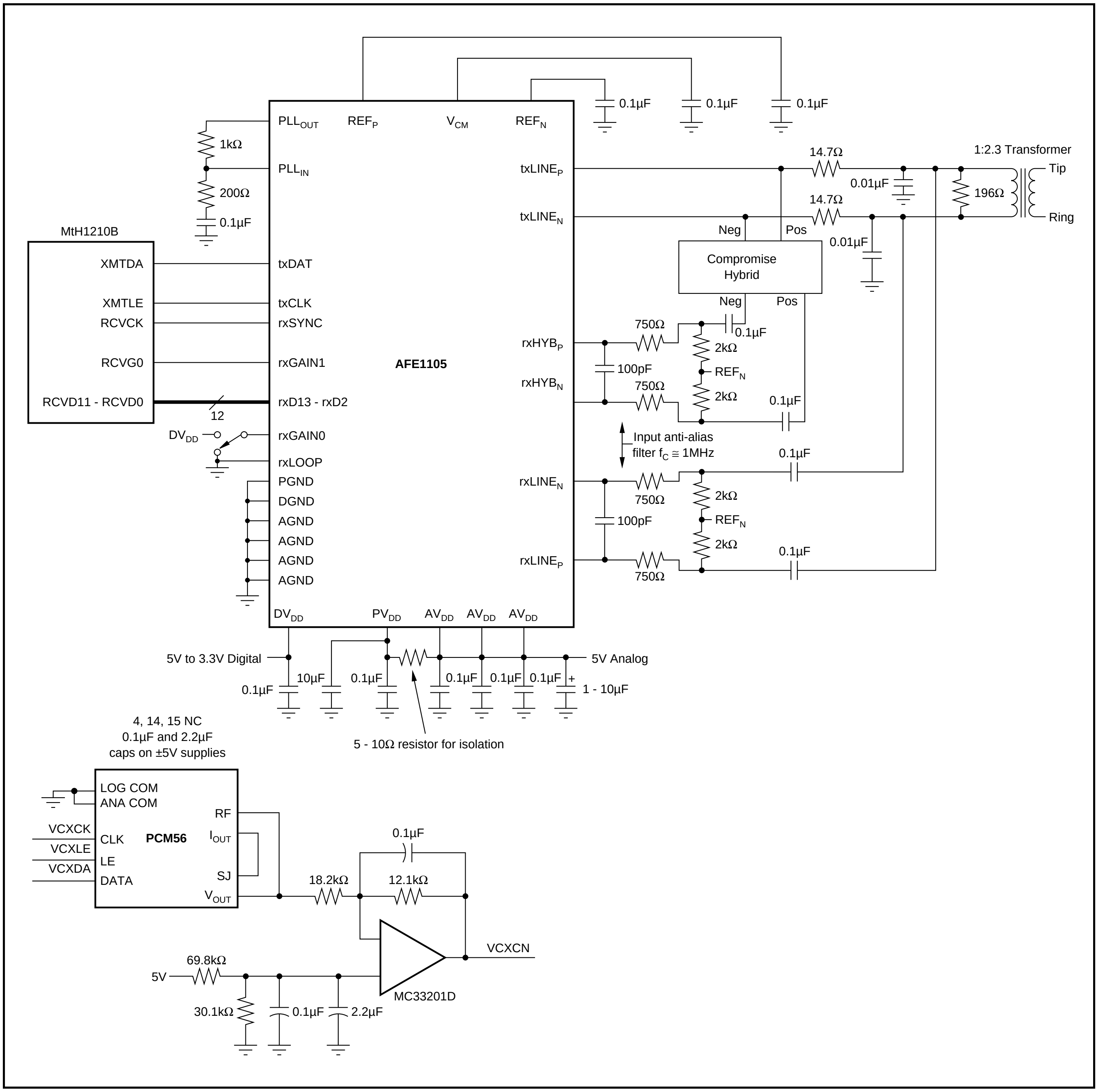


FIGURE 2. Basic Connection Diagram.

rxHYB AND rxLINE INPUT ANTI-ALIASING FILTERS

The –3dB frequency of the input anti-aliasing filter for the rxLINE and rxHYB differential inputs should be about 1MHz. Suggested values for the filter are 750Ω for each of the two input resistors and 100pF for the capacitor. Together the two 750Ω resistors and the 100pF capacitor result in –3dB frequency of just over 1MHz. The 750Ω input resistors will result in a minimal voltage divider loss with the input impedance of the AFE1105.

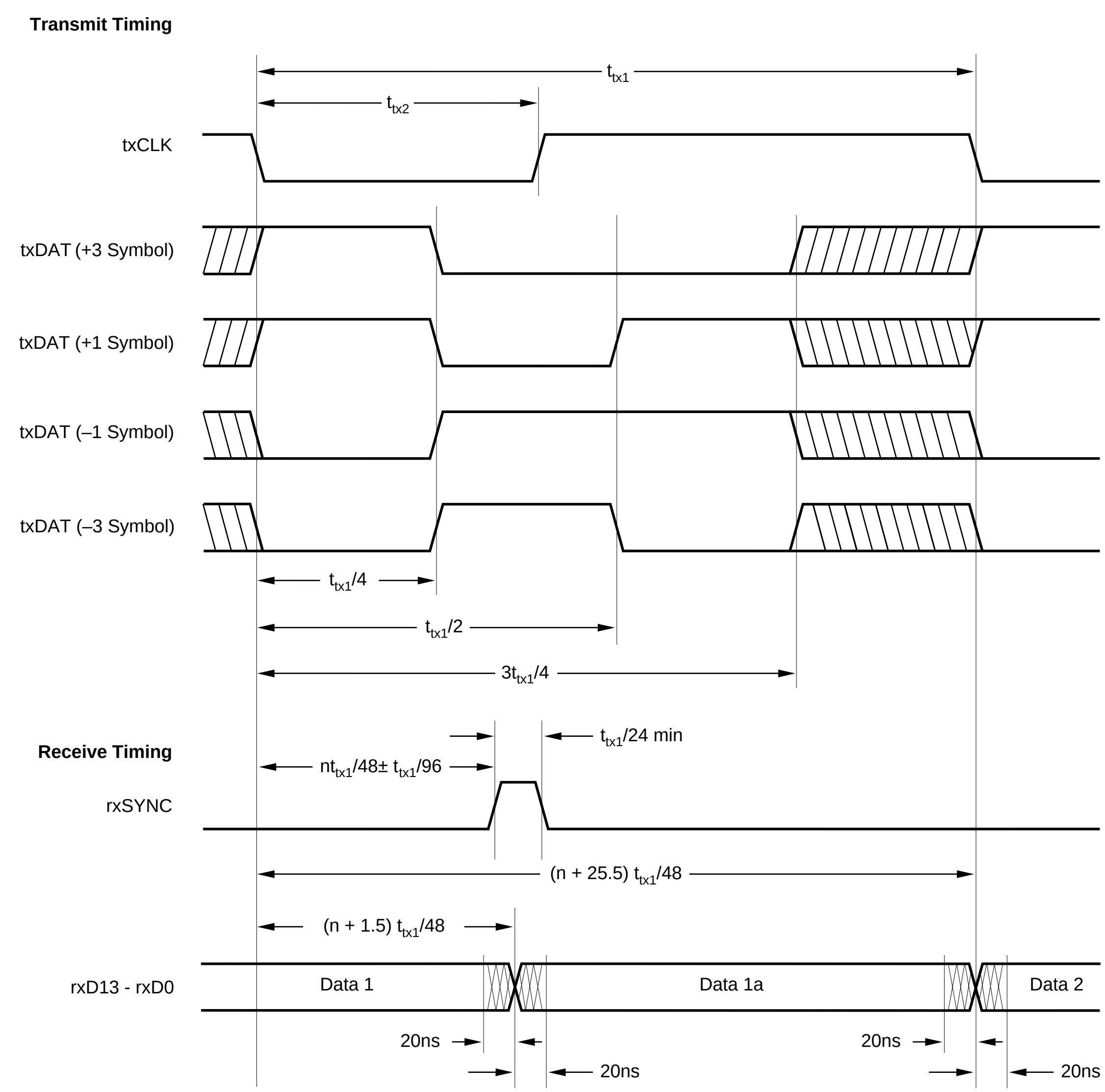
This circuit applies at both T1 and E1 rates. For slower rates, the antialiasing filters will give best performance with their –3dB frequency approximately equal to the bit rate. For example, a –3dB frequency of 500kHz should be used for a single pair bit rate of 500kbps.

rxHYB AND rxLINE INPUT BIAS VOLTAGE

The transmitter output on the txLINE pins is centered at midscale, 2.5V. But, the rxLINE input signal is centered at 1.5V in the circuit shown in Figure 2 above.

Inside the AFE1105, the rxHYB and rxLINE signals are subtracted as described in the paragraph on echo cancellation above. This means that the rxHYB inputs need to be centered at 1.5V just as the rxLINE signal is centered at 1.5V. REF_N (Pin 36) is a 1.5V voltage source. The external compromise hybrid must be designed so that the signal into the rxHYB inputs is centered at 1.5V.

TIMING DIAGRAM



NOTES: (1) Any transmit sequence not shown will result in a zero symbol. (2) All transitions are specified relative to the falling edge of txCLK. (3) Maximum allowable error for any txDAT edge is $\pm t_{tx1}/12$ (±17.8ns at E1 rate; ±26.6ns at T1 rate). (4) Both txDAT inputs are read by the AFE1103 at 1/8, 3/8, and 5/8 of a symbol period from the rising edge of txCLK. (5) rxSYNC can shift to one of 48 discrete delay times from the falling edge of txCLK. (6) It is recommended that rxD13 - rxD0 be read on the rising edge of rxSYNC.

FIGURE 3. Timing Diagram.

RECEIVE TIMING

The rxSYNC signal controls portions of the A/D converter's decimation filter and the data output timing of the A/D converter. It is generated at the symbol rate by the user and must be synchronized with txCLK. The rising edge of rxSYNC can occur at the falling edge of txCLK or it can be shifted by the user in increments of 1/48 of a symbol period to one of 47 discrete delay times after the falling edge of txCLK.

The bandwidth of the A/D converter decimation filter is equal to one half of the symbol rate. The A/D converter data output rate is 2X the symbol rate. The specifications of the AFE1105 assume that one A/D converter output is used per symbol period and the other interpolated output is ignored. The Receive Timing Diagram above suggests using the rxSYNC pulse to read the first data output in a symbol period. Either data output may be used. Both data outputs may be used for more flexible post-processing.

DISCUSSION OF SPECIFICATIONS

UNCANCELLED ECHO

The key measure of transceiver performance is uncancelled echo. This measurement is made as shown in the diagram of Figure 4. The AFE is connected to an output circuit including a typical 1:2 line transformer. The line is simulated by a 135Ω resistor. Symbol sequences are generated by the tester and applied both to the AFE and to the input of an adaptive filter. The output of the adaptive filter is subtracted from the AFE output to form the uncancelled echo signal. Once the filter taps have converged, the RMS value of the uncancelled echo is calculated. Since there is no far-end signal source or additive line noise, the uncancelled echo contains only noise and linearity errors generated in the transmitter and receiver.

The data sheet value for uncancelled echo is the ratio of the RMS uncancelled echo (referred to the receiver input through the receiver gain) to the nominal transmitted signal (13.5dBm into 135Ω, or 1.74Vrms). This echo value is measured under a variety of conditions: with loopback enabled (line input disconnected); with loopback disabled under all receiver gain ranges; and with the line shorted (S_1 closed in Figure 4).

LAYOUT

The analog front end of an HDSL system has a number of conflicting requirements. It must accept and deliver digital outputs at fairly high rates of speed, phase-lock to a high-speed digital clock, and convert the line input to a high-precision (14-bit) digital output. Thus, there are really three sections of the AFE1105: the digital section, the phase-locked loop, and the analog section.

The power supply for the digital section of the AFE1105 can range from 3.3V to 5V. This supply should be decoupled to digital ground with a ceramic 0.1µF capacitor placed as close to DGND (pin 12) and DV_{DD} (pin 13) as possible. Ideally, both a digital power supply plane and a digital ground plane should run up to and underneath the digital pins of the AFE1105 (pins 3 through 26). However, DV_{DD} may be supplied by a wide printed circuit board (PCB) trace. A digital ground plane underneath all digital pins is strongly recommended.

The phase-locked loop is powered from PV_{DD} (pin 2) and its ground is referenced to PGND (pin 1). Note that PV_{DD} must be in the 4.75V to 5.25V range. This portion of the AFE1105 should be decoupled with both a 10µF Tantalum capacitor

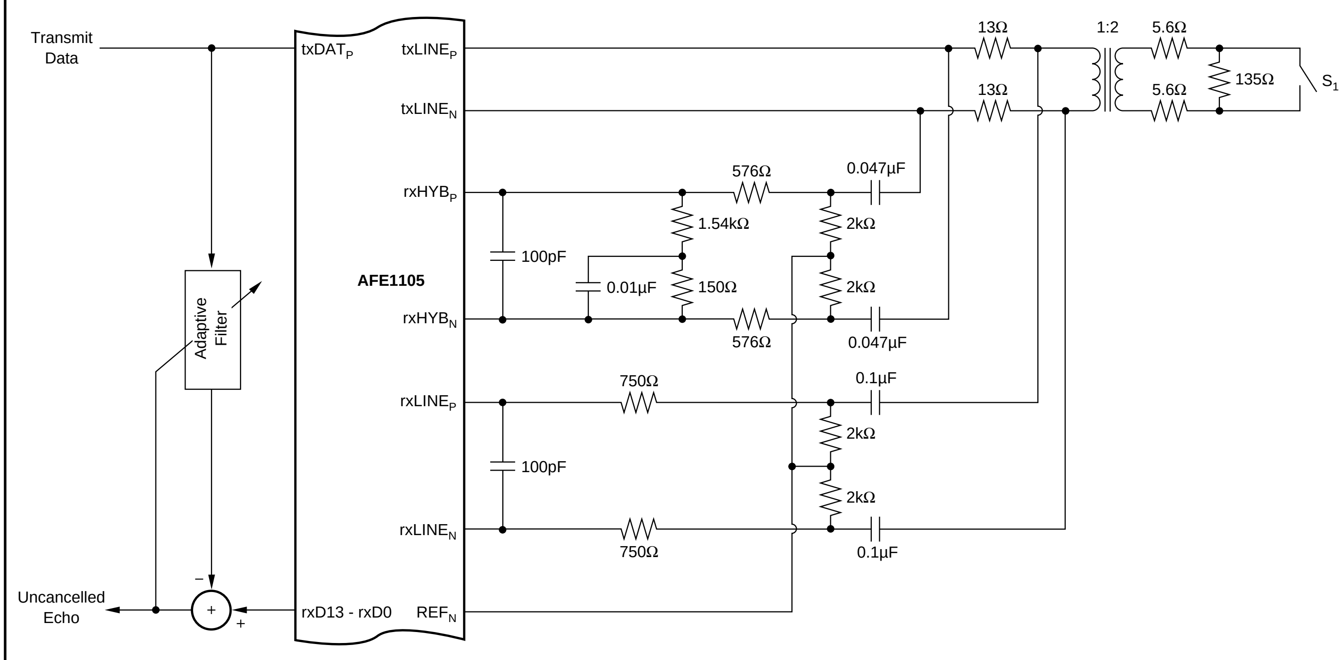


FIGURE 4. Uncancelled Echo Test Diagram.

and a 0.1μF ceramic capacitor. The ceramic capacitor should be placed as close to the AFE1105 as possible. The placement of the Tantalum capacitor is not as critical, but should be close. In each case, the capacitor should be connected between PV_{DD} and PGND.

In most systems, it will be natural to derive PV_{DD} from the AV_{DD} supply. A 5Ω to 10Ω resistor should be used to connect PV_{DD} to the analog supply. This resistor in combination with the 10μF capacitor form a lowpass filter—keeping glitches on AV_{DD} from affecting PV_{DD}. Ideally, PV_{DD} would originate from the analog supply (via the resistor) near the power connector for the printed circuit board. Likewise, PGND should connect to a large PCB trace or small ground plane which returns to the power supply connector underneath the PV_{DD} supply path. The PGND "ground plane" should also extend underneath PLL_{IN} and PLL_{OUT} (pins 47 and 48).

The remaining portion of the AFE1105 should be considered analog. All AGND pins should be connected directly to a common analog ground plane and all AV_{DD} pins should be connected to an analog 5V power plane. Both of these planes should have a low impedance path to the power supply.

Ideally, all ground planes and traces and all power planes and traces should return to the power supply connector before being connected together (if necessary). Each ground and power pair should be routed over each other, should not overlap any portion of another pair, and the pairs should be separated by a distance of at least 0.25 inch (6mm). One exception is that the digital and analog ground planes should be connected together underneath the AFE1105 by a small trace.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
AFE1105E	ACTIVE	SSOP	DL	48	30	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
AFE1105E/1K	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
AFE1105E/1KG4	ACTIVE	SSOP	DL	48	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
AFE1105EG4	ACTIVE	SSOP	DL	48	30	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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