

December 1996

Fast CMOS 3.3V 8-Bit Transparent Latch

Features

- Advanced 0.6 micron CMOS Technology
- Compatible with LCX™ Families of Products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input Can Be 3V or 5V
 - Output Can Be 3V or Connected to 5V Bus
- Advanced Low Power CMOS Operation
- Excellent Output Drive Capability:
 - Balanced Drives (24mA Sink and Source)
- Low Ground Bounce Outputs
- Hysteresis on All Inputs

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD74LPT373AM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT373AQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT373CM	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT373CQM	-40 to 85	20 Ld QSOP	M20.15-P
CD74LPT373M	-40 to 85	20 Ld SOIC	M20.3-P
CD74LPT373QM	-40 to 85	20 Ld QSOP	M20.15-P

NOTE: QSOP is commonly known as SSOP.

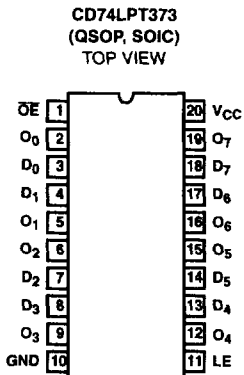
When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

Description

The CD74LPT373 is an 8-bit transparent latch designed with three-state outputs and is intended for bus oriented applications. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When \overline{OE} is HIGH, the bus output is in the high impedance state.

The CD74LPT373 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

Pinout

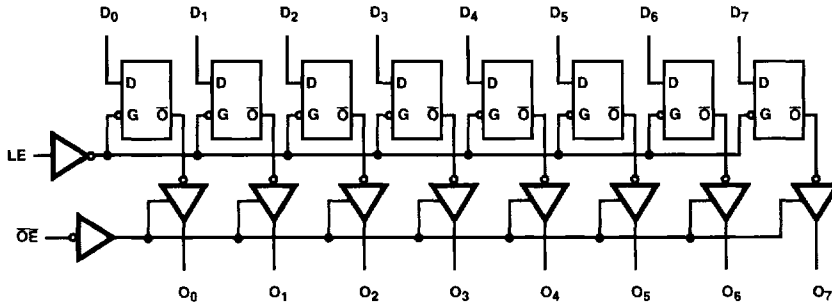


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Functional Block Diagram



TRUTH TABLE (NOTE 1)

INPUTS			OUTPUTS
D _N	LE	OE	O _N
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance

Pin Descriptions

PIN NAME	DESCRIPTION
OE	Output Enable Input (Active LOW)
LE	Latch Enable Input (Active HIGH)
D ₇ -D ₀	Data Inputs
O ₇ -O ₀	Three-State Outputs
GND	Ground
V _{CC}	Power

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Electrical Specifications (Continued)

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS	MIN	(NOTE 4) TYP	MAX	UNITS		
Short Circuit Current (Note 6)	I_{OS}	$V_{CC} = \text{Max (Note 5), } V_{OUT} = \text{GND}$	-60	-85	-240	mA		
Power Down Disable	I_{OFF}	$V_{CC} = 0V, V_{IN} \text{ or } V_{OUT} \leq 4.5V$	-	-	± 100	μA		
Input Hysteresis	V_H		-	150	-	mV		
CAPACITANCE $T_A = 25^\circ C, f = 1\text{MHz}$								
Input Capacitance (Note 8)	C_{IN}	$V_{IN} = 0V$	-	4.5	6	pF		
Output Capacitance (Note 8)	C_{OUT}	$V_{OUT} = 0V$	-	5.5	8	pF		
POWER SUPPLY SPECIFICATIONS								
Quiescent Power Supply Current	I_{CC}	$V_{CC} = \text{Max}$		$V_{IN} = \text{GND}$ or V_{CC}	-	0.1	10	μA
Quiescent Power Supply Current TTL Inputs HIGH	ΔI_{CC}	$V_{CC} = \text{Max}$		$V_{IN} = V_{CC} - 0.6V$ (Note 9)	-	2.0	30	μA
Dynamic Power Supply (Note 10)	I_{CCD}	$V_{CC} = \text{Max, Outputs Open}$ $\overline{OE} = \text{GND}$ One Bit Toggling 50% Duty Cycle		$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	50	75	$\mu A/\text{MHz}$
Total Power Supply Current (Note 12)	I_C	$V_{CC} = \text{Max, Outputs Open}$ $f_1 = 10\text{MHz, 50\% Duty Cycle}$ $\overline{OE} = \text{GND}$ One Bit Toggling		$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	-	0.6	2.3	mA
		$V_{CC} = \text{Max, Outputs Open}$ $f_1 = 2.5\text{MHz, 50\% Duty Cycle}$ $\overline{OE} = \text{GND}$ 8 Bits Toggling		$V_{IN} = V_{CC} - 0.6V$ $V_{IN} = \text{GND}$	-	2.1	4.7 (Note 11)	mA

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Switching Specifications Over Operating Range (Note 13)

PARAMETER	SYMBOL	(NOTE 14) TEST CONDITIONS	CD74LPT373		CD74LPT373A		CD74LPT373C		UNITS
			(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	(NOTE 15) MIN	MAX	
Propagation Delay D_X to O_X	t_{PLH} , t_{PHL}	$C_L = 50pF$ $R_L = 500\Omega$	1.5	8.0	1.5	5.2	1.5	4.2	ns
Propagation Delay LE to O_X	t_{PLH} , t_{PHL}		2.0	8.5	2.0	8.5	2.0	5.5	ns
Output Enable Time $\bar{O}E$ to O_X	t_{PZH} , t_{PZL}		1.5	8.5	1.5	6.5	1.5	5.5	ns
Output Disable Time (Note 16) $\bar{O}E$ to O_X	t_{PHZ} , t_{PLZ}		1.5	7.5	1.5	5.5	1.5	5.0	ns
Setup Time HIGH or LOW, D_X to LE	t_{SU}		2.0	-	2.0	-	2.0	-	ns
Hold Time HIGH or LOW, D_X to LE	t_H		1.5	-	1.5	-	1.5	-	ns
LE Pulse Width (Note 16) HIGH	t_W		6.0	-	5.0	-	5.0	-	ns
Output Skew (Note 17)	$t_{SK(O)}$		-	0.5	-	0.5	-	0.5	ns

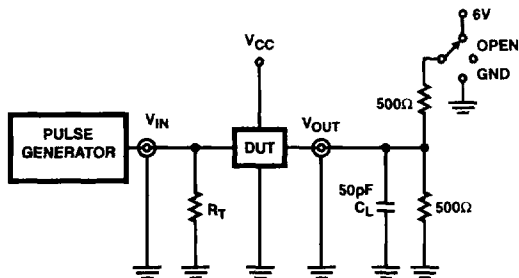
NOTES:

3. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
4. Typical values are at $V_{CC} = 3.3V$, 25°C ambient and maximum loading.
5. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
6. This parameter is guaranteed but not tested.
7. $V_{OH} = V_{CC} - 0.6V$ at rated current.
8. This parameter is determined by device characterization but is not production tested.
9. Per TTL driven input; all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
11. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
12. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} =$ Quiescent Current
 $\Delta I_{CC} =$ Power Supply Current for a TTL High Input
 $D_H =$ Duty Cycle for TTL Inputs High
 $N_T =$ Number of TTL Inputs at D_H
 $I_{CCD} =$ Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 $f_{CP} =$ Clock Frequency for Register Devices (Zero for Non-Register Devices)
 $f_i =$ Input Frequency
 $N_i =$ Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.
13. Propagation Delays and Enable/Disable times are with $V_{CC} = 3.3V \pm 0.3V$, normal range. For $V_{CC} = 2.7V$, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
14. See test circuit and wave forms.
15. Minimum limits are guaranteed but not tested on Propagation Delays.
16. This parameter is guaranteed but not production tested.
17. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

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Test Circuits and Waveforms



NOTE:

18. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $Z_{OUT} \leq 50\Omega$;
 $t_r, t_f \leq 2.5\text{ns}$.

FIGURE 1. TEST CIRCUIT

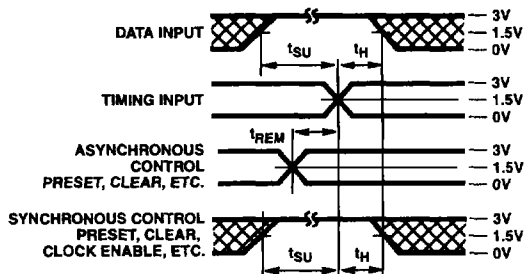


FIGURE 2. SETUP, HOLD, AND RELEASE TIMING

SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}, t_{PZL}, \text{Open Drain}$	6V
t_{PHZ}, t_{PZH}	GND
t_{PLH}, t_{PHL}	Open

DEFINITIONS:

C_L = Load capacitance, includes jig and probe capacitance.

R_T = Termination resistance, should be equal to Z_{OUT} of the Pulse Generator.

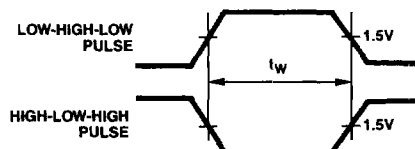


FIGURE 3. PULSE WIDTH

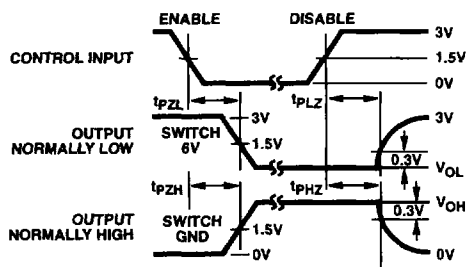


FIGURE 4. ENABLE AND DISABLE TIMING

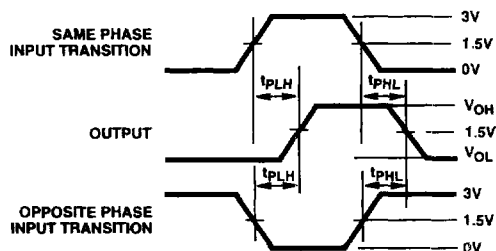


FIGURE 5. PROPAGATION DELAY