COS/MOS 64-Stage Static Shift Register

The RCA-CD4031A is a 64-stage static shift register in which each stage is a D-type, master-slave flip-flop.

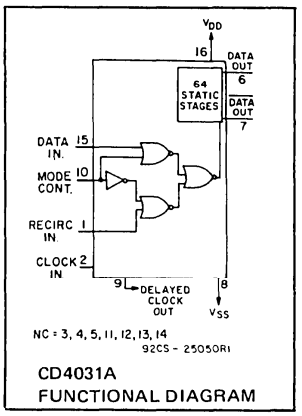
The logic level present at the DATA input is transferred into the first stage and shifted one stage at each positive-going clock transition. Maximum clock frequencies up to 4 Megahertz (typical) can be obtained. Because fully static operation is allowed, information can be permanently stored with the clock line in either the low or high state. The CD4031A has a MODE CONTROL input that, when in the high state, allows operation in the recirculating mode. Register packages can be cascaded and the clock lines driven directly for high speed operation. Alternatively, a delayed clock output (CL_D) is provided that enables cascading register packages while allowing reduced clock drive fan-out and rise- and fall-time requirements.

Data (Q) and $\overline{Data}$ ($\overline{Q}$) outputs are provided from the 64th register stage. The Data (Q) output is capable of drving one TTL or DTL load.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **Fully static operation: DC to 4 MHz typ. @ $V_{DD} - V_{SS} = 10$ V**
- **Operation from a single 3 to 15 V positive or negative power supply**
- **High noise immunity**
- **Microwatt quiescent power dissipation: 10 μW (typ.) for ceramic packages; 100 μW (typ.) for plastic packages**



CD4031A
FUNCTIONAL DIAGRAM

- **Single phase clocking requirements**
- **Recirculation capability**
- **Data compatible with TTL-DTL**
- **Two cascading modes:**
  - **Direct clocking for high-speed operation**
  - **Delayed clocking for reduced clock drive requirements**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Serial shift registers**
- **Time delay circuits**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, H . . . . . -55 to +125°C

PACKAGE TYPE E . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Hold Time, t_H	5	100	–	100	–	ns
	10	200	–	200	–	
Clock Pulse Width, t_W	5	2.5	–	2.6	–	μs
	10	1	–	1.3	–	
Clock Input Frequency, f_{CL}	5	dc	0.8	dc	0.4	MHz
	10	dc	2	dc	1	
Clock Rise and Fall Time, t_rCL, t_fCL*	5	–	2	–	2	μs
	10	–	1	–	1	

* If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF and the transition time of the output driving stage.

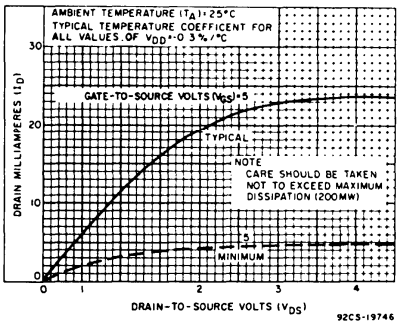


Fig. 1 – Typical and minimum output n-channel drain characteristics for Q output.

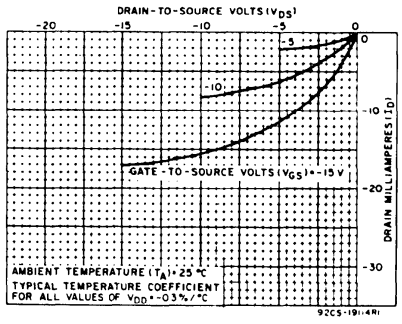
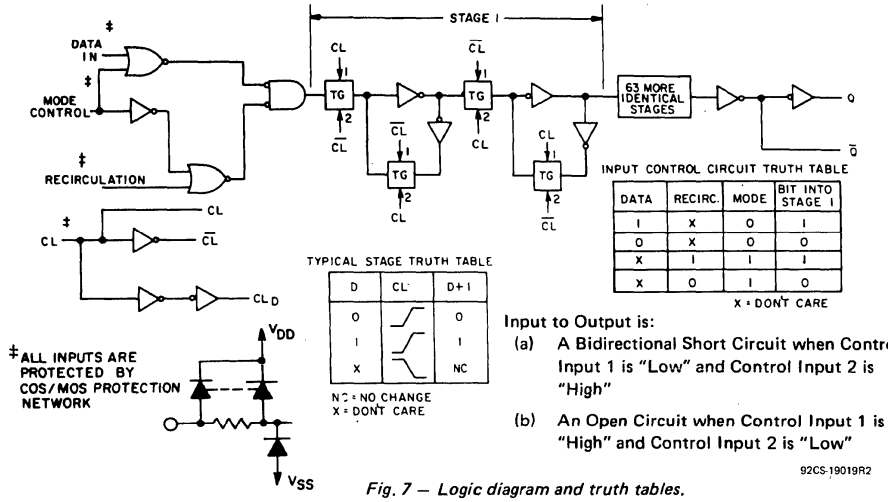


Fig. 2 – Typical output p-channel drain characteristics for Q output.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS		CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
					D, F, H PACKAGES				E PACKAGE				
		V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.		–	–	5	10	0.5	10	600	50	1	50	700	μA
		–	–	10	25	1	25	1500	100	2	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}		–	5	5	0 Typ.; 0.05 Max								V
		–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.								
		–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	Q	0.4	–	4.5	1.6	2.6	1.3	0.91	1.6	2.6	1.3	1.05	mA
		0.5	–	10	5	8	4	3.2	5	8	4	3.2	
	$\overline{Q}$	0.5	–	5	0.11	0.18	0.09	0.06	0.05	0.18	0.045	0.037	
		0.5	–	10	0.24	0.4	0.2	0.14	0.12	0.4	0.1	0.08	
	CL_D	0.5	–	5	0.48	0.8	0.4	0.28	0.24	0.8	0.2	0.16	
		0.5	–	10	1.5	2.4	1.2	0.84	0.75	2.4	0.6	0.5	
P- Channel (Source): I_DP Min.	Q	4.5	–	5	-0.4	-0.64	-0.32	-0.22	-0.20	-0.64	-0.16	-0.13	
		9.5	–	10	-0.85	-1.4	-0.70	-0.49	-0.42	-1.4	-0.35	-0.29	
	$\overline{Q}$	4.5	–	5	-0.11	-0.18	-0.09	-0.06	-0.05	-0.18	-0.045	-0.037	
		9.5	–	10	-0.24	-0.4	-0.20	-0.14	-0.12	-0.4	-0.10	-0.08	
	CL_D	4.5	–	5	-0.48	-0.8	-0.40	-0.28	-0.24	-0.8	-0.20	-0.16	
		9.5	–	10	-1	-1.6	-0.80	-0.56	-0.5	-1.6	-0.40	-0.32	
Input Leakage Current, I_{IL}, I_{IH}		Any Input	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA



TYPICAL STAGE TRUTH TABLE

D	CL	D+1
0	↑	0
1	↑	1
X	↓	NC

NC = NO CHANGE
X = DON'T CARE

INPUT CONTROL CIRCUIT TRUTH TABLE

DATA	RECIRC.	MODE	BIT INTO STAGE I
1	X	0	1
0	X	0	0
X	1	1	1
X	0	1	0

X = DON'T CARE

Input to Output is:

(a) A Bidirectional Short Circuit when Control Input 1 is "Low" and Control Input 2 is "High"

(b) An Open Circuit when Control Input 1 is "High" and Control Input 2 is "Low"

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Fig. 7 – Logic diagram and truth tables.

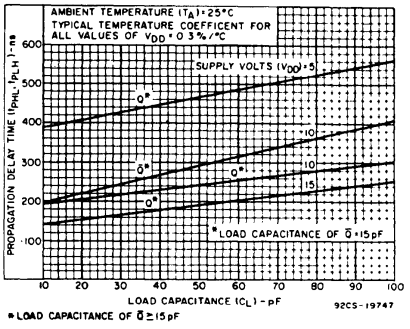


Fig. 3 – Typical propagation delay time vs. load capacitance for data outputs.

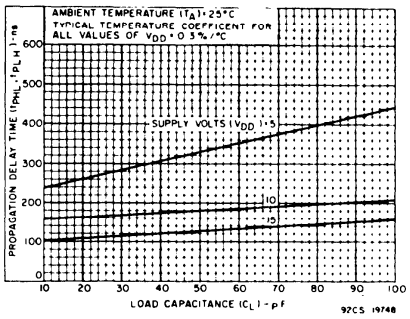


Fig. 4 – Typical propagation delay vs. load capacitance for delayed clock output.

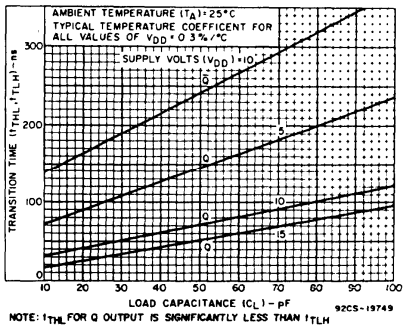


Fig. 5 – Typical transition time vs. load capacitance for data outputs.

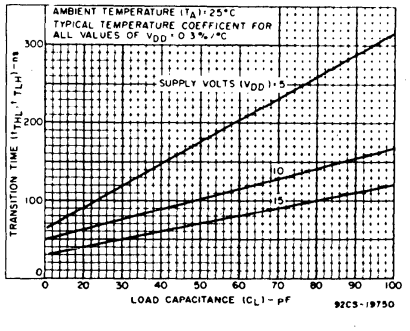


Fig. 6 – Typical transition time vs. load capacitance for delayed clock output.

DYNAMIC ELECTRICAL CHARACTERISTICS

at T_A=25°C, Input t_r,t_f=20 ns, C_L=15 pF (unless otherwise specified), R_L=200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D, F, H			E			
		V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time; t_{PLH}, t_{PHL}		5	–	400	800	–	400	1600	ns
Clock to Data Output Q & $\overline{Q}$ *		10	–	200	400	–	200	800	
Clock to CL_D	C_L = 60 pF	5	–	400	800	–	400	1600	
		10	–	200	400	–	200	800	
Transition Time; t_{THL}, t_{TLH} Q Output		5	–	75	150	–	75	300	ns
		10	–	30	60	–	30	120	
$\overline{Q}$ Output		5	–	300	600	–	300	1200	
		10	–	150	300	–	150	600	
CL_D Output	C_L = 60 pF	5	–	200	400	–	200	800	
		10	–	100	200	–	100	400	
Clock Rise and Fall Time; t_rCL, t_fCL**		5	–	–	2	–	–	2	μs
		10	–	–	1	–	–	1	
Minimum Data Set-Up Time, t_S		5	–	200	400	–	200	800	ns
		10	–	50	100	–	50	200	
Maximum Clock Input Frequency, f_{CL}***		5	0.8	2	–	0.4	2	–	MHz
		10	2	4	–	1	4	–	
Minimum Data Hold Time, t_H		5	–	50	100	–	50	100	ns
		10	–	100	200	–	100	250	
Minimum Clock Pulse Width, t_W		5	–	1.25	2.5	–	1.3	2.6	μs
		10	–	0.5	1	–	0.62	1.3	
Average Input Capacitance, C_I Clock			–	60	–	–	60	–	pF
All Others			–	5	–	–	5	–	

* Capacitive loading on $\overline{Q}$ output affects propagation delay of Q output. These limits apply for $\overline{Q}$ load $C_L \leq 15$ pF.

** If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF and the transition time of the output driving stage.

*** Maximum Clock Frequency for Cascaded Units;

a) Using Delayed Clock Feature –

$$f_{max} = \frac{1}{(n-1)\,CL_D \text{ prop. delay} + Q \text{ prop. delay} + \text{set-up time}}$$ where n = number of packages

b) Not Using Delayed Clock – $f_{max} = \frac{1}{\text{propagation delay} + \text{set-up time}}$

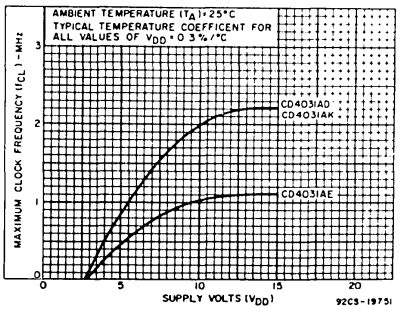


Fig. 8 – Maximum clock input frequency vs. supply voltage.

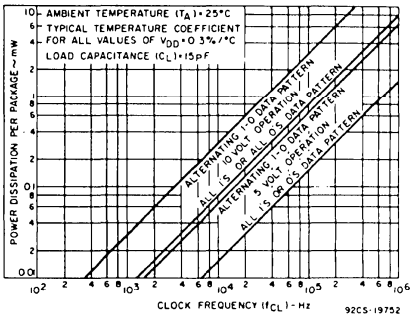


Fig. 9 – Typical power dissipation vs. frequency.

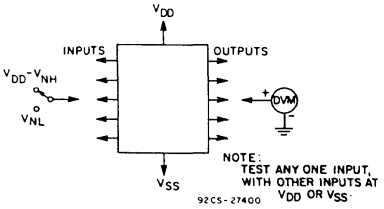


Fig. 10 – Noise-immunity test circuit.

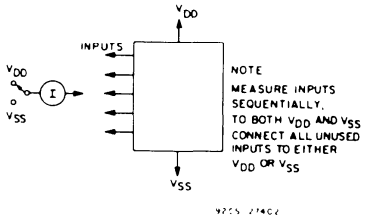
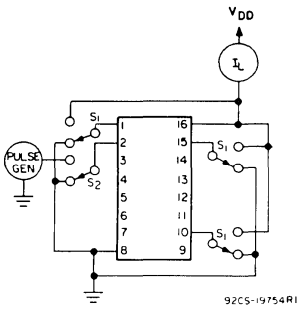
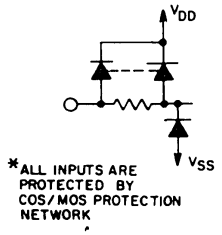


Fig. 11 – Input-leakage-current test circuit.



WITH S_1 AT GROUND, CLOCK UNIT 64 TIMES BY CONNECTING S_2 TO PULSE GENERATOR RETURN S_2 TO GND AND MEASURE LEAKAGE CURRENT. REPEAT WITH S_1 AT V_{DD}.

Fig. 13 – Quiescent-device-current test circuit.



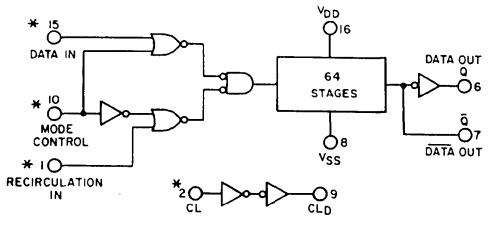


Fig. 12 – Functional diagram.